PRODUCT SPECIFICATION

DESCRIPTION

TFT Module – 4.3” HVGA
480 x (RGB) x 272
Full viewing angle High brightness

PART NUMBER

LT180408-043NT

VERSION

1.0

ROHS COMPLIANT

Revision Status

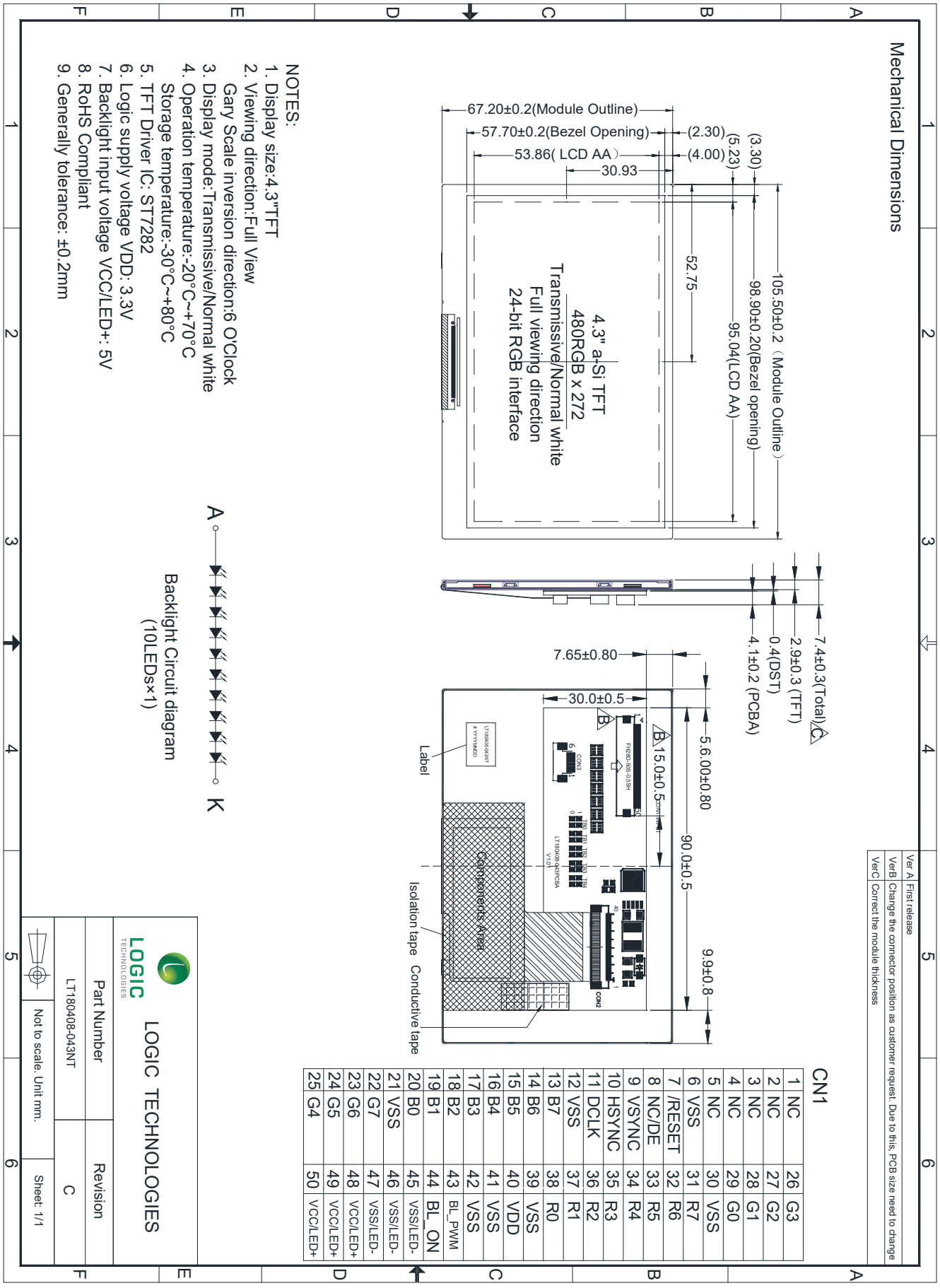
Revision	Revision Date	Page	Content	Notes
1.0	04.12.2018		Initial release	

Table of Contents

- GENERAL INFORMATION

Item	Contents	Unit
LCD Type	TFT Transmissive, anti-glare	/
Technology	a-Si TFT	-
Viewing Direction	Full View	O'clock
Viewing Angle (Gray Scale Inversion Direction)	6:00	O'clock
Module dimensions (W x H x T)	105.5x 67.2 x 7.7(Max)	mm
Active area (W x H)	95.04 x 53.86	mm
Number of pixels	480 x 3 (RGB) x 272	/
Pixel pitch (W x H)	0.198 x 0.198	mm2
Colours	16.7M	/
Contrast ratio	500 (typical)	/
Backlight	LED (10 in serial)	/
Backlight Brightness	600(typical)	cd/m2
Interface	RGB 24bit + TCON	/
Touch solution	Without Touch	/
Touch driver	NA	/
Touch Interface	NA	/
Operating temperature	-20 to +70	°C
Storage temperature	-30 to +80	°C

- MECHANICAL DIMENSIONS



- ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Min.	Max.	Unit	Note
Power Voltage	VDD	- 0.5	4.0	V	---
Backlight LED Forward Current	I_F	---	25	mA	One LED
Operating Temperature	T_{OPR}	- 20	70	°C	---
Storage temperature	T_{ST}	- 30	80	°C	---

- ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Min	Typ.	Max	Unit	Note
Supply Voltage		V_{DD}	3.0	3.3	3.6	V	
Input Signal Voltage	Low Level	V_{IL}	0	---	0.2xVDD	V	Note1
	High Level	V_{IH}	0.8xVDD	---	VDD	V	
Output Signal Voltage	Low Level	V_{OL}	0	---	0.2xVDD	V	
	High Level	V_{OH}	0.8xVDD	---	VDD	V	
Power Consumption (TFT panel only)		Black Mode (60Hz)	---	75	135	mW	

Note 1: Signals include R0~R7, G0~G7, B0~B7, CLKIN, STBYB, Hsync, Vsync, DE

- BACKLIGHT CHARACTERISTICS

Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Driver Input Voltage	VCC/LED+	---	5	6	V	
Current of driver IC	IVLED	---	172	256	mA	
Power Consumption	P_{BL}	---	860	1536	mW	
PWM Frequency	PWM	100	150	200	Hz	10 series LEDs
Forward Current	IF	---	20	25	mA	
Forward Current Voltage	VF	---	31	35	V	
LED Lifetime	---	30k	---	---	Hrs	

NOTES

Backlight drive conditions : constant current driving method.

- The LED driving condition is defined for total backlight consumption.
- Forward Voltage adjustment depends on the Forward Current setting.
- One LED : max IF = 25mA, VF = 3.2V
- I_F is defined for one channel LED.
- If the LEDs are driven by high current, high ambient temperature & humidity condition the lifetime of the LEDs will be reduced.
- Operating life means brightness reduces to 50% of initial brightness.
- Typical operating life time is estimated data.
- Backlight Connection Internal Diagram

- ELECTRO-OPTICAL CHARACTERISTICS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Refer	Note
Response Time		T_{ON}	25°C	---	20	30	ms	Fig 1	1
		T_{OFF}							
Contrast ratio		Cr	θ=0°	---	500	---	---	Fig 2	1
Uniformity		U	---	---	75	---	%	Fig 2	3
NTSC		---	---	---	50	---	%		
Surface Luminance		Lv		500	600	---	cd/m^2	Fig 2	2
Viewing angle ratio		Cr=10	∅=Top	60	75	---	deg	Fig 3	6
			∅=Bottom	60	75	---			
			∅=Left	60	75	---			
			∅=Right	60	75	---			
CIE (x,y) chromaticity	Red	x	Backlight On	0.559	0.609	0.659	---	Fig 2.	5
		y		0.305	0.355	0.405			
	Green	x		0.277	0.315	0.364			
		y		0.505	0.555	0.605			
	Blue	x		0.089	0.136	0.189			
		y		0.089	0.139	0.189			
	White	x		0.254	0.304	0.354			
		y		0.294	0.344	0.394			

Note

1. Contrast ratio (CR) is defined mathematically in Figure 2.

$$\text{Contrast Ratio} = \frac{\text{Average Surface Luminance with all white pixels (P1, P2, P3, P4, P5)}}{\text{Average Surface Luminance with all black pixels (P1, P2, P3, P4, P5)}}$$

Note 2. Surface luminance is the LCD surface from the surface with all pixels displaying white. For more information see figure 2.

Lv = Average Surface Luminance with all white pixels (P1, P2, P3, P4, P5…)

Note 3. Uniformity of surface luminance, White, is defined mathematically in figure 2.

$$\text{White} = \frac{\text{Minimum Surface Luminance with all white pixels (P1, P2, P3, P4, P5)}}{\text{Maximum Surface Luminance with all white pixels (P1, P2, P3, P4, P5)}}$$

Note 4. Response time is the time required for the display to transition form white to black (rise time Tr) and from black to white (decay or fall time, Tf). The industry standard test equipment used is the Autronic-Melcher's Conoscope.

Note 5. CIE (x,y) chromaticity. The x,y value is determined by measuring luminance at each test position 1 through 5, then calculating the average value.

Note 6. The Viewing angle is the angle at which the contrast ratio is greater than 2. For a TFT module, the contrast ratio is greater than 10. The angles are determined for the horizontal or 'x' axis and the vertical or 'y' axis with respect to the 'z' axis, being the LCD surface reference. Also see figure 3.

Note 7. For viewing angle and response time testing, the testing data is based on Autronic-Melcher's BM-7A. For the contrast ratio, surface luminance, luminance uniformity and chromaticity (CIE), the test data is based on the industry's standard SR-3A photo detector.

Note 8. For TFT modules, grey scale reversing occurs in the direction of the panel viewing angle.

Figure 1. Definition of response time

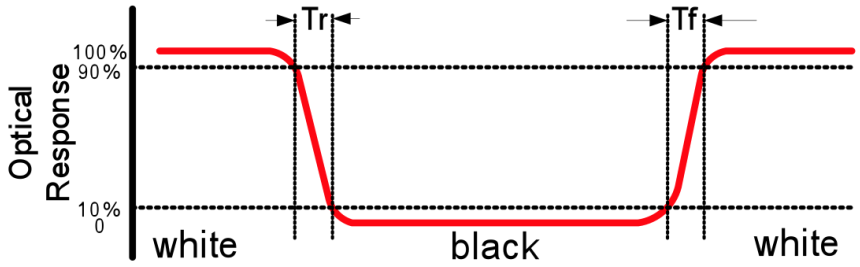


Figure 2. Measuring contrast ratio, surface luminance, luminance uniformity and CIE (chromaticity.)

A : 5mm, B : 5mm, H, V : Active area, Light spot size: dir=5mm, distance from the LCD surface to the detector lens 500mm. Measurement instrument is Topcon's luminance meter BM-5.

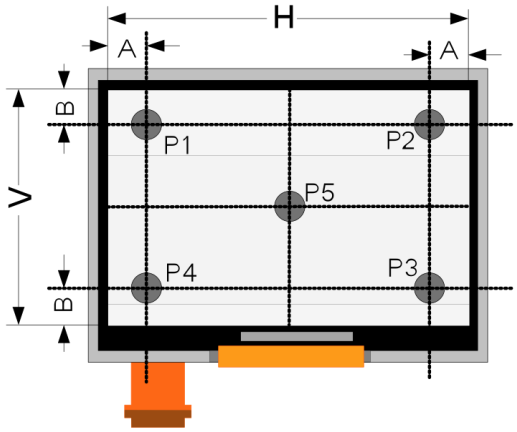
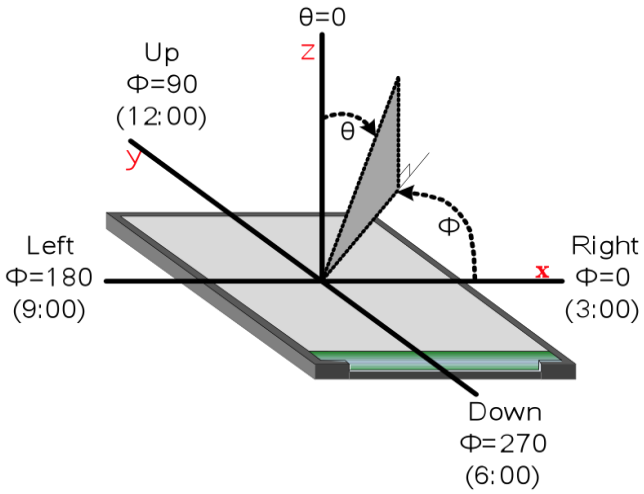


Figure 3. Definition of viewing angle



- INTERFACE DESCRIPTION

Pin	Symbol	I/O	Description	Note
1	T_/INT(YU)	I/O	Cap touch wake up /Interrupt; Resistive touch YU terminal; NC when no touch.	
2	T_NC(XL)	I/O	Resistive touch XU terminal; NC when with cap touch or no touch.	
3	T_/RST(YD)	I/O	Cap touch /Reset pin; Resistive touch YD terminal; NC when no touch.	
4	T_SDA(XR)	I/O	Cap touch I2C data input/output pin; Resistive touch XR terminal; NC when no touch.	
5	T_SCL	I	Cap touch I2C clock input pin; NC when with resistive touch or no touch.	
6	VSS	P	TFT&CTP Ground	
7	/RESET	I	TFT display system reset	
8	NC/DE	I	NC	Note1
9	VSYNC	I	Vertical Synch Input	
10	HSYNC	I	Horizontal Synch Signal	
11	DCLK	I	Display Pixel Clock	
12	VSS	I	TFT&CTP Ground	
13	B7	I	Blue data signal (MSB)	
14	B6	I	Blue data signal	
15	B5	I	Blue data signal	
16	B4	I	Blue data signal	
17	B3	I	Blue data signal	
18	B2	I	Blue data signal	
19	B1	I	Blue data signal	
20	B0	I	Blue data signal (LSB)	
21	VSS	P	TFT&CTP Ground	
22	G7	I	Green data signal (MSB)	
23	G6	I	Green data signal	
24	G5	I	Green data signal	
25	G4	I	Green data signal	
26	G3	I	Green data signal	
27	G2	I	Green data signal	

28	G1	I	Green data signal	
29	G0	I	Green data signal (LSB)	
30	VSS	P	TFT&CTP Ground	
31	R7	I	Red data signal (MSB)	
32	R6	I	Red data signal	
33	R5	I	Red data signal	
34	R4	I	Red data signal	
35	R3	I	Red data signal	
36	R2	I	Red data signal	
37	R1	I	Red data signal	
38	R0	I	Red data signal (LSB)	
39	VSS	P	TFT&CTP Ground	
40	VDD	P	TFT&CTP Power supply, 3.3V	
41	VSS	P	TFT&CTP Ground	
42	VSS	P	TFT&CTP Ground	
43	BL_PWM	I	PWM signal to control backlight diming. 100~200Hz	
44	BL_ON	I	Backlight on/off control pin. H: On ; L: Off	
45	VSS/LED-	P	Backlight Ground which is LED Cathode. R19=0ohm to connect it to TFT&CTP Ground	
46	VSS/LED-	P		
47	VSS/LED-	P		
48	VCC/LED+	P	Backlight supply voltage input, 5V typical	
49	VCC/LED+	P		
50	VCC/LED+	P		

I -Input only; O -Output only; I/O -Input /output; P -Power or Ground.

Suggested connection for this connector is 0.5pitch 50pins FFC or FPC.

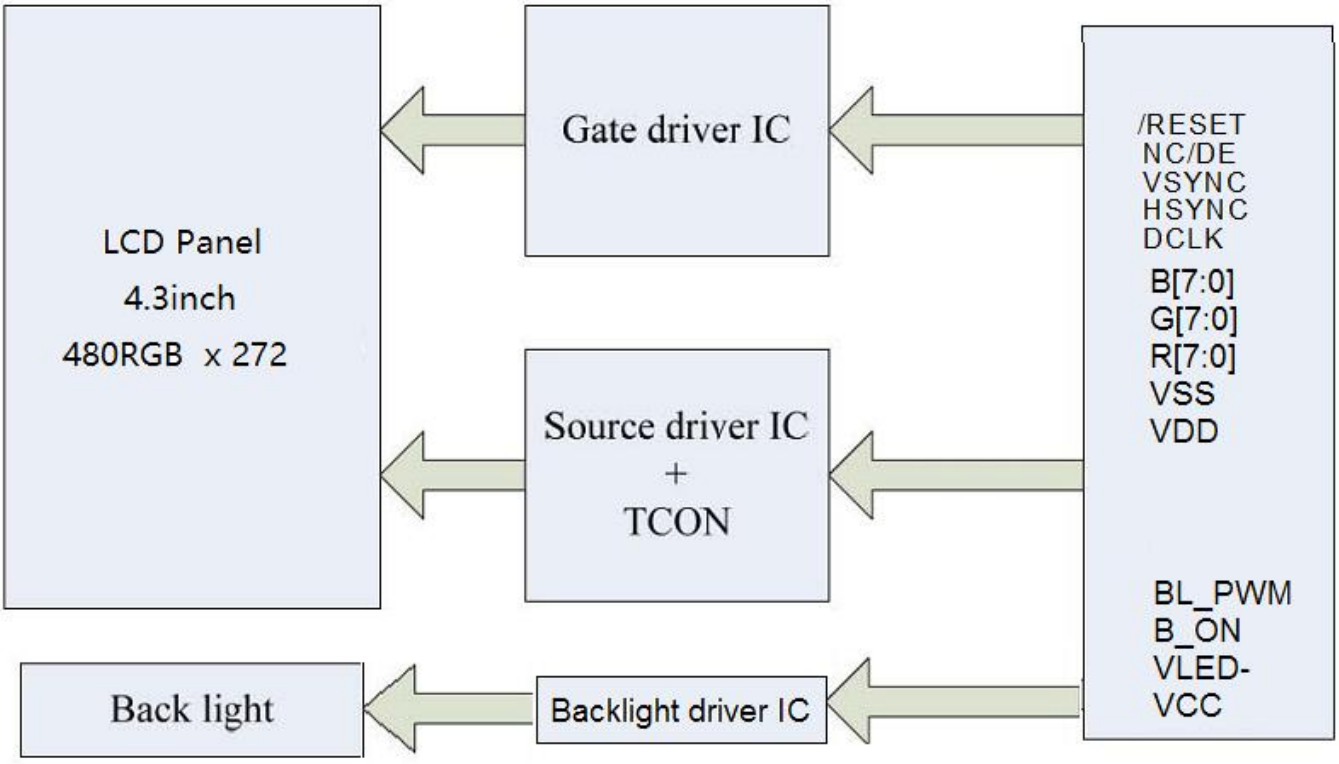
Note 1: Note: Default mode is SYNC-DE mode. According ST7282 IC full spec, it support SYNC-DE mode timing. But after confirm with Sitronix FAE, they back that if only SYNC mode signals, that without DE enable data signal, also ok. So, it supports both SYNC mode and DE mode.

Note 2: When input 18 bits RGB data, the two low bits of R,G and B data must be grounded.

Note 3: Data shall be latched at the rasing edge of DCLK.

Note 4: Global reset pin, low active. Suggest it connect with an RC reset circuit for stability. Normally pull high.

Block Diagram



- **TIMING CHARACTERISTICS**

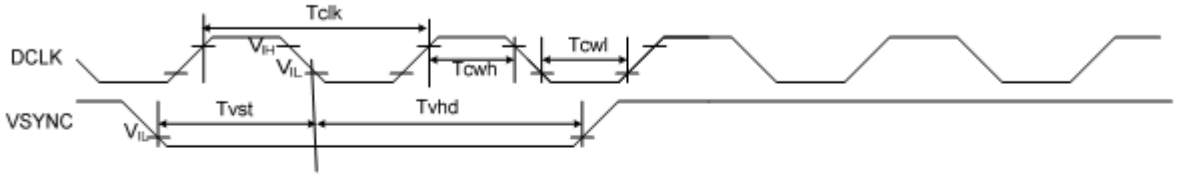
AC Characteristics

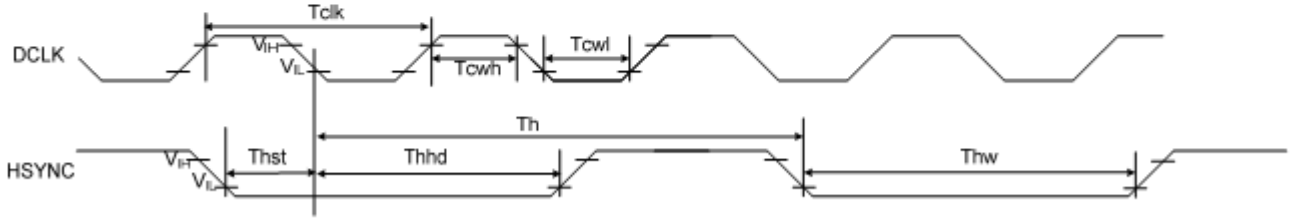
VDDI= 1.8V, VDD= 3.3V, AGND= 0V

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
System operation timing						
VDD power source slew time	TPOR	-	-	20	ms	From 0V to 99% VDD
GRB pulse width	tRSTW	10	50	-	us	R=10Kohm, C=1uF
Input/ Output timing						
CLK pulse duty	Tcw	40	50	60	%	
Hsync width	Thw	1	-	-	DCLK	
Hsync period	Th	55	60	65	us	
Vsync setup time	Tvst	12	-	-	ns	
Vsync hold time	Tvhd	12	-	-	ns	
Hsync setup time	Thst	12	-	-	ns	
Hsync hold time	Thhd	12	-	-	ns	
Data setup time	Tdsu	12	-	-	ns	
Data hold time	Tdhd	12	-	-	ns	
SD output stable time	Tst	-	-	12	us	Output settled within +20mV Loading = 6.8k+28.2pF.
GD output rise and fall time	Tgst	-	-	6	us	Output settled (5%~95%), Loading = 4.7k+29.8pF
3-wire serial communication						
Delay between CSB and Vsync	Tcv	1			us	
CS input setup time	Ts0	50			ns	
Serial data input setup time	Ts1	50			ns	
CS input hold time	Th0	50			ns	
Serial data input hold time	Th1	50			ns	
SCL pulse high width	Twh1	50			ns	
SCL pulse low width	Twl1	50			ns	
CS pulse high width	Tw2	400			ns	

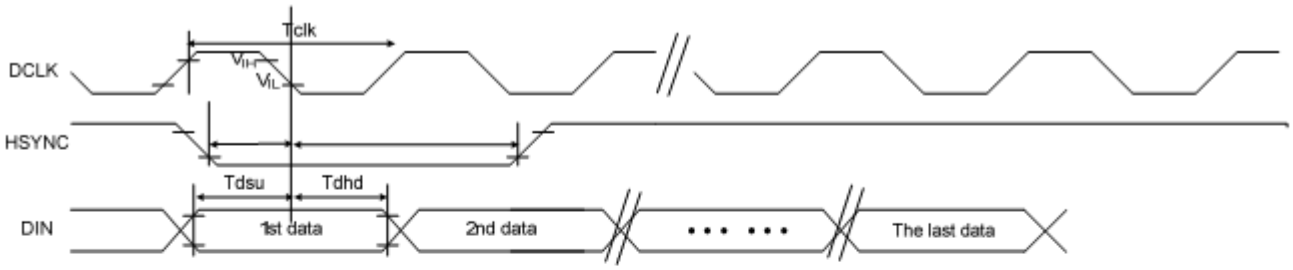
AC Timing Diagram

Clock and Data Input Timing Diagram

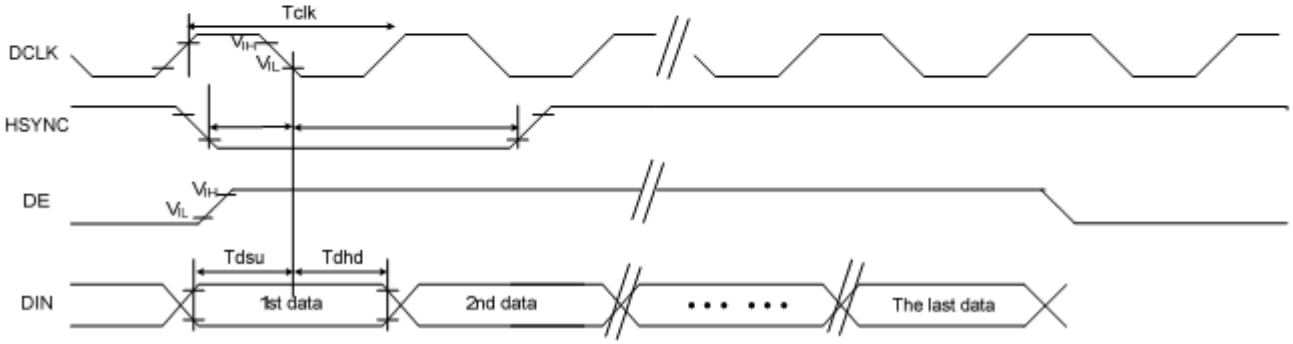




SYNC Mode



SYNC-DE Mode

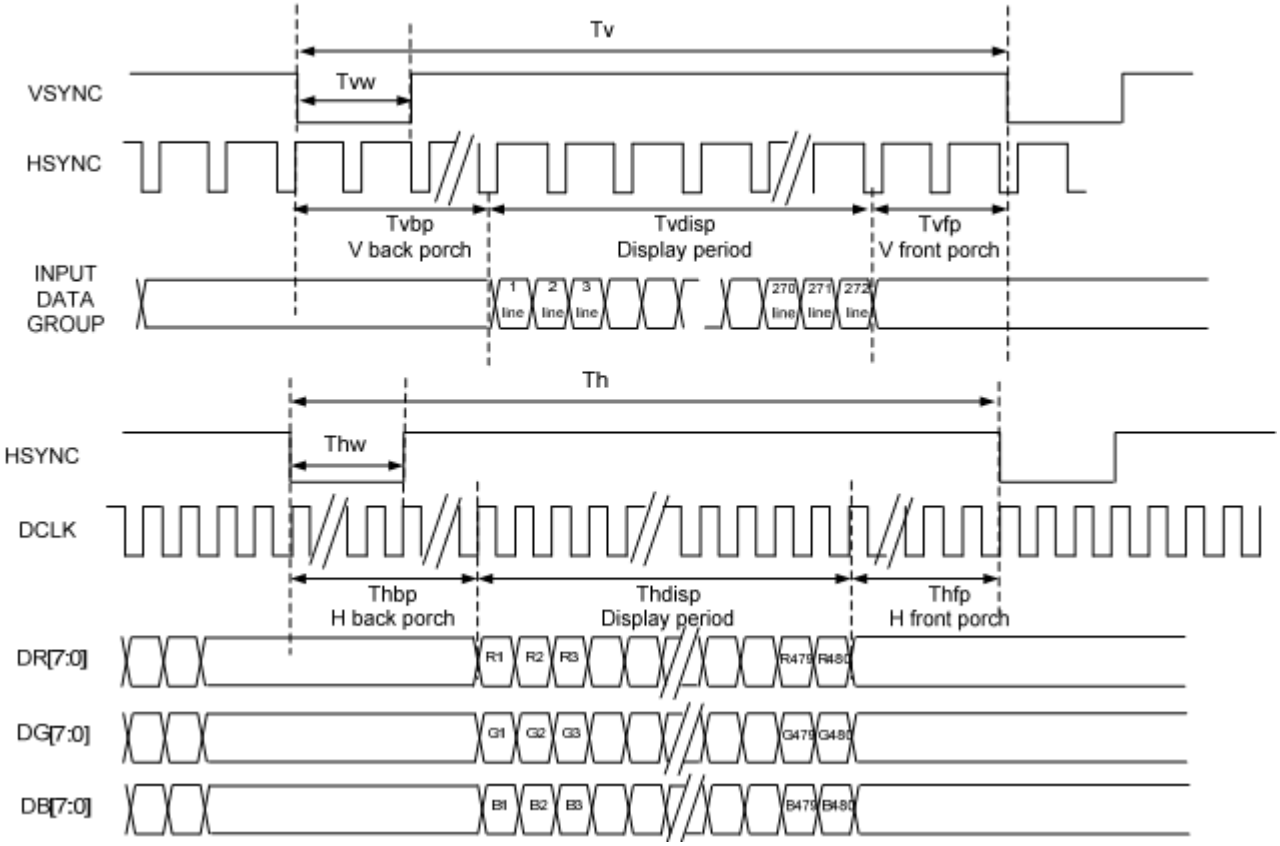


RGB Input Timing Table

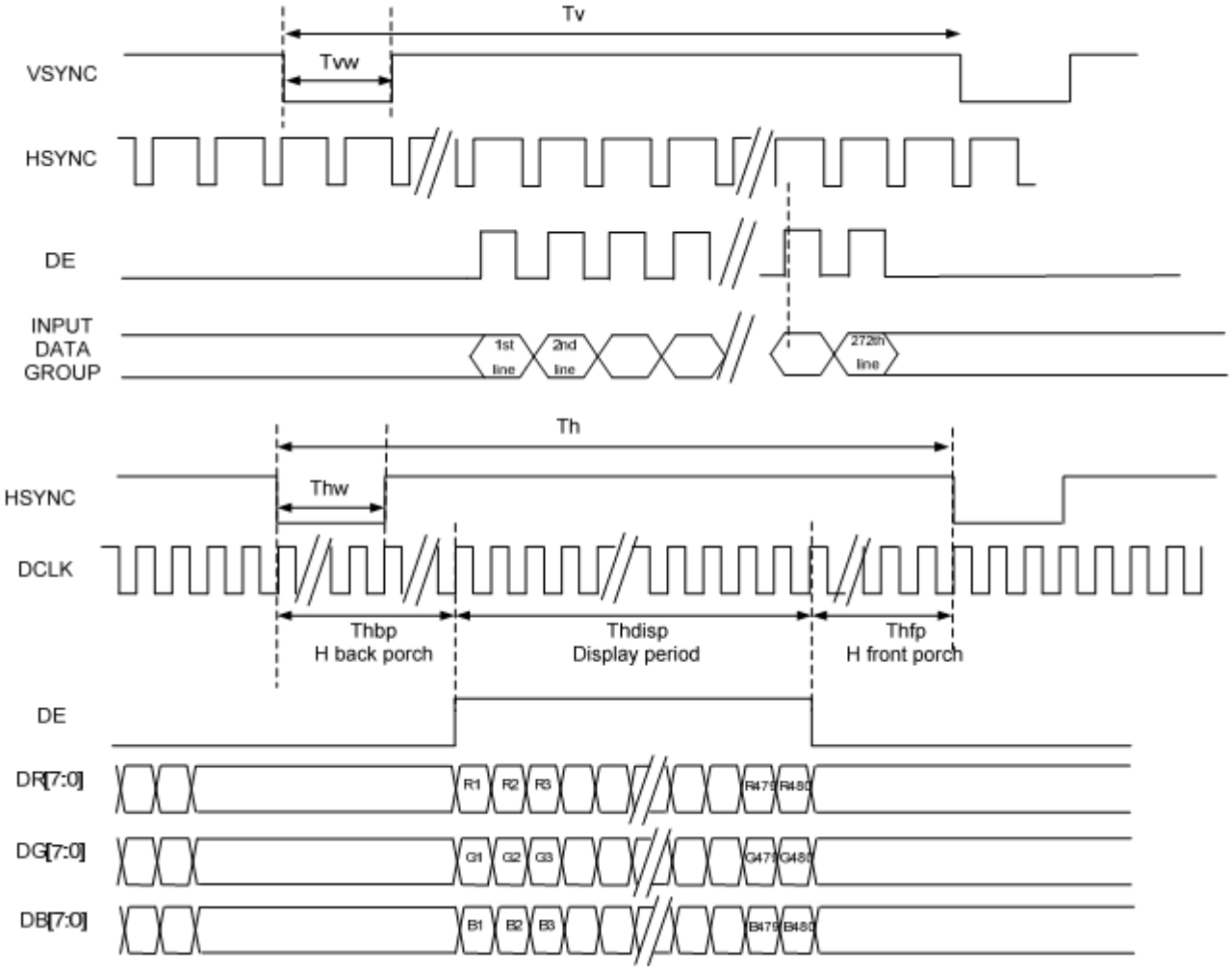
Parallel 24-bit RGB Timing Table

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK Frequency		Fclk	9	12	15	MHz	
DCLK Period		Tclk	67	83	111	ns	
HSYNC	Period Time	Th	486	526	533	DCLK	
	Display Period	Thdisp		480		DCLK	
	Back Porch	Thbp	3	43	50	DCLK	By H_Blanking setting
	Front Porch	Thfp	2	2	2	DCLK	
	Pulse Width	Thw	1	1	1	DCLK	
VSYNC	Period Time	Tv	276	286	304	H	
	Display Period	Tvdisp		272		H	
	Back Porch	Tvbp	2	12	30	H	By V_Blanking setting
	Front Porch	Tvfp	1	1	1	H	
	Pulse Width	Tvw	1	1	1	H	

SYNC Mode Timing Diagram

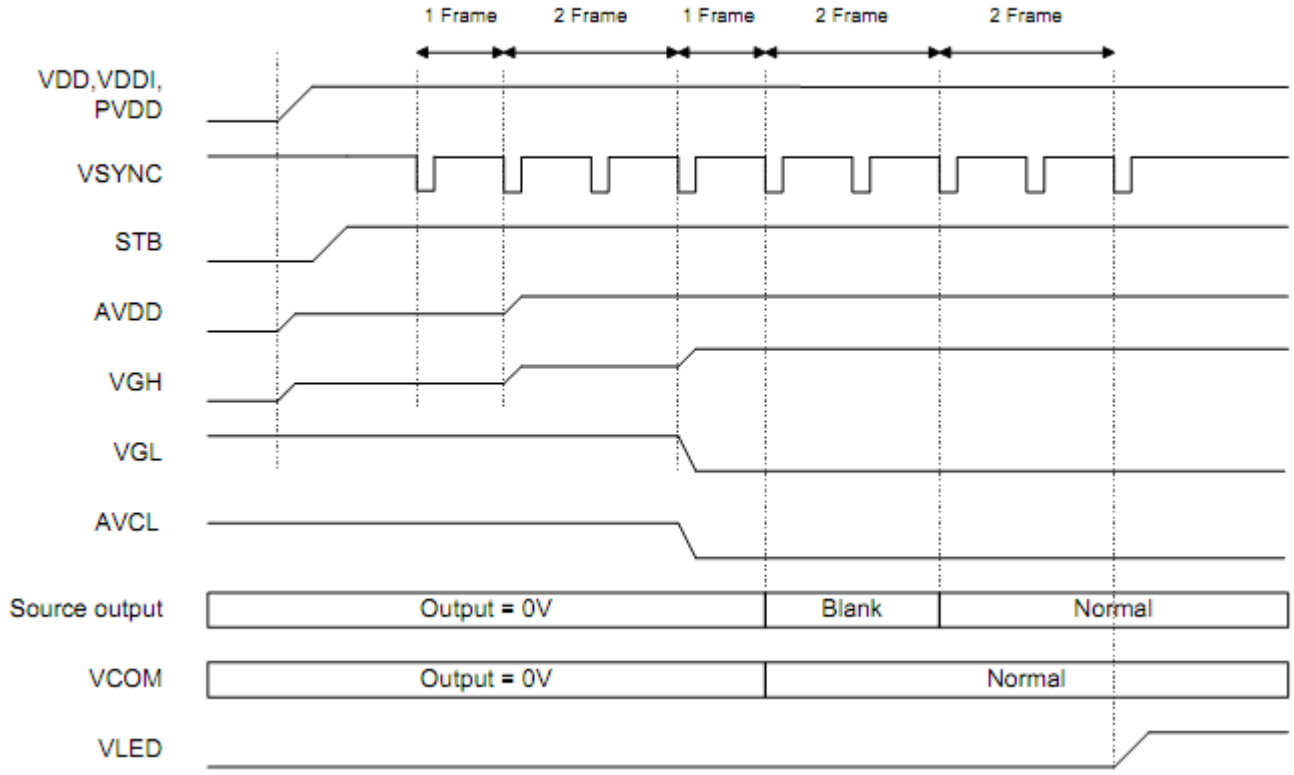


SYNC-DE Mode Timing Diagram



- **POWER ON/OFF SEQUENCE**

Power On Sequence



Power Off Sequence