FSC-BT671C

Bluetooth 5.2 & 10dBm maximum power output

Wireless MCU Module Datasheet

Version 1.2

Revision History

Version	Data	Notes	
1.0	2021/07/06	Initial Version	Marsh
1.1	2021/11/04	Modify Bluetooth Version: Upgrade from BT5.1 to BT5.2	Marsh
1.2	2022/02/23	Change storage temperature：-40°C to +105°C	LJC

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Contents

1. INTRODUCTION

Overview

The Bluetooth low energy chip used by FSC-BT671C includes a 32-bit 80 MHz ARM Cortex-M33 microcontroller, which can provide a maximum power output of 10 dBm. The chip's maximum receiving sensitivity is -97.5 (1 Mbit/s GFSK) dBm, and it supports a complete DSP instruction set and floating point unit, which can speed up calculations. Low-power gecko technology supports fast wake-up time and energy-saving mode. FSC-BT671C software and SDK support Bluetooth Low Energy (LE), Bluetooth 5.2 and Bluetooth mesh network. The module also supports the development of proprietary wireless protocols.

FSC-BT671C combines an energy-friendly MCU with a highly integrated radio transceiver. The module is suited for any battery operated application other systems requiring high performance and low energy consumption.

Features

- Bluetooth low energy (BLE) 5.2
- Integrate MCU to execute Bluetooth protocol stack.
- Postage stamp sized form
- Class 1 support (up to +10 dBm)
- The default UART Baud rate is 115.2Kbps and can support from 1200bps up to 230.4Kbps
- UART, I2C, SPI, 12-bit 1Msps SAR ADC
- Support the OTA upgrade
- Bluetooth stack profiles support: LE HID and all BLE protocols
- PWM

Application

- Lighting
- Connected Home
- Gateways and Digital Assistants
- Building Automation and Security

Module picture as below showing

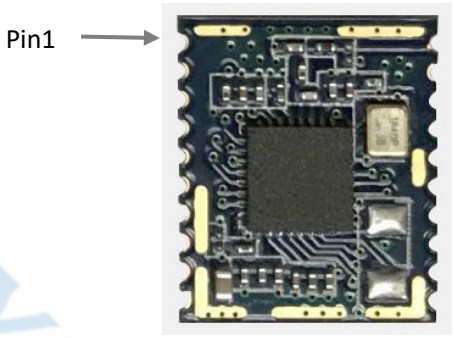


Figure 1: FSC-BT671C Picture

2. General Specification

Table 1: General Specifications

Categories	Features	Implementation
Wireless Specification	Chip model	SILICON LABS EFR32BG21
	Bluetooth Version	Bluetooth low energy (BLE) 5.2
	Frequency	2.4 - 2.4835 GHz
	Transmit Power	+10 dBm (Maximum)
	Receive Sensitivity	-97.5 dBm @ 1 Mbit/s GFSK -94.4 dBm @ 2 Mbit/s GFSK -104.9 dBm @ 125 kbps GFSK
	Modulation	GFSK
Host Interface and Peripherals	UART Interface	TX, RX, CTS, RTS
		General Purpose I/O
		Default 115200,N,8,1
		Baudrate support from 1200 to 230400bps
		5, 6, 7, 8 data bit character
	GPIO	15(maximum – configurable) lines
		O/P drive strength (4 mA)
		Pull-up resistor (40 KΩ) control
		Read pin-level
	I2C Interface	1 (configurable from GPIO total). Up to 400 kbps
	ADC Interface	Analog input voltage range: 0V ~ 3.3V
		Supports single 12-bit 1 Msps SAR ADC conversion
		8 channels (configured from GPIO total)
	PWM	3 General-Purpose Timer Modules
		Four General-Purpose Timer Modules (Two 16-Bit or One 32-Bit Timers, PWM Each)
Profiles	Classic Bluetooth	NA
	Bluetooth Low Energy	GATT Client & Peripheral - Any Custom Services
		BT5.2 Specifications
Maximum Connections	Classic Bluetooth	NA
	Bluetooth Low Energy	1 Clients
FW upgrade		Over the Air
		Xds
Supply Voltage	Supply	1.71V ~ 3.8V
Power Consumption		33.8 mA TX current @ 10 dBm output power at 2.4 GHz
		Standby Doze (Wait event): ~5mA
		50.9 µA/MHz in Active Mode
		4.5 µA DeepSleep current （16 kB RAM retention and RTC running from LFRCO)
Physical	Dimensions	10mm X 11.9mm X 1.8mm; Pad Pitch 1.1mm
Environmental	Operating	-40°C to +105°C

	Storage	-40°C to +105°C
Miscellaneous	Lead Free	Lead-free and RoHS compliant
	Warranty	One Year
Humidity		10% ~ 90% non-condensing
MSL grade:		MSL 3
ESD grade:	Human Body Model	All pins: ±2500V
	Charged device model	RF pins/ Non-RF pins: ±750V

3. HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

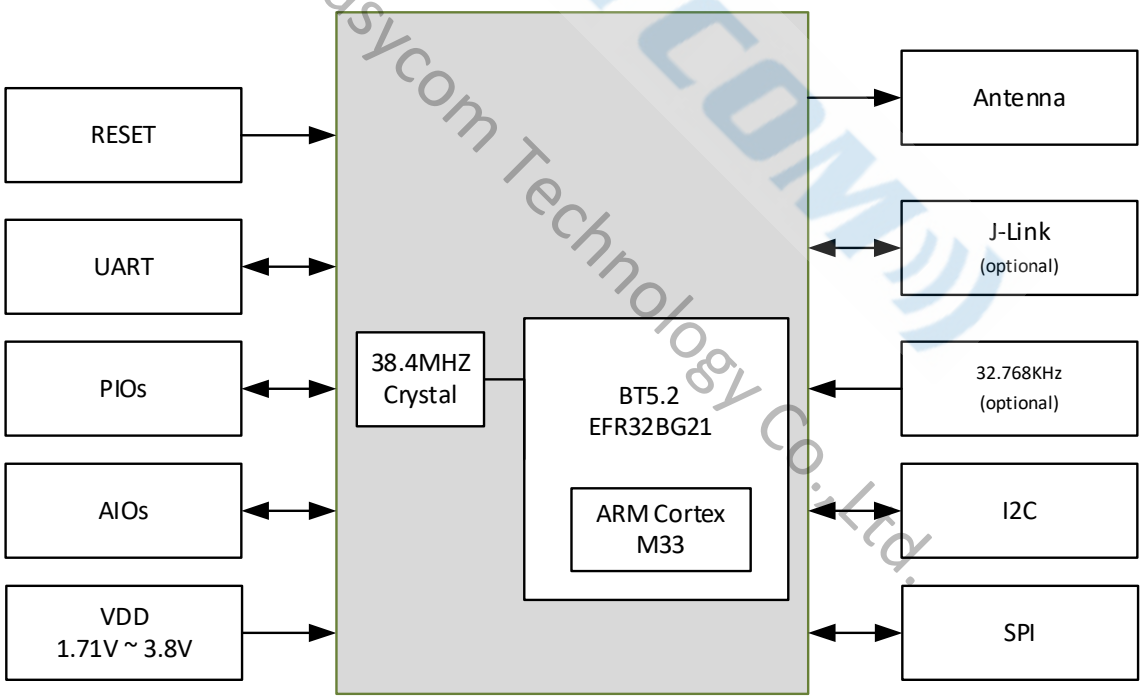


Figure 2: Block Diagram

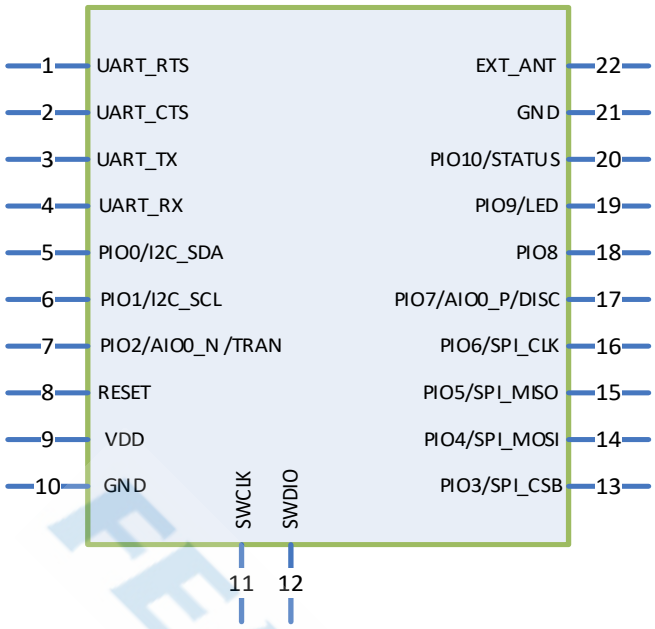


Figure 3: FSC-BT671C PIN Diagram (Top View)

3.2 PIN Definition Descriptions

Table 2: Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	UART_RTS	O	UART Request to Send (assert deassert)	Note 1，9
2	UART_CTS	I	UART Clear to Send (assert deassert)	Note 1，9
3	UART_TX	O	UART Data output	Note 1，9
4	UART_RX	I	UART Data input	Note 1，9
5	PIO0/I2C_SDA	I/O	Programmable input/output line *Alternative Function: I2C_SDA*	Note 2
6	PIO1/I2C_SCL	I/O	Programmable input/output line *Alternative Function: I2C_SCL*	Note 2
7	PIO2/AIO0_N/TRAN	I/O	Programmable input/output line Alternative Function 1: Analog to digital converter ADC0 external reference input negative pin. Alternative Function 2: Host MCU change UART transmission mode.	Note 3,5
8	RESET	I	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	
9	VDD	Vdd	Power supply voltage 3.3V	
10	GND	Vss	Power Ground	
11	SWCLK	I/O	Debugging through the clk line(Default) Alternative Function: Programmable input/output line	Note 1
12	SWDIO	I/O	Debugging through the data line(Default) Alternative Function: Programmable input/output line	Note 1

13	PIO3/SPI_CSB	I/O	Programmable input/output line Alternative Function: Chip select for SPI, active low	
14	PIO4/SPI_MOSI	I/O	Programmable input/output line Alternative Function: SPI data input	
15	PIO5/SPI_MISO	I/O	Programmable input/output line Alternative Function: SPI data out	
16	PIO6/SPI_CLK	I/O	Programmable input/output line Alternative Function: SPI clock	
17	PIO7/AIO0_P/DISC	I/O	Programmable input/output line Alternative Function 1: Analog to digital converter ADC0 external reference input positive pin. Alternative Function 2: Host MCU disconnect bluetooth.	Note 4,5
18	PIO8	I/O	Programmable input/output line	
19	PIO9/LED	I/O	Programmable input/output line Alternative Function: LED	Note 6
20	PIO10/STATUS	I/O	Programmable input/output line Alternative Function: BT Status	Note 7
21	GND	Vss	Power Ground	
22	EXT_ANT	O	RF signal output .	Note 8

Module Pin Notes:

Note 1	For customized module, this pin can be work as I/O Interface.
Note 2	I2C Serial Clock and Data. It is essential to remember that pull-up resistors on both SCL and SDA lines are not provided in the module and MUST be provided external to the module.
Note 3	When bluetooth connection established, UART transmission mode will be determined by PIO2's level : High: Command Mode ; Low: Throughput Mode
Note 4	When bluetooth connection established, a rising edge of PIO7 will cause disconnection with remote device.
Note 5	The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.
Note 6	LED(Default)-- Power On: Light Slow Shinning ; Connected: Steady Lighting.
Note 7	BT Status(Default)-- Disconnected: Low Level; Connected: High Level.
Note 8	This PIN can connect to an external antenna to improve the Bluetooth signal coverage.
Note 9	GPIO with 3.3V tolerance are indicated by (3.3V).

4. PHYSICAL INTERFACE

4.1 Power Supply

The transient response of the regulator is important. If the power rails of the module are supplied from an external voltage source, the transient response of any regulator used should be 20μs or less. It is essential that the power rail recovers quickly.

*** Please supply the module with a current supply greater than 200mA.

4.2 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I2S

4.3 Reset

A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

The module needs to add an external RC reset circuit.

4.4 General Purpose Analog IO

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples.

The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

4.5 General Purpose Digital IO

This module has up to 16 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

4.6 RF Interface

The Bluetooth module without antenna, you need an external antenna to achieve the best wireless performance, expanded wireless coverage.

- The user can connect a 50 ohm antenna directly to the RF port
- 2400–2483.5 MHz
- TX output power of +10dBm (Maximum)
- Receiver to achieve maximum sensitivity -97.5dBm @ 1 Mbps GFSK

4.7 Serial Interfaces

4.7.1 UART

FSC-BT671C provides one channels of Universal Asynchronous Receiver/Transmitters(UART)(Full-duplex asynchronous communications). The UART Controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART Controller channel supports ten types of interrupts.

This is a standard UART interface for communicating with other serial devices. The UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

When the module is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.

This module output is at 3.3V CMOS logic levels (tracks VCC). Level conversion must be added to interface with an RS-232 level compliant interface.

Some serial implementations link CTS and RTS to remove the need for handshaking. We do not recommend linking CTS and RTS except for testing and prototyping. If these pins are linked and the host sends data when the FSC-BT671C deasserts its RTS signal, there is significant risk that internal receive buffers will overflow, which could lead to an internal processor crash. This drops the connection and may require a power cycle to reset the module. We recommend that you adhere to the correct CTS/RTS handshaking protocol for proper operation.

Table 3: Possible UART Settings

Parameter	Possible Values	
Baudrate	Minimum	1200 baud (≤2%Error)
	Standard	115200bps(≤1%Error)
	Maximum	230400bps(≤1%Error)
Flow control		RTS/CTS, or None
Parity		None, Odd or Even
Number of stop bits		1 /1.5/2
Bits per channel		5/6/7/8

When connecting the module to a host, please make sure to follow .

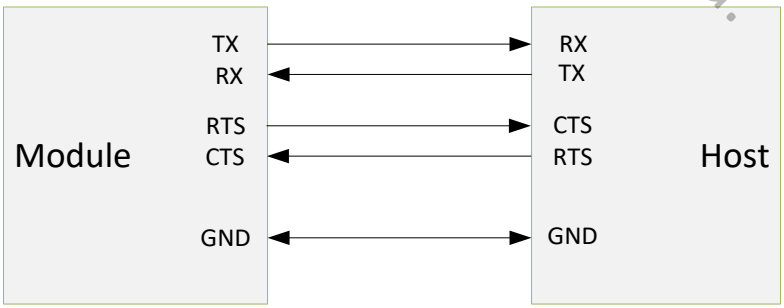


Figure 4: UART Connection

4.7.2 I²C Interface

- Up to two I²C bus interfaces can support both master and slave mode with a frequency up to 1000KHZ.

The I2C module provides an interface between the MCU and a serial I2C bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I2C module allows precise timing control of the transmission process and highly automated transfers.
Automatic recognition of slave addresses is provided in active and low energy modes.

4.8 Counters/Timers and PWM

4.8.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER_0 only.

4.8.2 Wide Timer/Counter (WTIMER)

WTIMER peripherals function just as TIMER peripherals, but are 32 bits wide. They keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each WTIMER is a 32-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the WTIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit WTIMER_0 only.

4.8.3 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LFXO), the 32.768 kHz RC oscillator (LFRCO), or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.

5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Absolute maximum ratings for supply voltage and voltages on digital and analogue pins of the module are listed below. Exceeding these values causes permanent damage.

The average PIO pin output current is defined as the average current value flowing through any one of the corresponding pins for a 100mS period. The total average PIO pin output current is defined as the average current value flowing through all of the corresponding pins for a 100mS period. The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

Table 4: Absolute Maximum Rating

Parameter	Min	Max	Unit
Storage temperature range	-40	105	°C
Voltage on any supply pin	-0.3	3.8	V
Voltage ramp rate on any supply pin		1	V / μs
DC voltage on any GPIO pin	-0.3	VDD + 0.3	V
Voltage on HFXO pins	-0.3	1.2	V
Total current into VDD power lines - Source		200	mA
Total current into VSS ground lines - Sink		200	mA

5.2 Recommended Operating Conditions

Table 5: Recommended Operating Conditions

Parameter	Min	Type	Max	Unit
Operating ambient temperature range	-40	25	+105	°C
VREGVDD operating supply voltage	1.71	3.3	3.8	V
VREGVDD current DCDC in bypass, T ≤105 °C			200	mA

5.3 General-Purpose I/O (GPIO)

Table 6: General-Purpose I/O (GPIO)

Parameter	Min	Type	Max	Unit
V_{IL} - Input low voltage			VDD*0.3	V
V_{IH} - Input high voltage	VDD*0.7			V
V_{OH} - Sourcing 20 mA, VDD = 3.0 V	VDD*0.8			V
Sourcing 8 mA, VDD = 1.62 V	VDD*0.6			V
V_{OL} - Sourcing 20 mA, IOVDD = 3.0 V			VDD*0.2	V
Sourcing 8 mA, IOVDD = 1.62V			VDD*0.4	V
I_{IOLEAK} – MODEx = DISABLED, VDD = 1.71V		1.9		nA
MODEx = DISABLED, VDD = 3.0V		2.5		nA

	MODEx = DISABLED, VDD = 3.8V			200	nA
R_{PULL} -	I/O pin pull-up/pull-down resistor	35	44	55	KΩ

5.4 Analog Characteristics

Table 7: Specifications of 12-bit SARADC

Unless otherwise indicated, typical conditions are: ADCCLK=10 MHz, OSR=2

Parameter		Min	Type	Max	Unit
$V_{RESOLUTION}$ -	Resolution		12		Bits
V_{ADCIN} -	Input voltage range				
	Single ended			VFS	V
	Differential	-VFS/2		VFS/2	V
$V_{ADCREFIN\_P}$ -	Input range of external reference voltage, single ended and differential	1		VDD	V
$PSRR_{ADC}$ -	Power supply rejection (At DC)		80.4		dB
$CMRR_{ADC}$ -	Analog input common mode rejection ratio (At DC)		87		dB
f_{ADCCLK} -	ADC clock frequency			10	MHz
$f_{ADCRATE}$ -	Throughput rate			1	Msps
$SNDR_{ADC}$ -	Differential Input. Gain=1x,fIN = 10kHz, Internal VREF=1.21V	65	69.1		dB
	Differential Input. Gain=2x, fIN = 10 kHz, Internal VREF=1.21V		68.8		dB
	Differential Input. Gain=4x, fIN = 10 kHz, Internal VREF=1.21V		66.9		dB
	Differential Input. Gain=0.5x, fIN = 10 kHz, InternalVREF=1.21V		69.2		dB
$SFDR_{ADC}$ -	Differential Input. Gain=1x, fIN = 10 kHz, Internal VREF=1.21V	72	86.5		dB
DNL_{ADC} -	Differential non-linearity(DNL) 12 bit resolution, No missing codes	-1		1.5	LSB
INL_{ADC} -	Integral non-linearity (INL),End point method 12 bit resolution	-2.5		2.5	LSB
$V_{ADCOFFSETERR}$ -	GAIN = 1 and 0.5, Differential Input	-3	0	3	LSB
$V_{ADCGAIN}$ -	GAIN=1 and 0.5, using external VREF, direct mode.	-0.3	0.069	0.3	%
	GAIN=2, using external VREF, direct mode.	-0.4	0.151	0.4	%
	GAIN=3, using external VREF, direct mode.	-0.7	0.186	0.7	%
	GAIN=4, using external VREF, direct	-1.1	0.227	1.1	%
	Internal VREF, Gain=1mode.		0.023		%
V_{TS_SLOPE} -	Temperature sensor slope		-1.84		mV/°C

5.5 I2C

Table 8: I2C Standard-mode (Sm)

Parameter	Min	Type	Max	Unit

f_{SCL} -	SCL clock frequency	0	100	KHz
t_{LOW} -	SCL clock low time	4.7		us
t_{HIGH} -	SCL clock high time	4		us
t_{SU_DAT} -	SDA set-up time	250		ns
t_{HD_DAT} -	SDA hold time	0	0	ns
t_{SU_STA} -	Repeated START condition set-up time	4.7		us
t_{HD_STA} -	(Repeated) START condition hold time	4		us
t_{SU_STO} -	STOP condition set-up time	4		us
t_{BUF} -	Bus free time between a STOP and START condition	4.7		us

Table 9: I2C Fast-mode (Fm)

Parameter		Min	Type	Max	Unit
f_{SCL} -	SCL clock frequency	0		400	KHz
t_{LOW} -	SCL clock low time	1.3			us
t_{HIGH} -	SCL clock high time	0.6			us
t_{SU_DAT} -	SDA set-up time	100			ns
t_{HD_DAT} -	SDA hold time	0			ns
t_{SU_STA} -	Repeated START condition set-up time	0.6			us
t_{HD_STA} -	(Repeated) START condition hold time	0.6			us
t_{SU_STO} -	STOP condition set-up time	0.6			us
t_{BUF} -	Bus free time between a STOP and START condition	1.3			us

Table 10: I2C Fast-mode Plus (Fm+)

Parameter		Min	Type	Max	Unit
f_{SCL} -	SCL clock frequency	0		1000	KHz
t_{LOW} -	SCL clock low time	0.5			us
t_{HIGH} -	SCL clock high time	0.26			us
t_{SU_DAT} -	SDA set-up time	50			ns
t_{HD_DAT} -	SDA hold time	100			ns
t_{SU_STA} -	Repeated START condition set-up time	0.26			us
t_{HD_STA} -	(Repeated) START condition hold time	0.26			us
t_{SU_STO} -	STOP condition set-up time	0.26			us
t_{BUF} -	Bus free time between a STOP and START condition	0.5			us

5.6 SPI

Table 11: SPI Master Timing

Parameter	Min	Type	Max	Unit
t_{SCLK} - SCLK period[1 3 2]	2 * $t_{HFPERCLK}$			ns
t_{CS_MO} - CS to MOSI[1 3]	-18.5		22.5	ns
t_{SCLK_MO} - SCLK to MOSI[1 3]	-13		11	ns
t_{SU_MI} - MISO setup time[1 3]	34			ns
t_{H_MI} - MISO hold time[1 3]	-8.5			ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1
2. tHFPERCLK is one period of the selected HFPERCLK.
3. Measurement done with 8 pF output loading at 10% and 90% of VDD (figure shows 50% of VDD).

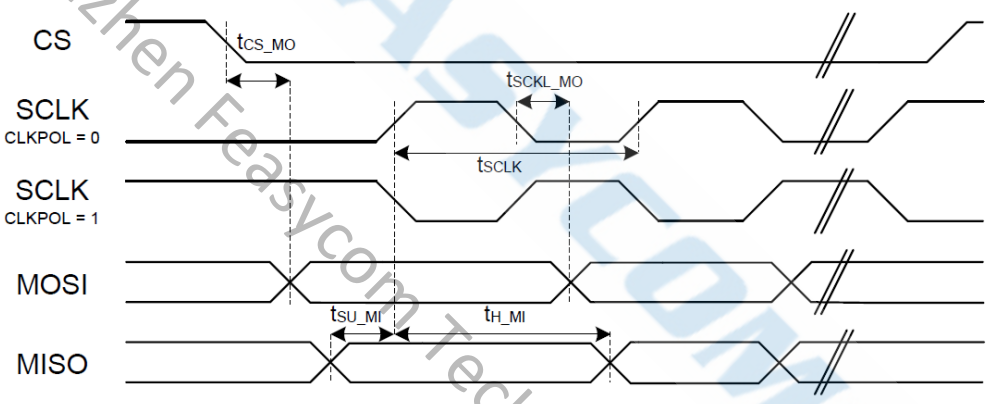


Figure 5: SPI Master Timing Diagram

Table 12: SPI Slave Timing

Parameter	Min	Type	Max	Unit
t_{SCLK} - SCLK period[1 3 2]	6 * $t_{HFPERCLK}$			ns
t_{SCLK_HI} - SCLK high time[1 3 2]	2.5 * $t_{HFPERCLK}$		14	ns
t_{SCLK_LO} - SCLK low time[1 3 2]	2.5 * $t_{HFPERCLK}$		10.5	ns
$t_{CS\_ACT\_MI}$ - CS active to MISO [1 3]	16		52.5	
$t_{CS\_DIS\_MI}$ - CS disable to MISO [1 3]	15		46	
t_{SU_MO} - MOSI setup time [1 3]	3.5			
t_{H_MO} - MOSI hold time [1 3 2]	4.5			
t_{SCLK_MI} - SCLK to MISO [1 3 2]	13.5 + 1.5 * $t_{HFPERCLK}$		31 + 2.5 * $t_{HFPERCLK}$	

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.
3. Measurement done with 8 pF output loading at 10% and 90% of VDD (figure shows 50% of VDD).

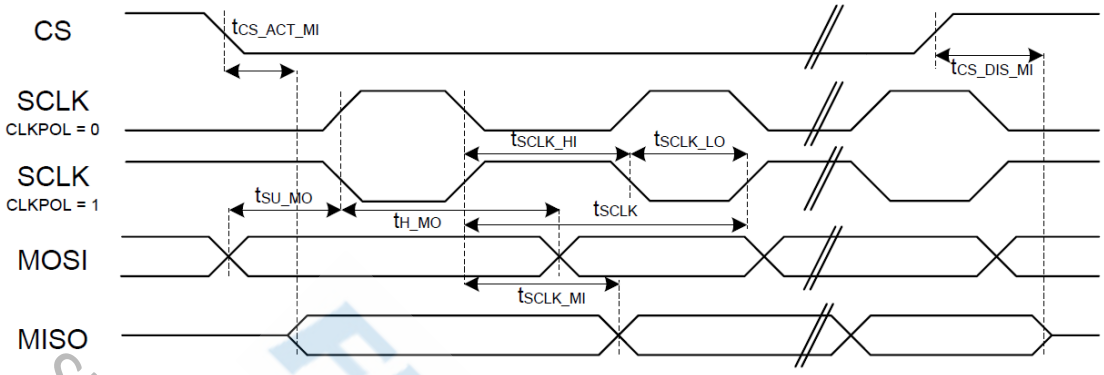


Figure 6: SPI Slave Timing Diagram

5.7 Power consumptions

Table 13: Power consumptions VDD=3.3V , T = 25°C

Parameter	Test Conditions	Type	Max.	Unit
Current consumption in EM0 mode with all peripherals disabled	38.4 MHz crystal, CPU running while loop from flash	128		uA/MHz
Current consumption in EM1 mode with all peripherals disabled	38.4 MHz crystal	76		uA/MHz
Current consumption in EM2 mode, with voltage scaling enabled	Full 64 kB RAM retention and RTCC running from LFXO	1.9		uA
	Full 64 kB RAM retention and RTCC running from LFRCO	2.2		uA
Current consumption in EM3 mode, with voltage scaling enabled	Full 64 kB RAM retention and CRYOTIMER running from ULFRCO	1.53	3.0	uA
Current consumption in EM4H mode, with voltage scaling enabled	128 byte RAM retention, RTCC running from LFXO	0.93		uA
	128 byte RAM retention, CRYOTIMER running from ULFRCO	0.45		uA
	128 byte RAM retention, no RTCC	0.44	0.9	uA
Current consumption in EM4S mode	No RAM retention, no RTCC	0.04	0.085	uA

Table 14: BLE MODE Consumption Report(TBD) VDD=3.3V , T = 25°C

Parameter	Test Conditions	Unit

Beacon TX Power	0	10	dBm
sleep mode	1.75	1.75	uA
100ms interval	462	1040	uA
200ms interval	255.34	548.49	uA
500ms interval	100	222.12	uA
800ms interval	75.45	176.81	uA
1000ms interval	59.71	139	uA

5.8 Thermal Characteristics

Table 15: Thermal Characteristics

Parameter	Test Conditions	Type	Unit
Thermal Resistance Junction to Ambient	2-Layer PCB, Natural Convection	94.3	°C /W
QFN32 (4x4mm) Package	4-Layer PCB, Natural Convection	35.4	°C /W
Thermal Resistance Junction to Case	2-Layer PCB, Natural Convection	36.3	°C /W
QFN32 (4x4mm) Package	4-Layer PCB, Natural Convection	23.5	°C /W
Note: 1. Measured according to JEDEC standard JESD51-2A. Integrated Circuit Thermal Test Method Environmental Conditions – Natural Convection (Still Air).			

6. MSL & ESD

Table 16: MSL and ESD

Parameter	Test Conditions		Value
MSL grade:	MSL 3(1)		
ESD grade:	Human body model (HBM), per ANSI/ESDA/JEDEC JS001(2)	All pins	±2500V
	Charged device model (CDM), per JESD22-C101(3)	RF pins	±750V
		Non-RF pins	±750V

(1)The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7. RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the Picture below and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the

Picture below, the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Table 17: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

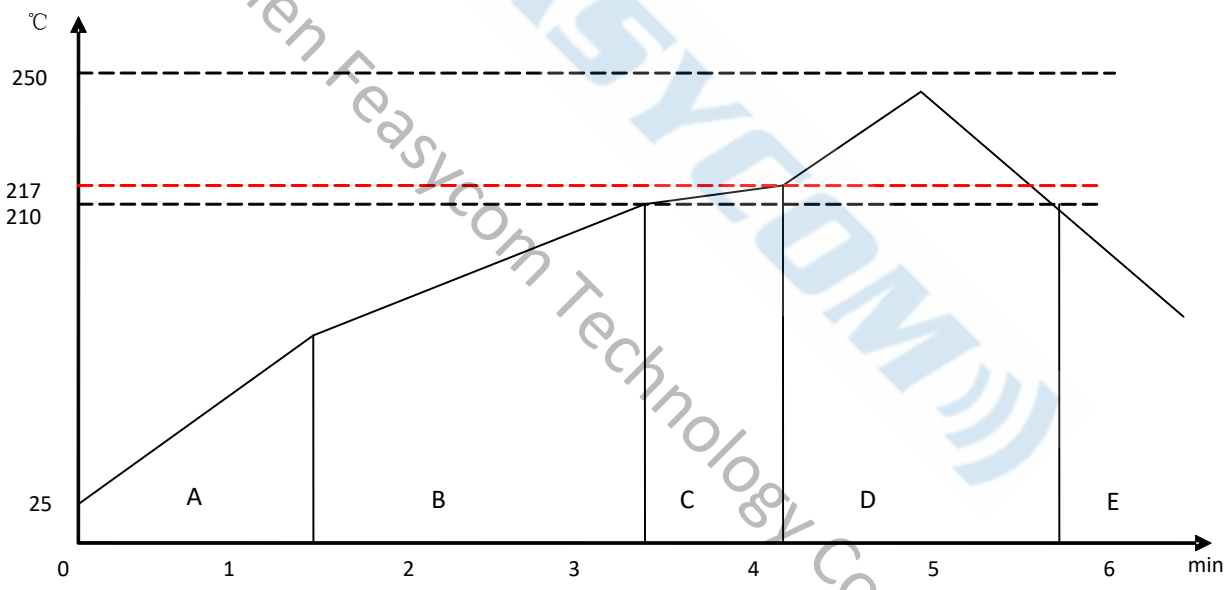


Figure 7: Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the

temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

8. MECHANICAL DETAILS

8.1 Mechanical Details

- Dimension: 10mm(W) x 11.9mm(L) x 1.8mm(H) Tolerance: ±0.1mm
- Module size: 10mm X 11.9mm Tolerance: ±0.1mm
- Pad size: 0.9mmX0.6mm Tolerance: ±0.1mm
- Pad pitch: 1.1mm Tolerance: ±0.1mm

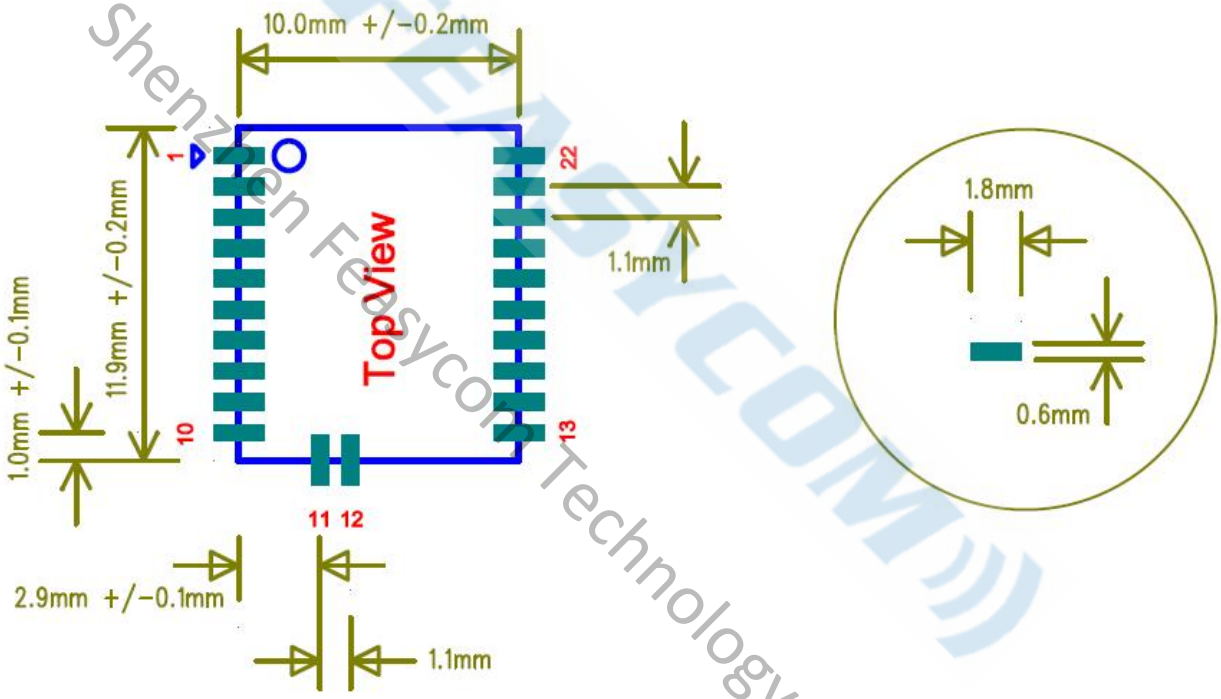


Figure 8: FSC-BT671C footprint

9. HARDWARE INTEGRATION SUGGESTIONS

9.1 Soldering Recommendations

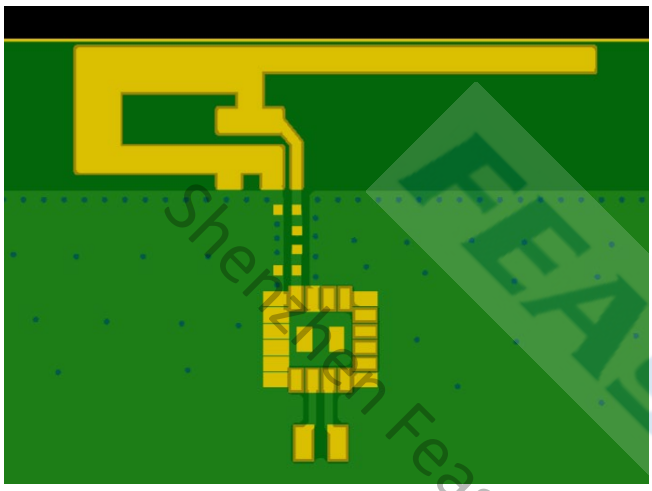
FSC-BT671C is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

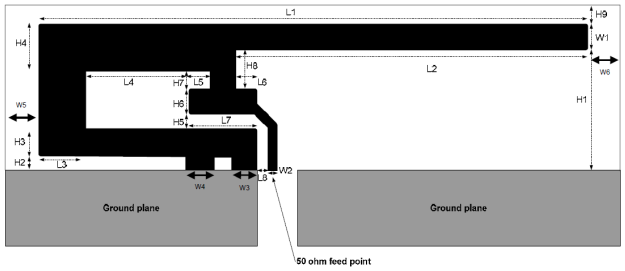
Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

9.2 Layout Guidelines(Internal Antenna)

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.





H1	5.70 mm	W2	0.46 mm	W4	1.20 mm
H2	0.74 mm	L1	25.58 mm	W5	5.00 mm
H3	1.29 mm	L2	16.40 mm	W6	5.00 mm
H4	2.21 mm	L3	2.18 mm		
H5	0.66 mm	L4	4.80 mm		
H6	1.21 mm	L5	1.00 mm		
H7	0.80 mm	L6	1.00 mm		
H8	1.80 mm	L7	3.20 mm		
H9	0.61 mm	L8	0.45 mm		
W1	1.21 mm	W3	1.00 mm		

Figure 9: FSC-BT671C Restricted Area

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

9.3 Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in picture below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

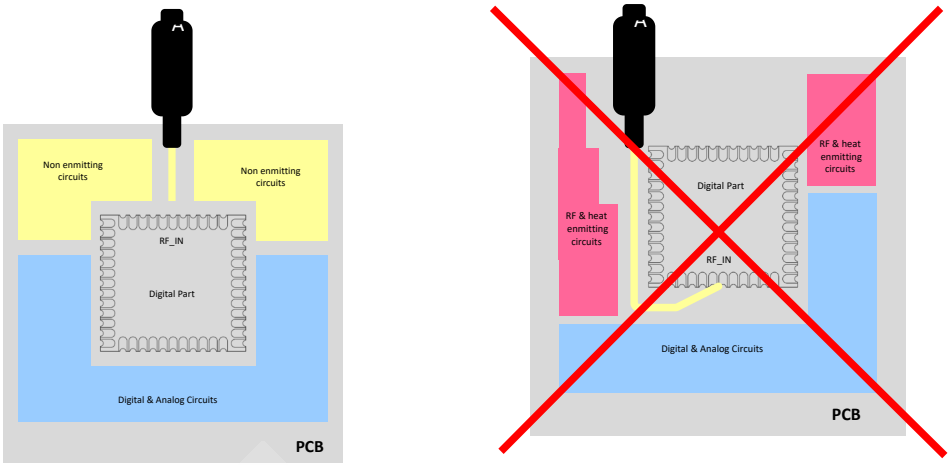


Figure 10: Placement the Module on a System Board

9.3.1 Antenna Connection and Grounding Plane Design

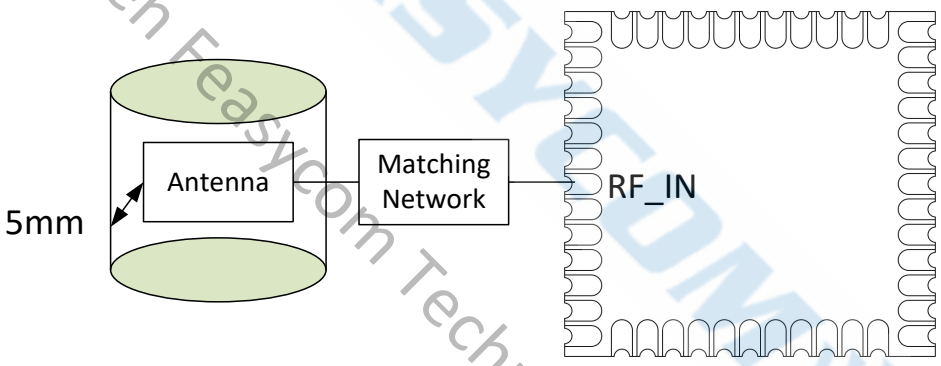


Figure 11: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

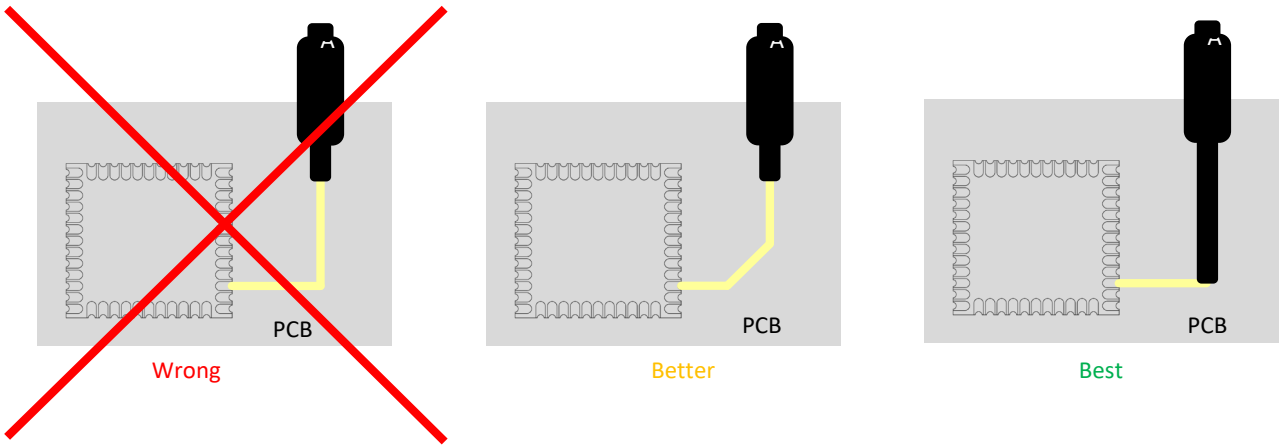


Figure 12: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

10. PRODUCT PACKAGING INFORMATION

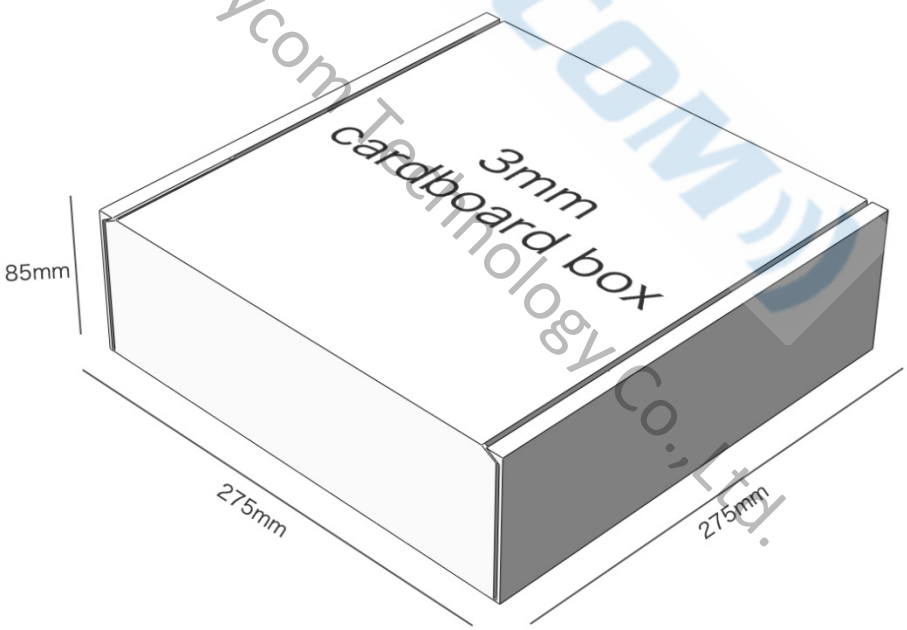
10.1 Default Packing

a, Tray vacuum

b, Tray Dimension: 180mm * 195mm

Figure 13: Tray vacuum

10.2 Packing box(Optional)



* If require any other packing, must be confirmed with customer

* Package: 1000PCS Per Carton (Min Carton Package)

Figure 14: Packing Box

11. APPLICATION SCHEMATIC