OLED DISPLAY SPECIFICATION

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REX012864U

General Specification

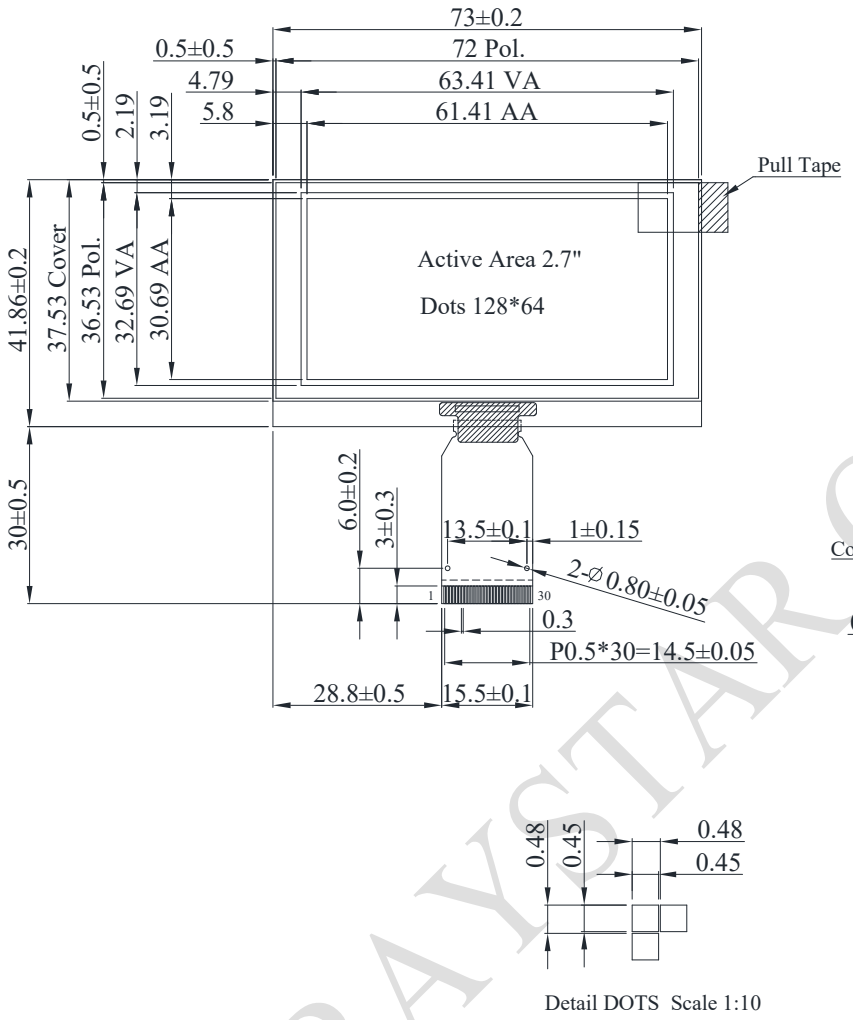
- Dot Matrix: 128 x 64
- Module dimension: 73.0 x 41.86 x 2.01 mm
- Active Area: 61.41 x 30.69 mm
- Pixel Size: 0.45 x 0.45 mm
- Pixel Pitch: 0.48 x 0.48 mm
- Display Mode: Passive Matrix
- Display Color: Monochrome
- Drive Duty: 1/64 Duty
- Gray Scale: 4 bits
- Interface: 8-bits 6800 and 8080 parallel, 4-line SPI, I2C
- IC: SSD1357
- Size: 2.7 inch

Interface Pin Function

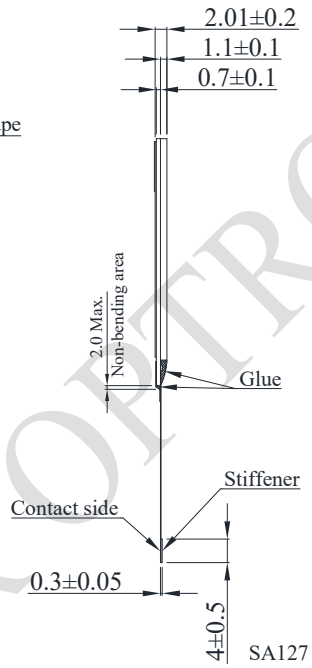
<table>
<tr><th>No.</th><th>Symbol</th><th>Function</th></tr>
<tr><td>1</td><td>NC(GND)</td><td>No connection.</td></tr>
<tr><td>2</td><td>VSS</td><td>Ground pin. It must be connected to external ground.</td></tr>
<tr><td>3</td><td>VCC</td><td>Power supply for panel driving voltage. This is also the most positive power voltage supply pin.
A capacitor should be connected between this pin and VSS.</td></tr>
<tr><td>4</td><td>VCOMH</td><td>COM signal deselected voltage level.
A capacitor should be connected between this pin and VSS.</td></tr>
<tr><td>5</td><td>VLSS</td><td>Analog system ground pin. It must be connected to external ground.</td></tr>
<tr><td>6~13</td><td>D7~D0</td><td>These pins are bi-directional data bus connecting to the MCU data bus. Unused pins are recommended to tie LOW.
When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SDIN and D2 should be kept NC.
When I2C mode is selected, D2, D1 should be tied together and serve as SDAout, SDAin in application and D0 is the serial clock input, SCL.</td></tr>
<tr><td>14</td><td>E/RD#</td><td>This pin is MCU interface input.
When 6800 interface mode is selected, this pin will be used as the Enable (E) signal.
Read/write operation is initiated when this pin is pulled HIGH and the chip is selected.
When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected.
When serial or I2C interface is selected, this pin must be connected to VSS.</td></tr>
<tr><td>15</td><td>R/W#</td><td>This pin is read / write control input pin connecting to the MCU interface.
When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW.
When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected.
When serial or I2C interface is selected, this pin must be connected to VSS.</td></tr>
<tr><td>16
17</td><td>BS1
BS2</td><td>Communicating Protocol Select.
These pins are MCU interface selection input. See the following table:
<table>
<tr><th></th><th>BS1</th><th>BS2</th></tr>
<tr><td>I2C</td><td>1</td><td>0</td></tr>
<tr><td>4-wire Serial</td><td>0</td><td>0</td></tr>
<tr><td>8-bit 8080 Parallel</td><td>1</td><td>1</td></tr>
<tr><td>8-bit 6800 Parallel</td><td>0</td><td>1</td></tr>
</table>
</td></tr>
</table>

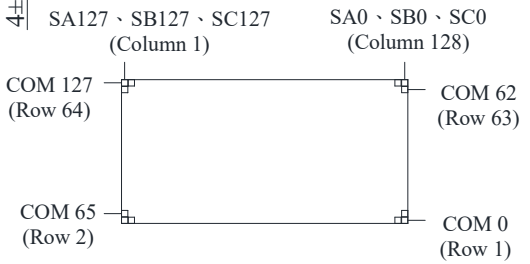
18	D/C#	This pin is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data at D[7:0] will be interpreted as data. When the pin is pulled LOW, the data at D[7:0] will be transferred to a command register. In I2C mode, this pin acts as SA0 for slave address selection.
19	CS#	This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW (active LOW).
20	RES#	This pin is reset signal input. When the pin is pulled LOW, initialization of the chip is executed. Keep this pin pull HIGH during normal operation.
21	FR	This pin outputs RAM write synchronization signal. Proper timing between MCU data writing and frame display timing can be achieved to prevent tearing effect. It should be kept NC if it is not used.
22	IREF	This pin is the segment output current reference pin. IREF is supplied externally.
23	N.C.	Reserved Pin The N.C. pin between function pins is reserved for compatible and flexible design.
24	VDD	Power supply pin for core logic operation. A capacitor should be connected between this pin and VSS.
25	VP	This pin is the segment pre-charge voltage reference pin. A capacitor can be connected between this pin and VSS to improve vision performance. No external power supply is allowed to connect to this pin.
26	VDD	Power supply pin for core logic operation. A capacitor should be connected between this pin and VSS.
27	VSL	This is segment voltage (output low level) reference pin. This pin has to connect with resistor and diode to ground.
28	VLSS	Analog system ground pin. It must be connected to external ground.
29	VCC	Power supply for panel driving voltage. This is also the most positive power voltage supply pin. A capacitor should be connected between this pin and VSS.
30	NC(GND)	No connection

Contour Drawing



Detail DOTS Scale 1:10





PIN NO.	SYMBOL
1	NC(GND)
2	VSS
3	VCC
4	VCOMH
5	VLSS
6	D7
7	D6
8	D5
9	D4
10	D3
11	D2
12	D1
13	D0
14	E/RD#
15	R/W#
16	BS1
17	BS2
18	DC#
19	CS#
20	RES#
21	FR
22	IREF
23	NC
24	VDD
25	VP
26	VDD
27	VSL
28	VLSS
29	VCC
30	NC(GND)

The non-specified tolerance of dimension is ± 0.3mm.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage for Logic	VDD	-0.3	4.0	V
Supply Voltage for Display	VCC	0	19.0	V
Operating Temperature	TOP	-40	+80	°C
Storage Temperature	TSTG	-40	+85	°C

Electrical Characteristics

DC Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage for Logic	VDD	—	1.65	3.0	3.3	V
Supply Voltage for Display	VCC	—	8.0	10.0	10.5	V
High Level Input	VIH	—	0.8×VDD	—	VDD	V
Low Level Input	VIL	—	—	—	0.2×VDD	V
High Level Output	VOH	—	0.9×VDD	—	VDD	V
Low Level Output	VOL	—	—	—	0.1×VDD	V
Display 50% Pixel on	ICC	VCC =10.0V	—	46	69	mA