# OLED DISPLAY SPECIFICATION





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# RET025664A

#### **General Specification**

- Module dimension: 84.0×25.8×2.15 mm
- Active area: 69.098×17.258 mm
- Dot Matrix: 256× 64
- Pixel size: 0.248×0.248 mm
- Pixel pitch: 0.27×0.27 mm
- Duty: 1/64 Duty
- Display Mode: Passive Matrix
- Display Color: Monochrome
- IC: SSD1322 COF
- Interface: 6800, 8080, SPI
- Size: 2.8 inch

### Interface Pin Function

Pin	Symbol	I/O	Function			
No.						
Power Supply						
26	VCI	Ρ	Power Supply for Operation			
			This is a voltage supply pin. It must be connected to external			
			source & always be equal to or higher than VDD & VDDIO.			
25	VDD	P	Power Supply for Core Logic Circuit			
			This is a voltage supply pin. It can be supplied externally (within			
			the range of 2.4~2.6V) or regulated internally from VCI. A			
			capacitor should be connected between this pin & VSS under all			
			circumstances.			
24	VDDIO	P	Power Supply for I/O Pin			
			This pin is a power supply pin of I/O buffer. It should be			
			connected to VDD or external source. All I/O signal should have			
			VIH reference to VDDIO. When I/O signal pins (BS0~BS1,			
			D0~D7, control signals) pull high, they should be connected to			
		<u> </u>	VDDIO.			
2	VSS	P	Ground of Logic Circuit			
			This is a ground pin. It also acts as a reference for the logic pins.			
2 20	VCC		Rewer Supply for OLED Panel			
3,29	VUU	P	These are the most positive voltage supply pin of the chin. They			
			must be connected to external source			
5 28	2211	P	Ground of Analog Circuit			
0,20	VLOO	'	These are the analog ground pins. They should be connected to			
			VSS externally			
Driver	I					
22 IRFE   Current Reference for Brightness Adjustment						
			This pin is segment current reference pin. A resistor should be			
			connected between this pin and VSS. Set the current lower than			
			10uA.			
4	VCOMH	Р	Voltage Output High Level for COM Signal			
			This pin is the input pin for the voltage output high level for COM			
			signals. A tantalum capacitor should be connected between this			
			pin and VSS.			
27	VSL	P	Voltage Output Low Level for SEG Signal			
			This is segment voltage reference pin.			
× *			When external VSL is not used, this pin should be left open.			
			When external VSL is used, this pin should connect with resistor			
-			and diode to ground.			
Testing	Pads					
21	FR	0	Frame Frequency Triggering Signal			
			I his pin will send out a signal that could be used to identify the			
			driver status. Nothing should be connected to this pin. It should			
			de lett open individually.			

16	BS0		Communicating Protocol Select				
			These pins are MCU interface sele	ction input.	See the following		
			table:				
				BS0	BS1		
			3-wire SPI	1	0		
			4-wire SPI	0	0		
			8-bit 68XX Parallel	1	1		
17	BS1	-	8-bit 80XX Parallel	0	1		
17	531		0-on 00AA I aranci	v	1		
20	RES#	1	Power Reset for Controller and Driver				
			This pin is reset signal input. When the pin is low, initialization of				
			the chip is executed.				
19	CS#	1	Chip Select				
-	_		This pin is the chip select input. The	e chip is en	abled for MCU		
			communication only when CS# is pulled low				
18	D/C#	1	Data/Command Control				
			This pin is Data/Command control pin. When the pin is pulled				
			high, the input at D7~D0 is treated as display data.				
			When the pin is pulled low, the input at D7~D0 will be transferred				
			to the command register. For detail relationship to MCU interface				
			signals, please refer to the Timing Characteristics Diagrams.				
14	E/RD#	1	Read/Write Enable or Read				
			This pin is MCU interface input. When	nen interfac	ing to a 68XX-		
			series microprocessor, this pin will	be used as	the Enable (E)		
			signal. Read/write operation is initia	ated when t	his pin is pulled		
			high and the CS# is pulled low.				
			When connecting to an 80XX-microprocessor, this pin receives				
			the Read (RD#) signal. Data read operation is initiated when this				
			pin is pulled low and CS# is pulled low.				
4.5	D ////		when senar mode is selected, this pin must be connected to VSS. Read/Write Select or Write				
15	R/W#		Read/Write Select or Write	on interfee	ing to a COVV		
			I his pin is NUCU interface input. When interfacing to a 68XX-				
			selection input. Pull this pin to "High" for road mode and pull it to				
			"Low" for write mode				
			When 80XX interface mode is selected this nin will be the Write				
			(WR#) input Data write operation is initiated when this pin is				
			nulled low and the CS# is nulled low				
			When serial mode is selected this nin must be connected to VSS				
6~13	D7~D0	1/0	Host Data Input/Output Rus				
	2. 20		These pins are 8-bit bi-directional data bus to be connected to the				
× 1			microprocessor's data bus. When serial mode is selected. D1 will				
			be the serial data input SDIN and D	0 will be th	e serial clock input		
			SCLK.				
			Unused pins must be connected to VSS except for D2 in serial				
			mode	•			
Reserve							
23	N.C.	-	Reserved Pin				
			The N.C. pin between function pins	are reserv	ed for compatible		

			and flexible design.
1,30	N.C.	-	Reserved Pin (Supporting Pin)
	(GND)		The supporting pins can reduce the influences from stresses on
			the function pins. These pins must be connected to external
			ground.

#### **Counter Drawing**



## **Absolute Maximum Ratings**

Parameter	Symbol	Min	Мах	Unit
Supply Voltage for Logic	VDD	-0.5	2.75	V
Low voltage power supply	VCI	-0.3	4.0	V
Power supply for I/O pins	VDDIO	-0.5	VCI	V
Supply Voltage for Display	VCC	-0.5	20.0	V
Operating Temperature	TOP	-40	+80	°C
Storage Temperature	TSTG	-40	+85	°C

### **Electrical Characteristics**

#### **DC Electrical Characteristics**

Item	Symbol	Condition	Min	Тур	Max	Unit
Supply Voltage for Logic	VCI	-	2.8	3.0	3.3	V
Supply Voltage for Display	VCC	_	14	14.5	15	V
High Level Input	VIH	_	0.8×VDDIO	_	VDDIO	V
Low Level Input	VIL	_	0	_	0.2×VDDIO	V
High Level Output	VOH	_	0.9×VDDIO	_	VDDIO	V
Low Level Output	VOL	_	0	_	0.1×VDDIO	V
50% Check Board ope Current	VCC =14.5V	—	30	32	mA	