S9MPA021

16V Dual P-Channel MOSFETs

General Description

The S9MPA021 is the Dual P-Channel logic enhancement mode power field effect transistor is produced using high cell density, DMOS trench technology. This high-density process is especially tailored to minimize on-state resistance.

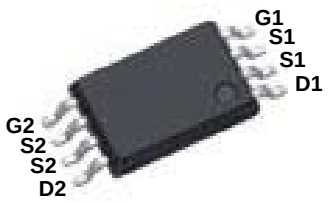
These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other Battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

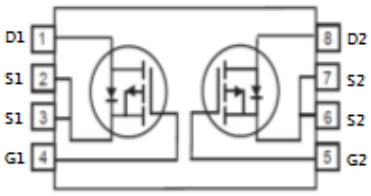
BV_{DSS}	$R_{DS(ON)}$	I_D
-16 V	21.1 mΩ	-8 A

Features

- -16V, -8A, $R_{DS(ON)}$=21.1mΩ@V_{GS}= -4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

TSSOP-8 Pin Configuration





Applications

- POWER Management in Note
- Portable Equipment
- Battery Powered System
- PWM applications
- Load Switch

Absolute Maximum Ratings T_C=25°C unless otherwise noted

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-16	V
V_{GS}	Gate-Source Voltage	±12	V
I_D	Drain Current - Continuous (T_C=25°C)	-8	A
	Drain Current - Continuous (T_C=100°C)	-5	A
I_{DM}	Drain Current - Pulsed	-32	A
P_D	Power Dissipation	1.56	W
T_J	Operating Junction Temperature Range	-50 to 150	°C
T_{STG}	Storage Temperature Range	-50 to 150	°C
Marking Code		PA021 / DEW2188	

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction to Ambient	---	80	°C/W

Electrical Characteristics (T_J=25°C, unless otherwise noted)

Off Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}= 0V , I_D= -250uA	-16	---	---	V
I_{DSS}	Drain-Source Leakage Current	V_{DS}= -16V , V_{GS}= 0V	---	---	-1	uA
		V_{DS}= -12V , V_{GS}= 0V , T_J=125°C	---	---	-10	uA
I_{GSS}	Gate-Source Leakage Current	V_{GS}= ±12V , V_{DS}= 0V	---	---	±100	nA

On Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}= -4.5V , I_D= -7A	---	15	21.1	mΩ
		V_{GS}= -2.5V , I_D= -6A	---	19.4	26.7	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D= -250uA	-0.55	-0.7	-0.9	V

Dynamic and switching Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Q_g	Total Gate Charge	V_{DS}= -10V , V_{GS}= -4.5V , I_D= -6A	---	12	---	nC
Q_{gs}	Gate-Source Charge		---	2	---	
Q_{gd}	Gate-Drain Charge		---	3	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DS}= -10V , V_{GEN}= -4.5V , R_G= 3Ω , I_D= -1A	---	10.2	---	nS
T_r	Rise Time		---	23.5	---	
$T_{d(off)}$	Turn-Off Delay Time		---	64	---	
T_f	Fall Time		---	37.5	---	
C_{iss}	Input Capacitance	V_{DS}= -10V , V_{GS}= 0V , F= 1MHz	---	1320	---	pF
C_{oss}	Output Capacitance		---	290	---	
C_{rss}	Reverse Transfer Capacitance		---	195	---	

Drain-Source Diode Characteristics and Ratings

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{SD}	Diode Forward Voltage	V_{GS}= 0V , I_S= -1A	---	---	-1.5	V

Characteristics Curves

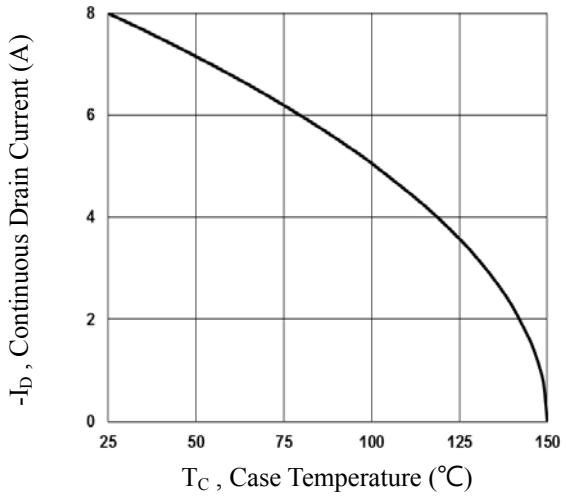


Fig.1 Continuous Drain Current vs. T_C

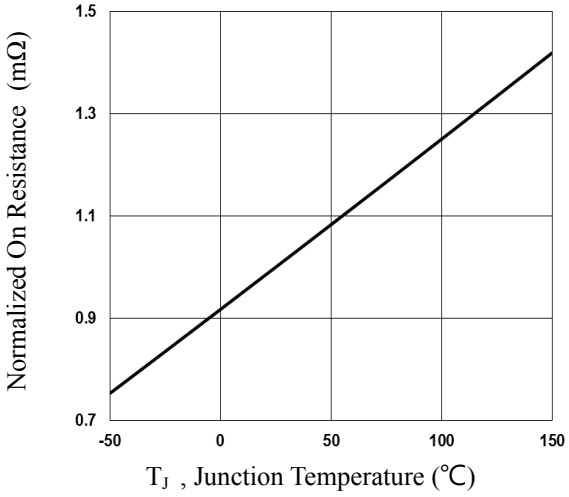


Fig.2 Normalized RDSON vs. T_J

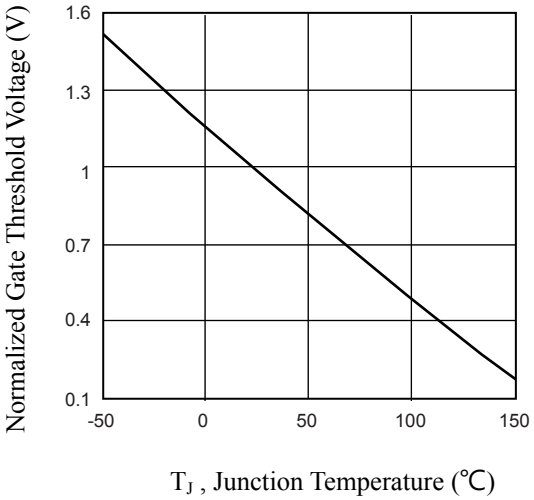


Fig.3 Normalized V_{th} vs. T_J

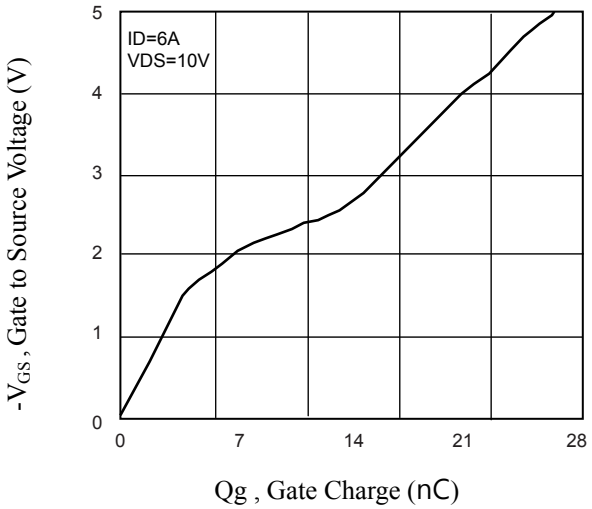


Fig.4 Gate Charge Waveform

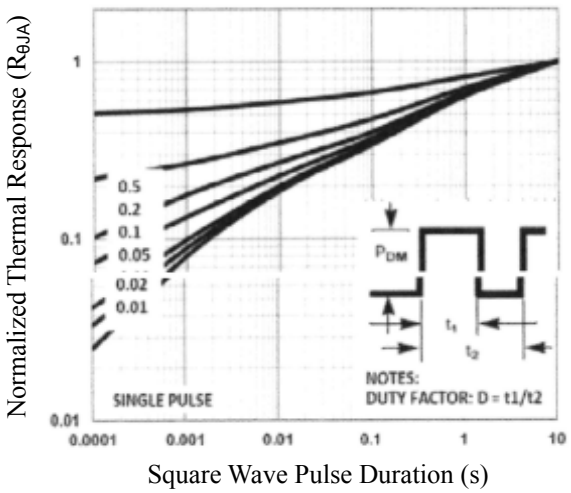


Fig.5 Normalized Transient Response

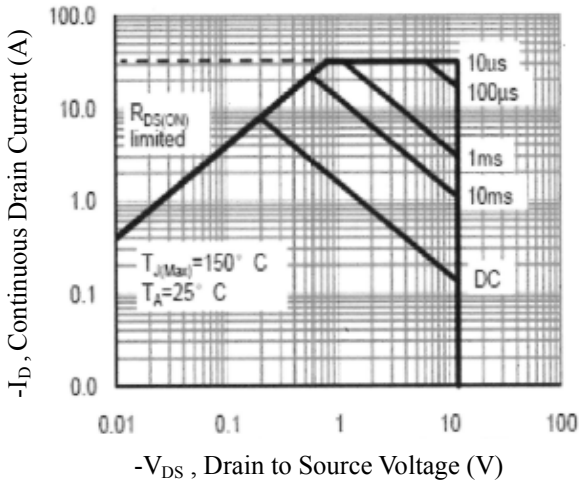


Fig.6 Maximum Safe Operation Area

Characteristics Curves

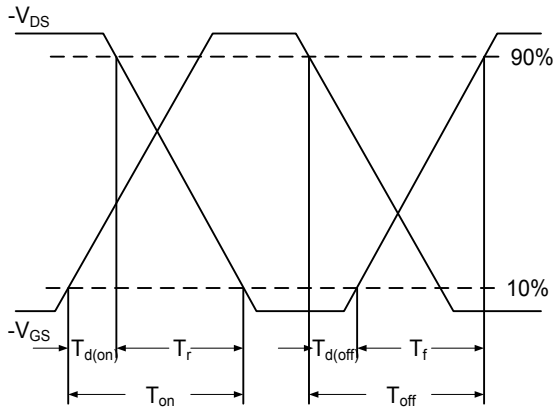


Fig.7 Switching Time Waveform

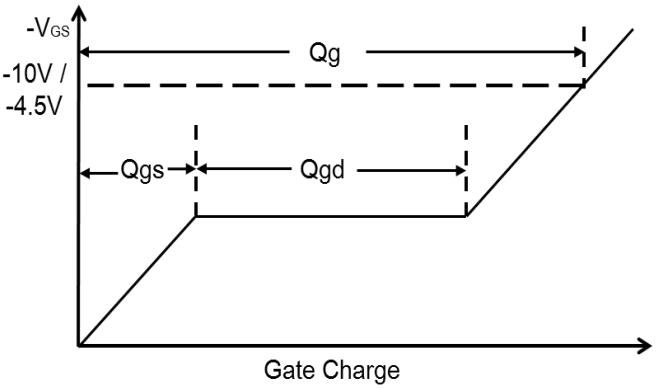
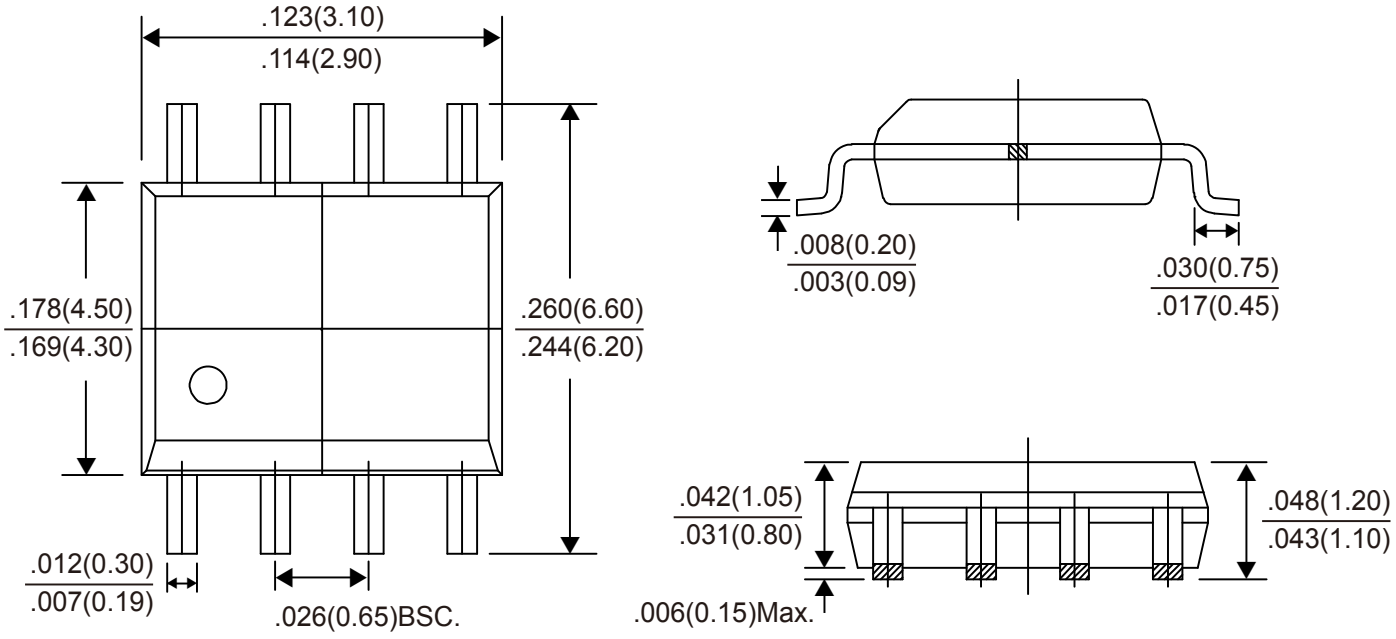


Fig.8 Gate Charge Waveform

Package Outline Dimensions



TSSOP-8

Dimensions in inches and (millimeters)

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