



## **General Description**

These P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

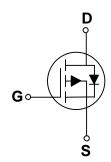
BV <sub>DSS</sub>	R <sub>DS(ON)</sub>	I <sub>D</sub>
-30 V	8.5 mΩ	-60 A

#### **Features**

- $R_{DS(ON)} \leq 8.5 \text{m}\Omega @V_{GS} = -10V$
- · Fast switching
- · Green Device Available
- · Improved dv/dt capability

### PPAK5X6 Pin Configuration





## **Applications**

- · MB / VGA / Vcore
- · POL Applications
- · LED Application
- · Load Switch

Absolute Maximum Ratings T <sub>C</sub> =25°C unless otherwise noted						
Symbol	Parameter	Rating	Units			
$V_{DS}$	Drain-Source Voltage	-30	V			
$V_{GS}$	Gate-Source Voltage	±20	V			
I_	Drain Current - Continuous (T <sub>C</sub> =25°C)	-60	Α			
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> =100°C)	-38	Α			
I <sub>DM</sub>	Drain Current - Pulsed (NOTE 1)	-240	Α			
P <sub>D</sub>	Power Dissipation (T <sub>C</sub> =25°C)	96	W			
ı D	Power Dissipation - Derate above 25°C	0.77	W/°C			
$T_J$	Operating Junction Temperature Range	-55 to 150	°C			
T <sub>STG</sub>	Storage Temperature Range	-55 to 150	°C			
Marking Code		PC8P5				

Thermal Characteristics					
Symbol	Parameter		Max.	Unit	
$R_{\theta JA}$	Thermal Resistance Junction to Ambient		62	°C/W	
$R_{ heta JC}$	Thermal Resistance Junction to Case		1.3	°C/W	





## Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)

#### **Off Characteristics**

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS}$ =0V , $I_D$ = -250uA	-30			V
I <sub>DSS</sub>	IDrain-Source Leakage Current	$V_{DS}$ = -30V , $V_{GS}$ =0V , $T_{J}$ =25 $^{\circ}$ C			-1	uA
		$V_{DS}$ = -24V , $V_{GS}$ =0V , $T_{J}$ =125°C			-10	uA
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}$ = ±20V , $V_{DS}$ =0V			±100	nA

#### On Characteristics

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	$V_{GS}$ = -10V , $I_D$ = -10A		7.1	8.5	- mΩ
		$V_{GS}$ = -4.5V , $I_{D}$ = -8A		11.5	14	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$ , $I_D=-250uA$	-1.2	-1.6	-2.5	V
gfs	Forward Transconductance	$V_{DS}$ = -10V , $I_{D}$ = -10A		14		S

#### **Dynamic and switching Characteristics**

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
$Q_g$	Total Gate Charge	V <sub>DS</sub> = -15V , V <sub>GS</sub> = -4.5V ,		35	56	
$Q_gs$	Gate-Source Charge	I <sub>D</sub> = -10A (NOTE 2 \ 3)		10.8	16	nC
$Q_{gd}$	Gate-Drain Charge			10.6	16	
$T_{d(on)}$	Turn-On Delay Time	45)/ )/ 40)/		24.5	38	
$T_r$	Rise Time	$V_{DD}$ = -15V , $V_{GS}$ = -10V , $R_G$ = 6 $\Omega$ , $I_D$ = -1A (NOTE 2 \cdot 3)		10.5	16	nS
$T_{d(off)}$	Turn-Off Delay Time			156.8	230	113
$T_f$	Fall Time			50	75	
$C_{iss}$	Input Capacitance			3300	4800	
C <sub>oss</sub>	Output Capacitance	$V_{DS}$ = -15V , $V_{GS}$ = 0V , F= 1MHz		410	700	pF
$C_{rss}$	Reverse Transfer Capacitance			280	500	
Rg	Gate resistance	$V_{GS}$ = 0V , $V_{DS}$ = 0V , F=1MHz		8.5	12	Ω

#### **Drain-Source Diode Characteristics and Ratings**

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
I <sub>S</sub>	Continuous Source Current	V <sub>G</sub> = V <sub>D</sub> = 0V , Force Current			-60	Α
I <sub>SM</sub>	Pulsed Source Current				-120	Α
$V_{SD}$	Diode Forward Voltage	$V_{GS}$ = 0V , $I_S$ = -1A , $T_J$ =25 $^{\circ}$ C			-1	V

### NOTES:

- 1. Repetitive Rating: Pulsed width limited by maximum junction temperature.
- 2. The data tested by pulsed , pulse width  $\leqq$  300us , duty cycle  $\leqq$  2%.
- 3. Essentially independent of operating temperature.





#### **Characteristics Curves**

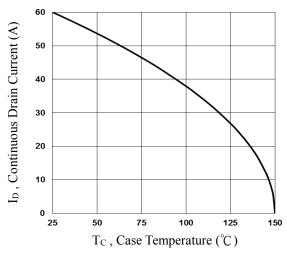


Fig.1 Continuous Drain Current vs. Tc

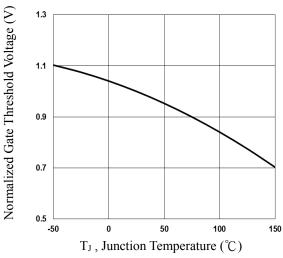


Fig.3 Normalized V<sub>th</sub> vs. T<sub>J</sub>

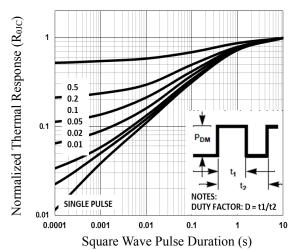


Fig.5 Normalized Transient Impedance

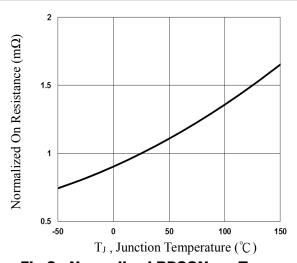


Fig.2 Normalized RDSON vs. T<sub>J</sub>

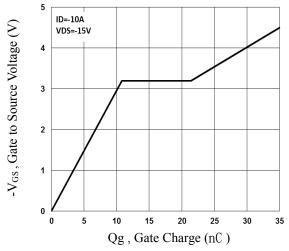


Fig.4 Gate Charge Waveform

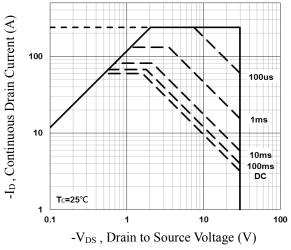
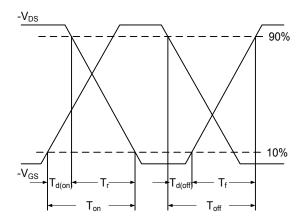


Fig.6 Maximum Safe Operation Area





#### **Characteristics Curves**





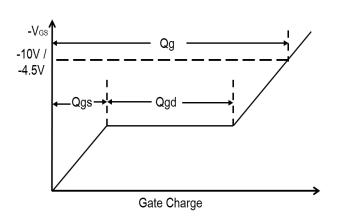
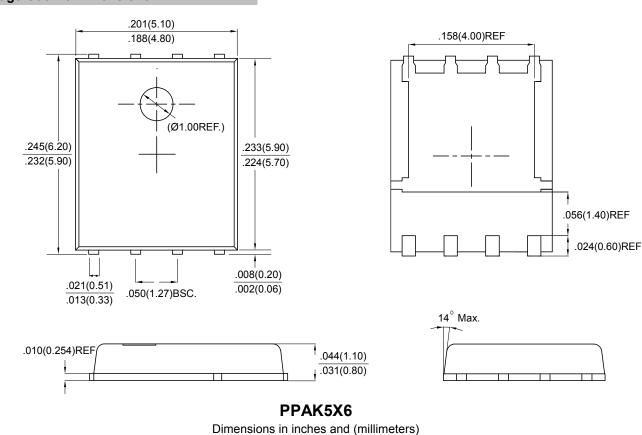


Fig.8 Gate Charge Waveform

## **Package Outline Dimensions**





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