



100V N-Channel MOSFETs

General Description

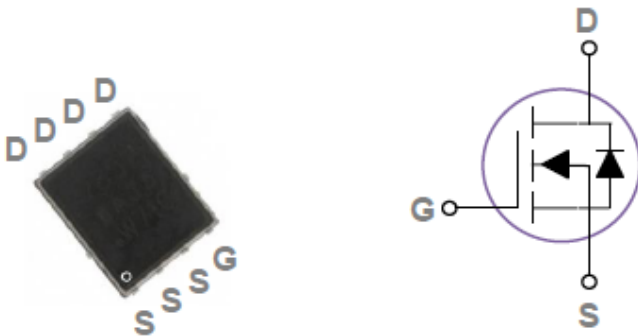
These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications

BVDSS	RDSON	ID
100V	7.2mΩ	65A

Features

- 100V,65A,RDS(ON)=7.2mΩ@VGS=10V
- Improved dv/dt capability
- Fast switching
- 100% EAS Guaranteed
- Green Device Available

PPAK5X6 Pin Configuration



Applications

- Networking
- Load Switch
- LED applications
- Quick Charger

Absolute Maximum Ratings Tc=25°C unless otherwise noted

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	100	V
V _{GS}	Gate-Source Voltage	+20 / -12	V
I _D	Drain Current – Continuous (TC=25°C) (Chip Limitation)	65	A
	Drain Current – Continuous (TC=100°C) (Chip Limitation)	40	A
I _{DM}	Drain Current – Pulsed ¹	255	A
EAS	Single Pulse Avalanche Energy ²	230	mJ
IAS	Single Pulse Avalanche Current ²	65	A
P _D	Power Dissipation (TC=25°C)	135	W
	Power Dissipation – Derate above 25°C	1.2	W/°C
T _{STG}	Storage Temperature Range	-50 to 150	°C
T _J	Operating Junction Temperature Range	-50 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction to ambient	---	65	°C/W
R _{θJC}	Thermal Resistance Junction to Case	---	1.1	°C/W



Electrical Characteristics (T_J=25°C, unless otherwise noted)

Off Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	100	---	---	V
ΔBV _{DSS} /ΔT _J	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =1mA	---	0.05	---	V/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =100V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =80V, V _{GS} =0V, T _J =125°C	---	---	10	uA
I _{GSS}	Gate-Source Leakage Current	V _{GS} =+20V, V _{DS} =0V	---	---	100	nA

On Characteristics

R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =18A	---	6.5	7.5	mΩ
		V _{GS} =4.5V, I _D =10A	---	9.0	11.5	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	1.2	---	2.5	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	-5.5	---	mV/°C
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =3A	---	15	---	S

Dynamic and switching Characteristics

Q _g	Total Gate Charge ^{3,4}	V _{DS} =80V, V _{GS} =10V, I _D =10A	---	55	85	nC
Q _{gs}	Gate-Source Charge ^{3,4}		---	8.0	15	
Q _{gd}	Gate-Drain Charge ^{3,4}		---	15	25	
T _{d(on)}	Turn-On Delay Time ^{3,4}	V _{DD} =50V, V _{GS} =10V, R _G =6Ω I _D =1A	---	15	33	ns
T _r	Rise Time ^{3,4}		---	35	68	
T _{d(off)}	Turn-Off Delay Time ^{3,4}		---	65	130	
T _f	Fall Time ^{3,4}		---	30	58	
C _{iss}	Input Capacitance	V _{DS} =25V, V _{GS} =0V, F=1MHz	---	---	6500	pF
C _{oss}	Output Capacitance		---	---	1800	
C _{rss}	Reverse Transfer Capacitance		---	---	180	
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, F=1MHz	---	1.25	---	Ω

Drain-Source Diode Characteristics and Maximum Ratings

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current	V _G =V _D =0V, Force Current	---	---	60	A
I _{SM}	Pulsed Source Current		---	---	125	A
V _{SD}	Diode Forward Voltage	V _{GS} =0V, I _S =1A, T _J =25°C	---	---	1	V

Note :

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. V_{DD}=50V, V_{GS}=10V, L=0.1mH, I_{AS}=68A., R_G=25Ω, Starting T_J=25°C.
3. The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%.
4. Essentially independent of operating temperature.



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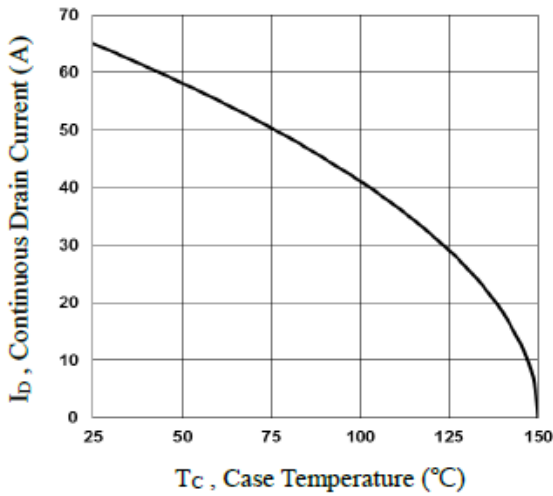


Fig.1 Continuous Drain Current vs. T_C

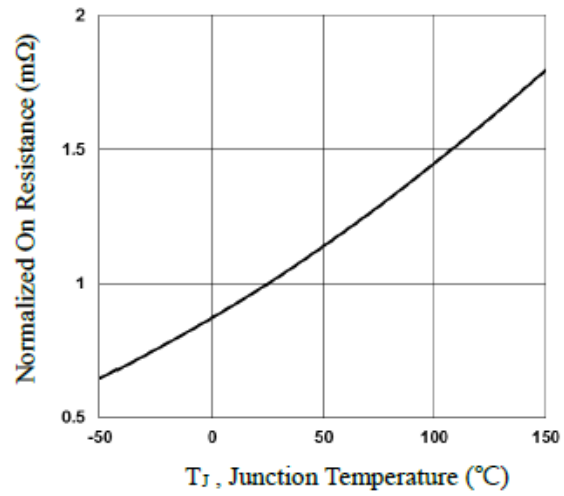


Fig.2 Normalized RDSONN vs. T_J

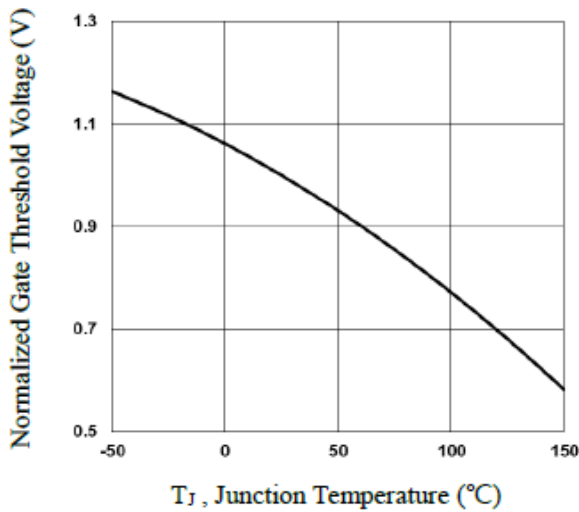


Fig.3 Normalized V_{th} vs. T_J

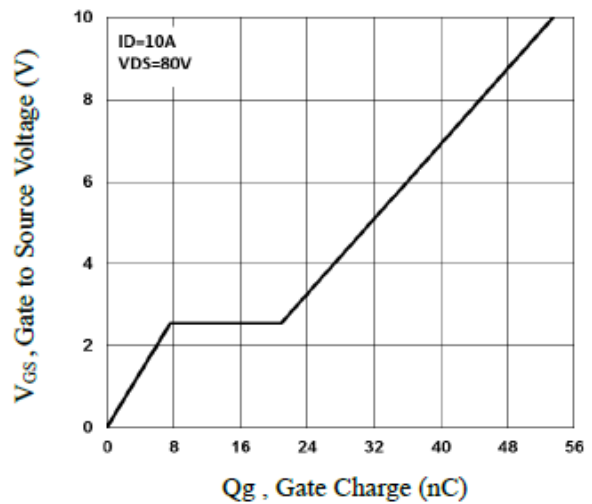


Fig.4 Gate Charge Characteristics

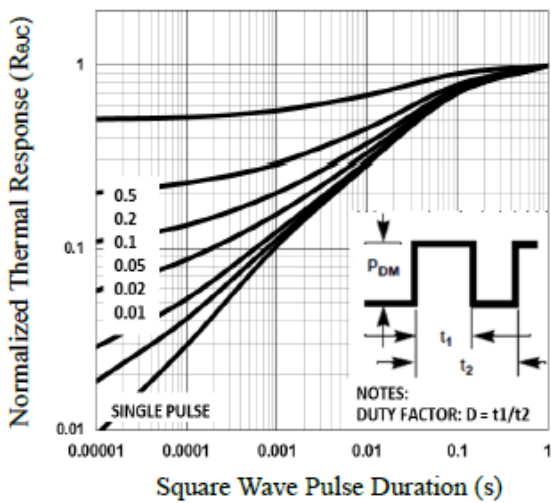


Fig.5 Normalized Transient Impedance

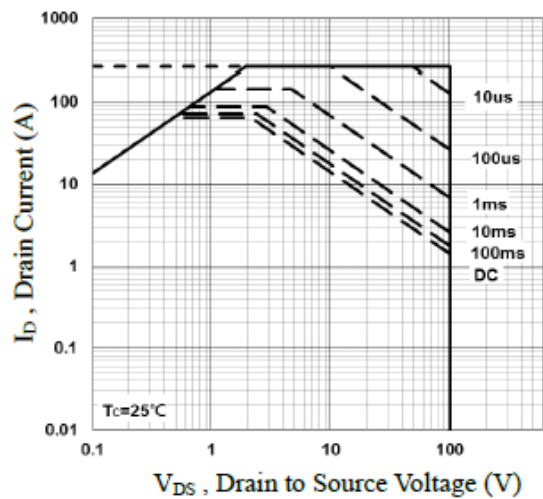


Fig.6 Maximum Safe Operation Area

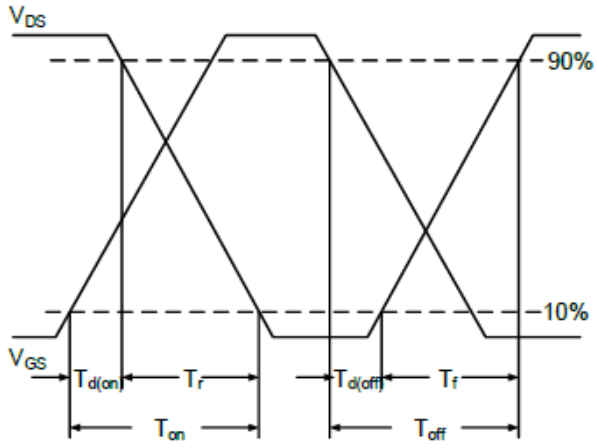


Fig.7 Switching Time Waveform

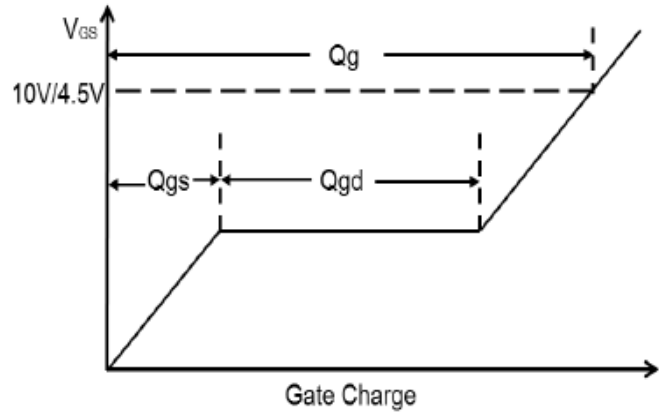
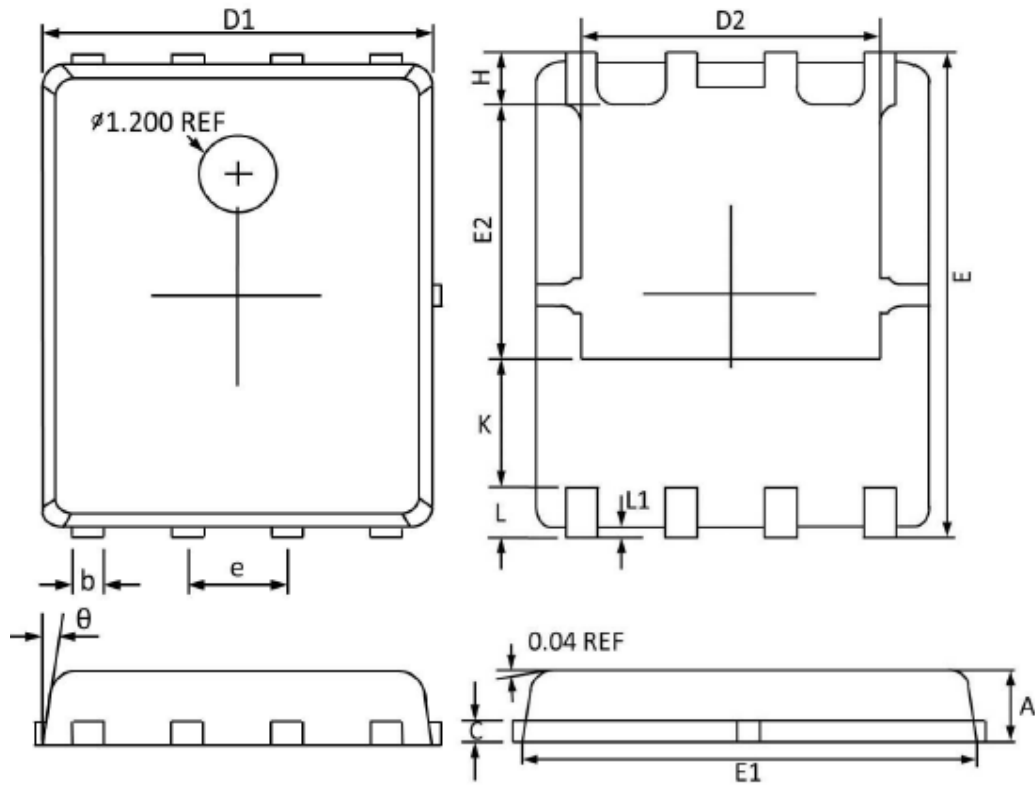


Fig.8 Gate Charge Waveform



PPAK5X6 PACKAGE INFORMATION



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MAX	MIN	MAX	MIN
A	1.100	0.800	0.043	0.031
b	0.510	0.330	0.020	0.013
C	0.300	0.200	0.012	0.008
D1	5.100	4.800	0.201	0.189
D2	4.100	3.610	0.161	0.142
E	6.200	5.900	0.244	0.232
E1	5.900	5.700	0.232	0.224
E2	3.780	3.350	0.149	0.132
e	1.27BSC		0.05BSC	
H	0.700	0.410	0.028	0.016
K	1.500	1.100	0.059	0.043
L	0.710	0.510	0.028	0.020
L1	0.200	0.060	0.008	0.002
θ	12°	0°	12°	0°



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