



100V N-Channel MOSFETs

General Description

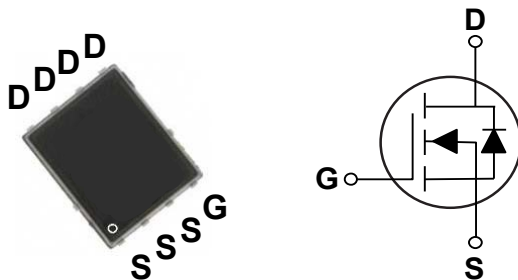
These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

BV_{DSS}	R_{DS(ON)}	I_D
100 V	5.5 mΩ	70 A

Features

- $R_{DS(ON)} \leq 5.5m\Omega @ V_{GS}=10V$
- Improved dv/dt capability
- Fast switching
- Green Device Available

PPAK5X6 Pin Configuration



Applications

- Networking
- Load Switch
- LED applications
- Quick Charger

Absolute Maximum Ratings $T_C=25^\circ C$ unless otherwise noted

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	+20 / -12	V
I_D	Drain Current – Continuous ($T_C=25^\circ C$)	70	A
	Drain Current – Continuous ($T_C=100^\circ C$)	44	A
I_{DM}	Drain Current – Pulsed (NOTE 1)	280	A
EAS	Single Pulse Avalanche Energy (NOTE 2)	320	mJ
IAS	Avalanche Current (NOTE 2)	80	A
P_D	Power Dissipation ($T_C=25^\circ C$)	142	W
T_J	Operating Junction Temperature Range	-50 to 150	$^\circ C$
T_{STG}	Storage Temperature Range	-50 to 150	$^\circ C$
Marking Code		NM5P5	

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction to Ambient	---	62	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction to Case	---	0.88	$^\circ C/W$

**Electrical Characteristics (T_J=25°C, unless otherwise noted)****Off Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	100	---	---	V
I _{DSS}	Drain-Source Leakage Current	V _{DS} =100V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =80V, V _{GS} =0V, T _J =85°C	---	---	10	uA
I _{GSS}	Gate-Source Leakage Current	V _{GS} =20V, V _{DS} =0V	---	---	100	nA

On Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A	---	4.6	5.5	mΩ
		V _{GS} =4.5V, I _D =10A	---	6.2	7.8	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	1.0	1.6	2.5	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =5A	---	18	---	S

Dynamic and switching Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Q _g	Total Gate Charge	V _{DS} =80V, V _{GS} =10V, I _D =10A (NOTE 3 · 4)	---	58.2	---	nC
Q _{gs}	Gate-Source Charge		---	9.2	---	
Q _{gd}	Gate-Drain Charge		---	20.8	---	
T _{d(on)}	Turn-On Delay Time	V _{DD} =50V, V _{GS} =10V, R _G =6Ω, I _D =1A (NOTE 3 · 4)	---	24	---	nS
T _r	Rise Time		---	19.8	---	
T _{d(off)}	Turn-Off Delay Time		---	46	---	
T _f	Fall Time		---	26	---	
C _{iss}	Input Capacitance	V _{DS} =25V, V _{GS} =0V, F=1MHz	---	4570	---	pF
C _{oss}	Output Capacitance		---	1180	---	
C _{rss}	Reverse Transfer Capacitance		---	49	---	
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, F=1MHz	---	2	---	Ω

Drain-Source Diode Characteristics and Ratings

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current	V _G =V _D =0V, Force Current	---	---	70	A
I _{SM}	Pulsed Source Current		---	---	140	A
V _{SD}	Diode Forward Voltage	V _{GS} =0V, I _S =1A, T _J =25°C	---	---	1	V
t _{rr}	Reverse Recovery Time	V _{GS} =0V, I _S =10A,	---	61.6	---	nS
Q _{rr}	Reverse Recovery Charge	dI/dt=100A/us, T _J =25°C	---	120	---	nC

NOTES :

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=80A, R_G=25Ω, starting T_J=25°C.
3. The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%.
4. Essentially independent of operating temperature.



Characteristics Curves

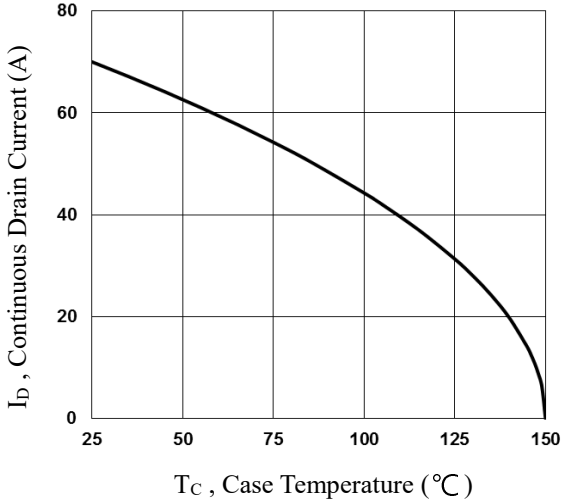


Fig.1 Continuous Drain Current vs. T_c

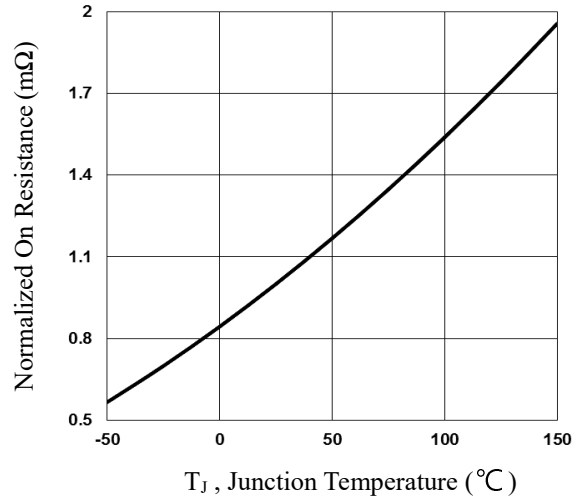


Fig.2 Normalized $R_{DS(on)}$ vs. T_j

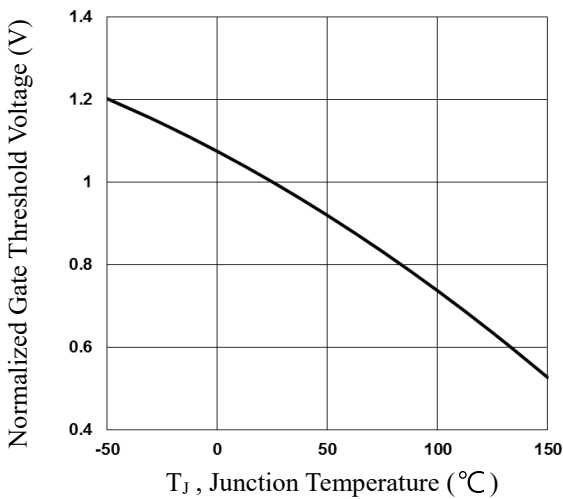


Fig.3 Normalized V_{th} vs. T_j

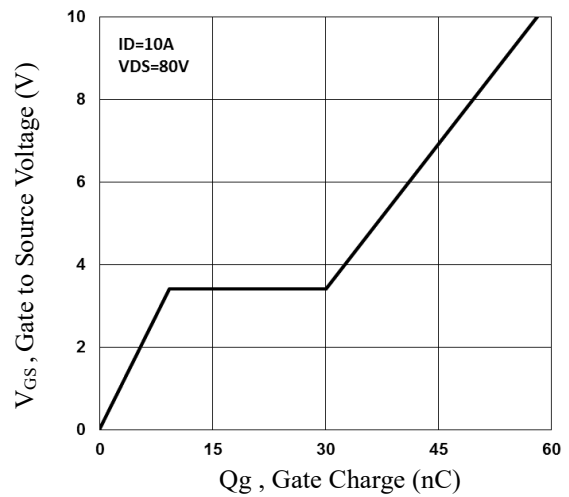


Fig.4 Gate Charge Characteristics

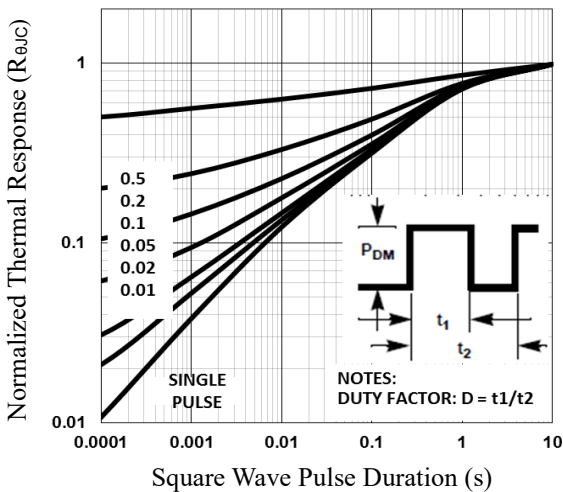


Fig.5 Normalized Transient Impedance

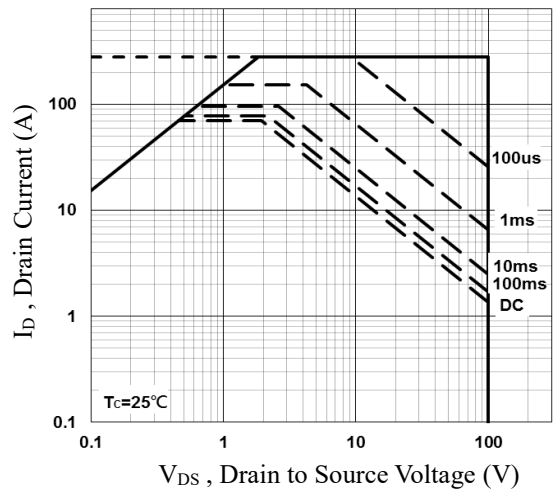


Fig.6 Maximum Safe Operation Area



Characteristics Curves

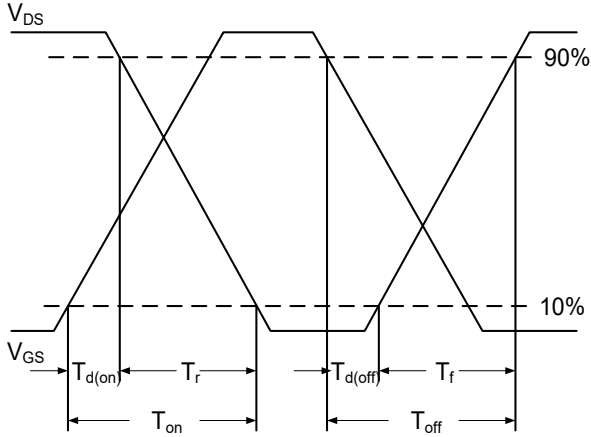


Fig.7 Switching Time Waveform

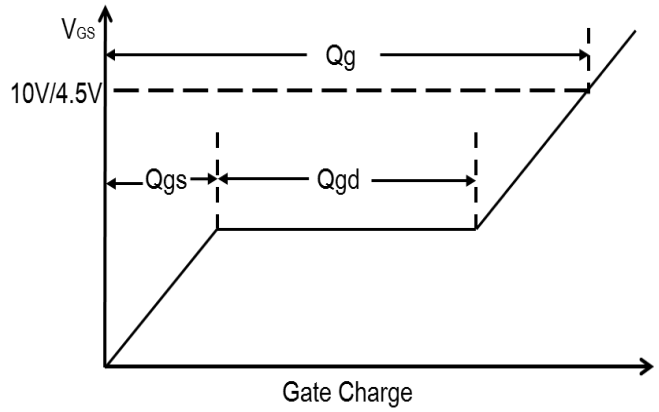
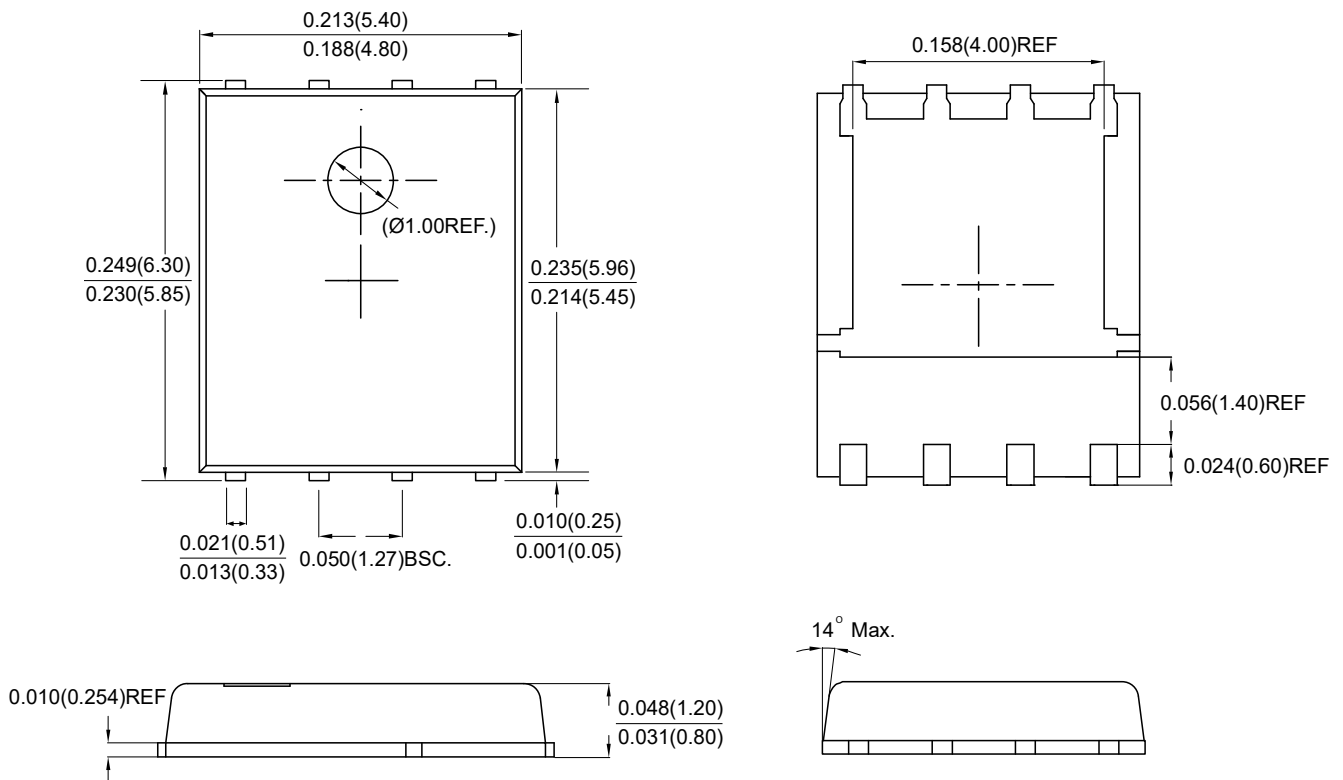


Fig.8 Gate Charge Waveform

Package Outline Dimensions



PPAK5X6

Dimensions in inches and (millimeters)



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