



General Description

These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

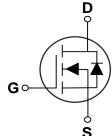
BV _{DSS}	R _{DS(ON)}	I _D
30 V	1.6 mΩ	130 A

Features

- $R_{DS(ON)} \le 1.6 m\Omega @V_{GS} = 10V$
- · Fast switching
- · Improved dv/dt capability
- · Green Device Available

PPAK5X6 Pin Configuration





Applications

- MB / VGA / Server Vcore
- POL Applications
- · SMPS 2nd SR
- · BMS System

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	±20	V
1	Drain Current - Continuous (T _C =25°C)	130	Α
I _D	Drain Current - Continuous (T _C =100°C)	82	Α
I _{DM}	Drain Current - Pulsed (NOTE 1)	520	Α
EAS	Single Pulse Avalanche Energy (NOTE 2)	245	mJ
IAS	Single Pulse Avalanche Current (NOTE 2)	70	Α
В	Power Dissipation (T _C =25°C)	166	W
P_D	Power Dissipation - Derate above 25°C	1.33	W/°(
T _J	Operating Junction Temperature Range	-50 to 175	°C
T_{STG}	Storage Temperature Range	-50 to 175	°C
larking Code		NC1P6	

Thermal Characteristics						
Symbol Parameter			Max.	Unit		
$R_{\theta JA}$	Thermal Resistance Junction to Ambient		62	°C/W		
R _{BJC} Thermal Resistance Junction to Case			0.9	°C/W		





Electrical Characteristics (T_J=25°C, unless otherwise noted)

Off Characteristics

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V_{GS} =0V , I_D =250uA	30			V
I	IDSS IDTAIN-SOUTCE LEAKAGE CUTTENT	V_{DS} =27V , V_{GS} =0V , T_J =25°C			1	uA
DSS		V _{DS} =24V , V _{GS} =0V , T _J =85°C			10	uA
I _{GSS}	Gate-Source Leakage Current	V_{GS} =±20V , V_{DS} =0V			±100	nA

On Characteristics

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
R _{DS(ON)}	Static Drain-Source On-Resistance	V_{GS} =10V , I_D =30A		1.2	1.6	mΩ
DS(ON)	(NOTE 3)	V _{GS} =4.5V , I _D =15A		1.8	2.4	11122
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=250uA$	1.0	1.6	2.5	V
gfs	Forward Transconductance	V_{DS} =10V , I_{D} =15A		30		S

Dynamic and switching Characteristics

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
Q_g	Total Gate Charge	\\ 45\\ \\ 45\\ \\ 100		65	120	
Q_gs	Gate-Source Charge	V _{DS} =15V , V _{GS} =4.5V , I _D =10A (NOTE 3 \ 4)		16	30	nC
Q_{gd}	Gate-Drain Charge	(10123 4)		21	40	
$T_{d(on)}$	Turn-On Delay Time	V_{DD} =15V , V_{GS} =10V , R_{G} =3.3 Ω , I_{D} =1A (NOTE 3 \ 4)		28	56	
T _r	Rise Time			45	90	nS
$T_{d(off)}$	Turn-Off Delay Time			105	200	113
T_f	Fall Time			40	80	
C _{iss}	Input Capacitance	V _{DS} =25V , V _{GS} =0V , F=1MHz		7720	11000	
C _{oss}	Output Capacitance			945	1400	pF
C _{rss}	Reverse Transfer Capacitance			435	650	
R_g	Gate resistance	V_{GS} =0V , V_{DS} =0V , f=1MHz		1.2	2.4	Ω

Guaranteed Avalanche Energy

-		6,					
	Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
	EAS	Single Pulse Avalanche Energy	V _{DD} =25V , L=0.1mH , IAS=30A	45			mJ

Drain-Source Diode Characteristics and Ratings

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
I _S	Continuous Source Current	-V _G =V _D =0V,Force Current			130	Α
I _{SM}	Pulsed Source Current (NOTE 3)				260	Α
V_{SD}	Diode Forward Voltage (NOTE 3)	V_{GS} =0V , I_{S} =1A , T_{J} =25 $^{\circ}$ C			1	V

NOTES

- 1. Repetitive Rating: Pulsed width limited by maximum junction temperature.
- 2. V_{DD} =25V, V_{GS} =10V, L=0.1mH, I_{AS} =70A, R_{G} =25 Ω , Starting T_{J} =25 $^{\circ}$ C.
- 3. The data tested by pulsed , pulse width \leq 300us , duty cycle \leq 2%.
- 4. Essentially independent of operating temperature.





Characteristics Curves

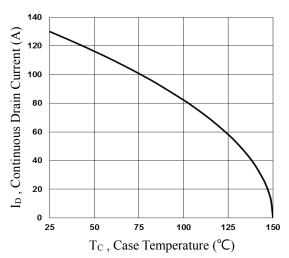


Fig.1 Continuous Drain Current vs. Tc

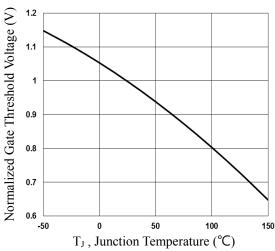


Fig.3 Normalized V_{th} vs. T_J

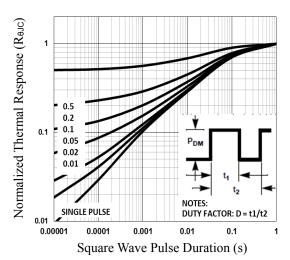


Fig.5 Normalized Transient Impedance

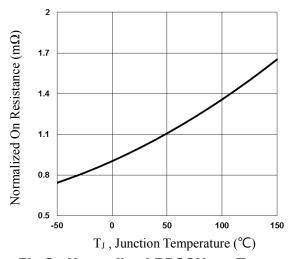


Fig.2 Normalized RDSON vs. TJ

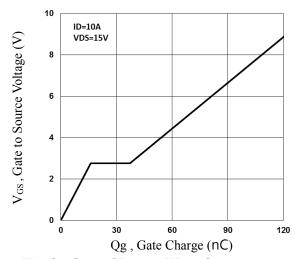


Fig.4 Gate Charge Waveform

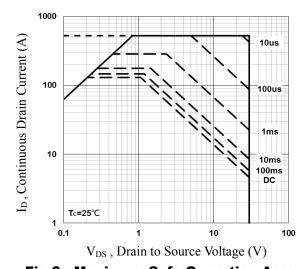


Fig.6 Maximum Safe Operation Area





Characteristics Curves

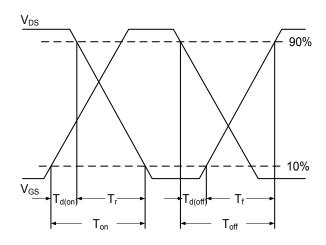


Fig.7 Switching Time Waveform

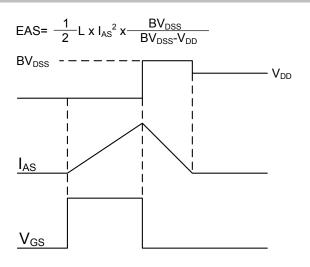
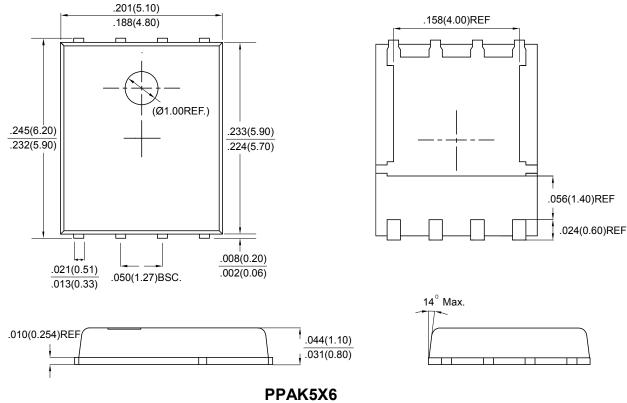


Fig.8 EAS Waveform

Package Outline Dimensions







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