2.1MHz, 600mA MOSFET Switching Regulator IC for Synchronous Buck Converter

■ FEATURES

- Programmable 3.3V, 5V or Adjustable Output
- Only 3 external components required (Fixed Output Voltage type)
- Synchronous rectification
- High oscillating frequency — Fixed 2.1MHz typ.
- External clock synchronization — 1.95MHz to 2.5MHz
- Efficiency improvement at light load (MODE pin selectable)
- Low quiescent current at sleep mode — 20µA typ.
- Current mode control
- Wide operating voltage range — 3.4V to 40V
- Switching current — 0.85A min.
- PWM control
- Maximum duty cycle — 100%
- Built-in compensation circuit
- Correspond to ceramic capacitor (MLCC)
- Soft start function — 1ms typ.
- Undervoltage lockout (UVLO)
- Overcurrent protection (Hiccup type)
- Thermal shutdown
- Power Good function
- Standby function
- Package — HSOP8-M1

■ DESCRIPTION

The NJW4175 is a high speed oscillating frequency buck converter with 40V/600mA MOSFET. The NJW4175 have PWM/PFM mode to ensure high efficiency at light load.

Operating voltage range is wide input range from 3.4V to 40V. Moreover, 100% maximum duty cycle contribute to maintain stable output voltage even if supply voltage drops.

Internal protection functions: UVLO, an over current protection and a thermal shutdown circuit can protect circuit when abnormal condition.

The NJW4175 has wide coverage in consumer electronics and industrial application, because of features that are wide input range, fixed output voltage type, high switching oscillating frequency and 100% maximum duty cycle.

■ PRODUCT CLASSIFICATION

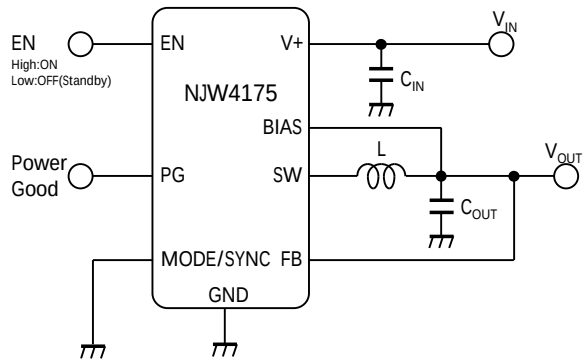
NAME	Ver.	f_{osc}	V_{OUT}	Package
NJW4175GM1-33A	A	2.1MHz	3.3V	HSOP8-M1
NJW4175GM1-05A			5.0V	HSOP8-M1
NJW4175GM1-JA			Ajustable	HSOP8-M1

■ APPLICATIONS

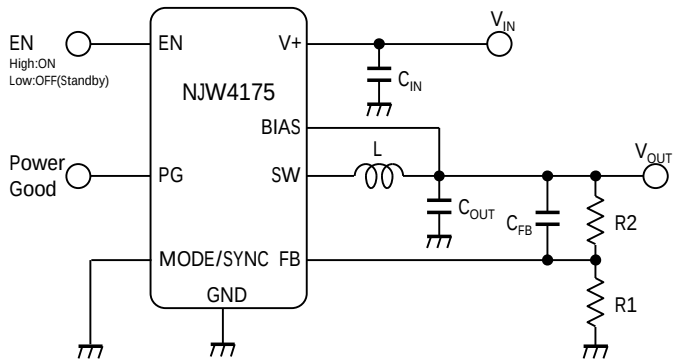
- Power supply for camera
- Low power buck converter
- Industrial equipment

■ TYPICAL APPLICATION

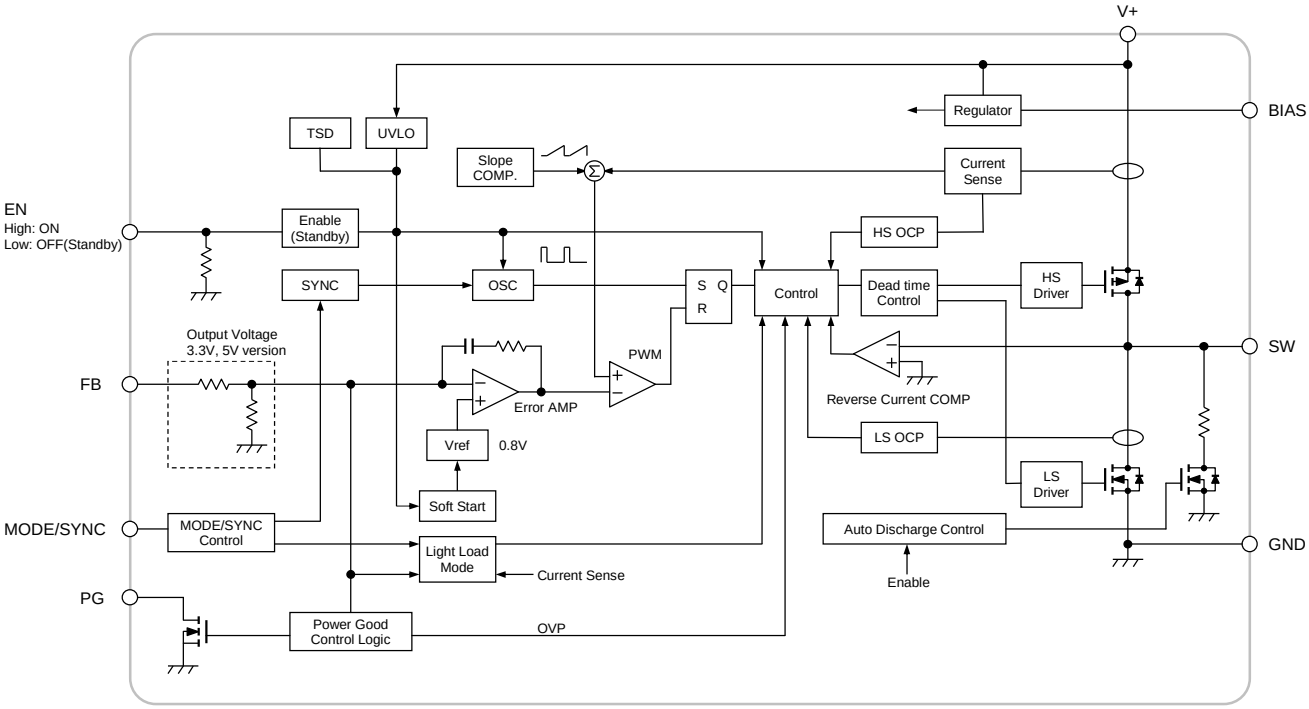
<Fixed Output Voltage type>



<Adjustable Output Voltage type>



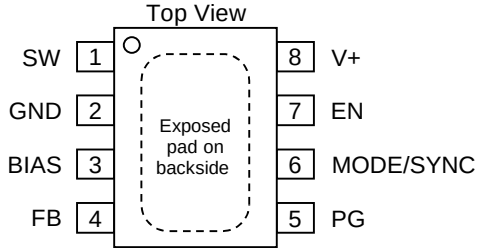
■ BLOCK DIAGRAM



■ PIN CONFIGURATION

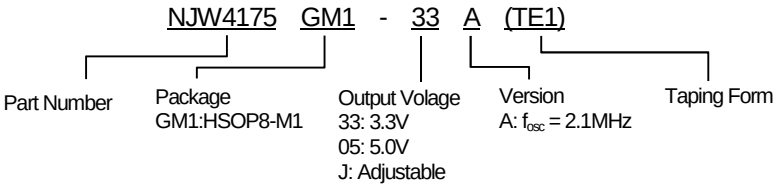
HSOP8-M1

Top View



PIN NO.	NAME	FUNCTION
1	SW	Switch output
2	GND	Ground
3	BIAS	Bias input
4	FB	Feedback input
5	PG	Power Good output
6	MODE/SYNC	Light load mode select and external clock synchronization
7	EN	Enable control
8	V+	Power supply

■ PRODUCT NAME INFORMATION



■ ORDERING INFORMATION

PRODUCT NAME	PACKAGE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ (pcs)
NJW4175GM1-33A (TE1)	HSOP8-M1	Yes	Yes	Sn100%	75AA	81	3000
NJW4175GM1-05A (TE1)	HSOP8-M1	Yes	Yes	Sn100%	75BA	81	3000
NJW4175GM1-JA (TE1)	HSOP8-M1	Yes	Yes	Sn100%	75JA	81	3000

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Pin Voltage	V^+	−0.3 to 45	V
SW Pin Voltage	V_{SW}	−0.3 to 45	V
EN Pin Voltage	V_{EN}	−0.3 to 45	V
BIAS Pin Voltage	V_{BIAS}	−0.3 to 45	V
FB Pin Voltage	V_{FB}	−0.3 to 7	V
MODE / SYNC Pin Voltage	$V_{MODE/SYNC}$	−0.3 to 45	V
PG Pin Voltage	V_{PG}	−0.3 to 7	V
Power Dissipation (T_a = 25°C) HSOP8-M1	P_D	2-Layer / 4-Layer 790 (1) / 2500 (2)	mW
Junction Temperature	T_j	−40 to 150	°C
Storage Temperature	T_{stg}	−50 to 150	°C

(1): Mounted on glass epoxy board. (76.2×114.3×1.6mm: based on EIA/JEDEC standard, 2Layers)

(2): Mounted on glass epoxy board. (76.2×114.3×1.6mm: based on EIA/JEDEC standard, 4Layers)

(For 4Layers: Applying 74.2×74.2mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Pin Voltage	V^+	3.4 to 40	V
EN Pin Voltage	V_{EN}	0 to 40	V
MODE/SYNC Pin Voltage	$V_{MODE/SYNC}$	0 to 40	V
PG Pin Voltage	V_{PG}	0 to 5.5	V
External Clock Input Range	f_{SYNC}	A ver. : 1950 to 2500	kHz
Operating Temperature	T_{opr}	−40 to 125	°C

■ **ELECTRICAL CHARACTERISTICS** $V^+ = V_{EN} = 12V$, $V_{BIAS} = 5V$, $V_{MODE/SYNC} = 12V$, $T_a = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
UNDER VOLTAGE LOCKOUT						
ON Threshold Voltage	V_{T_ON}	$V^+ = L \rightarrow H$	3.1	3.25	3.4	V
OFF Threshold Voltage	V_{T_OFF}	$V^+ = H \rightarrow L$	3.0	3.15	3.3	V
Hysteresis Voltage	V_{HYS}		70	100	-	mV
SOFT START						
Soft Start Time	t_{SS}	$V_{FB\_SOFT} = V_{FB} \times 0.9$	0.5	1	2	ms
OSCILLATOR						
Oscillating Frequency	f_{OSC}	A version	1900	2100	2300	kHz
Oscillating Frequency (Low Frequency Control)	f_{OSC_LOW}	A version	-	800	-	kHz
ERROR AMPLIFIRE						
Feedback Voltage	V_{FB}	$V_{OUT} = 3.3V$	−1.5%	3.3	+1.5%	V
		$V_{OUT} = 5.0V$	−1.5%	5.0	+1.5%	
		$V_{OUT} = ADJ$	−1.0%	0.8	+1.0%	
Input Bias Current	I_{FB}	$V_{OUT} = ADJ$	−0.1	-	0.1	µA
PWM COMPARATOR						
Maximum Duty Cycle	$MAXDUTY$	$V_{FB\_MAXD} = V_{FB} \times 0.9$	100	-	-	%
Minimum OFF Time	$t_{OFF\text{-}min}$		-	100	-	ns
Minimum ON Time	$t_{ON\text{-}min}$		-	50	-	ns
OUTPUT						
High-side SW ON Resistance	R_{ONH}	$I_{SW} = -600mA$	-	0.8	1.6	Ω
Low-side SW ON Resistance	R_{ONL}	$I_{SW} = 600mA$	-	0.4	0.8	Ω
High-side Switching Current Limit	I_{LIMH}		0.85	1.15	1.60	A
Low-side Switching Current Limit	I_{LIML}	SW to GND	0.85	1.15	1.60	A
Auto Discharge Resistance	$R_{AUTODIS}$	$I_{SW} = 10mA$	-	-	100	Ω
High-Side SW Leak Current	I_{LEAKH}	$V^+ - V_{SW} = 40V$	-	-	2	µA
Low-Side SW Leak Current	I_{LEAKL}	$V_{SW} - GND = 40V$	-	-	2	µA
OCP						
COOL DOWN Time	t_{COOL}		-	110	-	ms
ENABLE CONTROL						
EN Pin High Threshold Voltage	V_{THH_EN}	$V_{EN} = L \rightarrow H$	1.6	-	V^+	V
EN Pin Low Threshold Voltage	V_{THL_EN}	$V_{EN} = H \rightarrow L$	0	-	0.5	V
EN Pin Input Bias Current	I_{EN}	$V_{EN} = 12V$	-	0.8	1.8	µA
MODE CONTROL / SYNC						
MODE/SYNC Pin High Threshold Voltage	$V_{THH\_MODE/SYNC}$	$V_{MODE/SYNC} = L \rightarrow H$	1.6	-	V^+	V
MODE/SYNC Pin Low Threshold Voltage	$V_{THL\_MODE/SYNC}$	$V_{MODE/SYNC} = H \rightarrow L$	0	-	0.5	V
MODE/SYNC Pin Input Bias Current	$I_{MODE/SYNC}$	$V_{MODE/SYNC} = 12V$	-	40	60	µA

■ ELECTRICAL CHARACTERISTICS

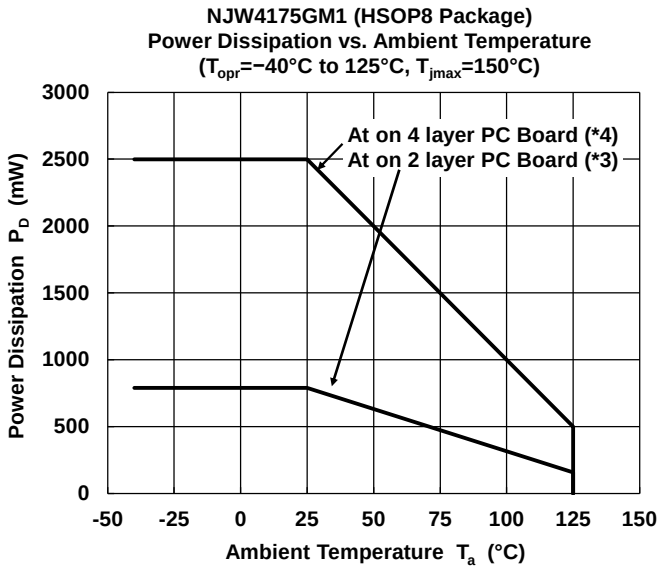
$V^+ = V_{EN} = 12V$, $V_{BIAS} = 5V$, $V_{MODE/SYNC} = 12V$, $T_a = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER GOOD						
High Level Detection Voltage	V_{THH_PG}	Measured at FB pin, Rising	104	110	116	%
Low Level Detection Voltage	V_{THL_PG}	Measured at FB pin, Rising	84	90	96	%
Hysteresis Region	V_{HYS_PG}		-	2	-	%
Power Good ON Resistance	R_{ON_PG}	$I_{PG} = 10mA$	-	100	150	Ω
Leak Current at OFF State	I_{LEAK_PG}	$V_{PG} = 5.5V$	-	-	0.1	μA
GENERAL CHARACTERISTICS						
V+ Pin Quiescent Current 1 (PWM Mode)	I_{DD1}	$V_{MODE/SYNC} = 12V$, R_L = No Load, Not Switching	-	0.5	0.7	mA
V+ Pin Quiescent Current 2 (Light Load Mode)	I_{DD2}	$V_{MODE/SYNC} = 0V$, R_L = No Load, Not Switching	-	20	45	μA
BIAS Pin Quiescent Current (Light Load Mode)	I_{BIAS}	$V_{BIAS} = 5V$, $V_{MODE/SYNC} = 0V$, R_L = No Load, Not Switching	-	65	100	μA
Standby Current	I_{DD_STB}	$V_{EN} = 0V$	-	-	3	μA

■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	VALUE	UNIT
Junction-To-Ambient Thermal Resistance HSOP8-M1	θ_{ja}	2-Layer / 4-Layer 158 (3) / 50 (4)	°C/W
Junction-To-Top of Package Characterization Parameter HSOP8-M1	ψ_{jt}	2-Layer / 4-Layer 28 (3) / 12 (4)	°C/W

■ POWER DISSIPATION vs. AMBIENT TEMPERATURE



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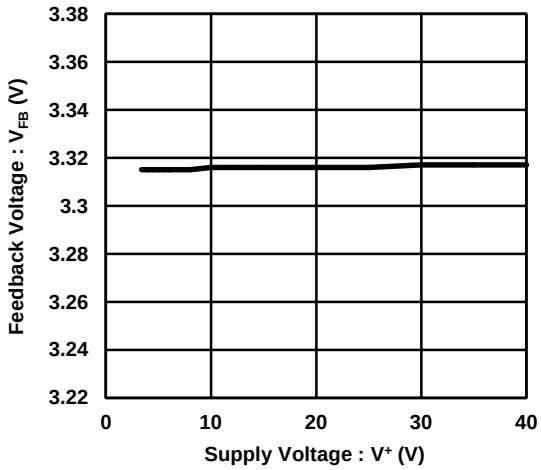
(4): Mounted on glass epoxy board. (76.2×114.3×1.6mm: based on EIA/JEDEC standard, 4Layers)

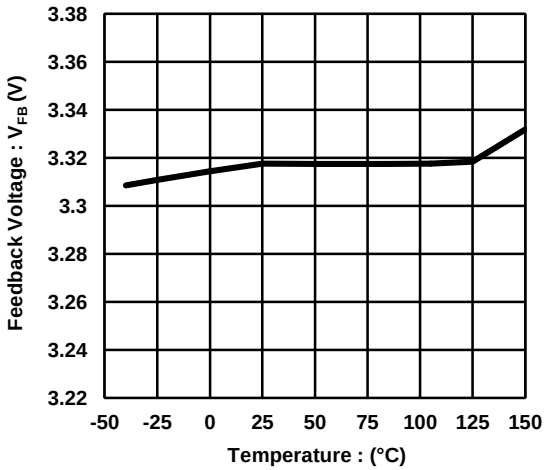
(For 4Layers: Applying 74.2×74.2mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

■ TYPICAL CHARACTERISTICS

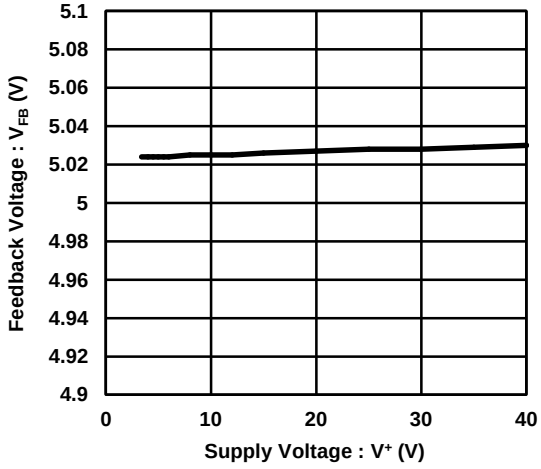
FeedBuck Voltage vs. Supply Voltage
(V_{OUT}=3.3V, T_a=25°C)



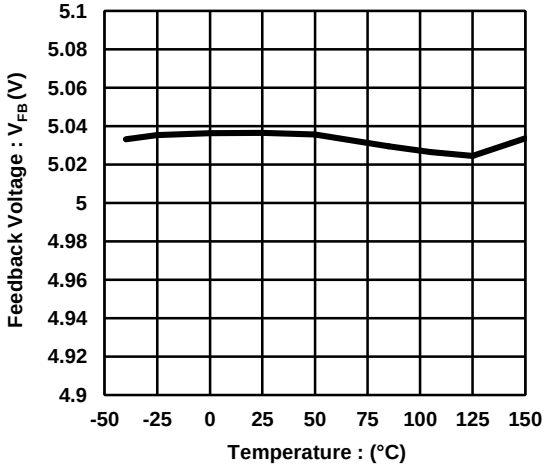
Feedback Voltage vs. Temperature
(V^+=12V, V_{OUT}=3.3V)



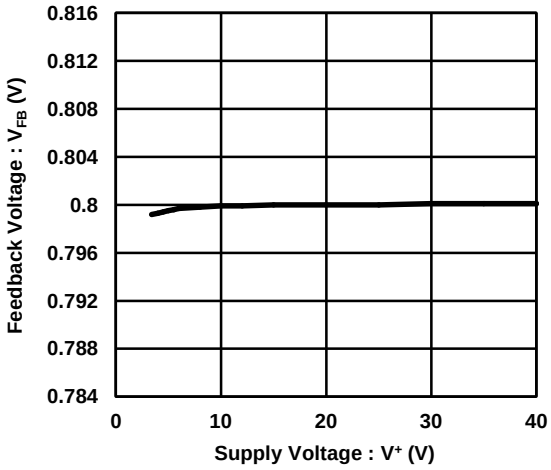
FeedBuck Voltage vs. Supply Voltage
(V_{OUT}=5.0V, T_a=25°C)



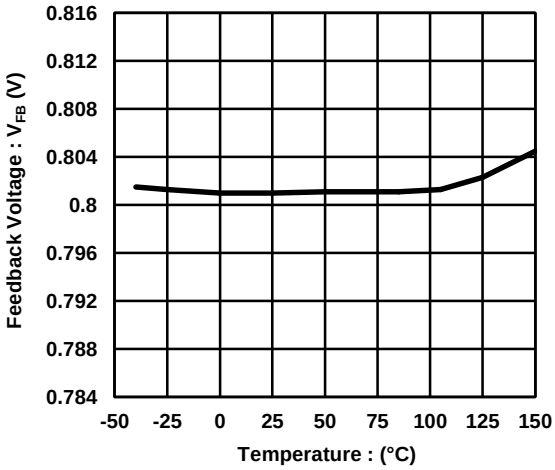
Feedback Voltage vs. Temperature
(V^+=12V, V_{OUT}=5.0V)



FeedBuck Voltage vs. Supply Voltage
(V_{OUT}=ADJ, T_a=25°C)

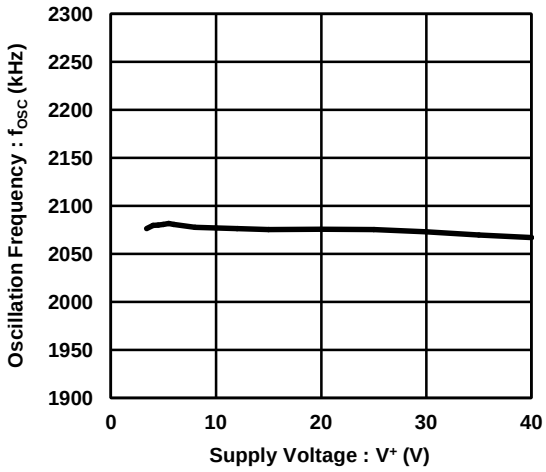


Feedback Voltage vs. Temperature
(V^+=12V, V_{OUT}=ADJ)

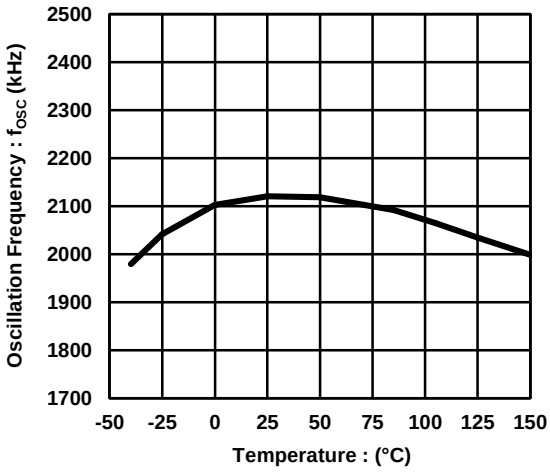


■ TYPICAL CHARACTERISTICS

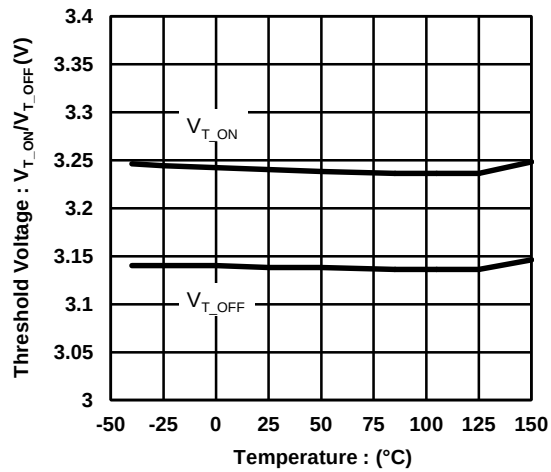
Oscillation Frequency vs. Supply Voltage
(T_a=25°C, A Version)



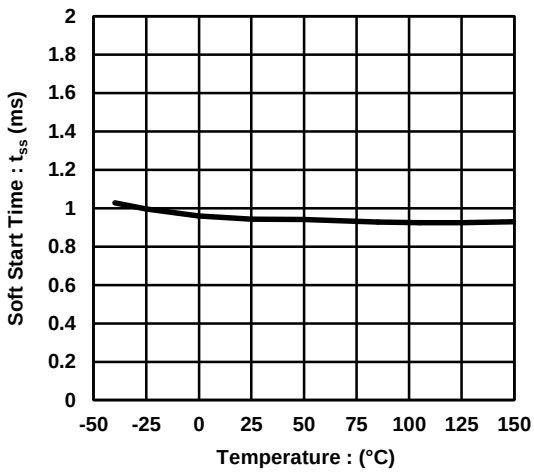
Oscillation Frequency vs. Temperature
(V^+=12V, A Version)



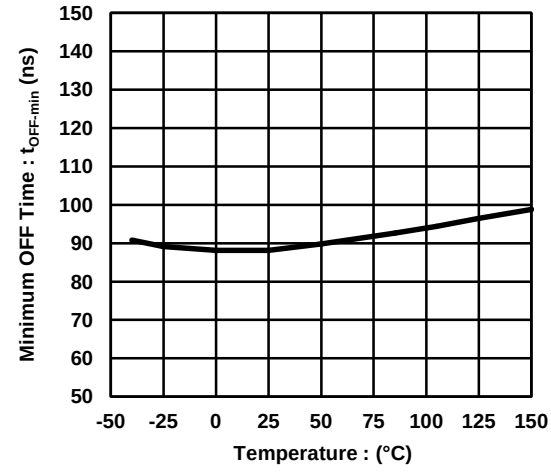
Under Voltage Lockout Voltage vs. Temperature



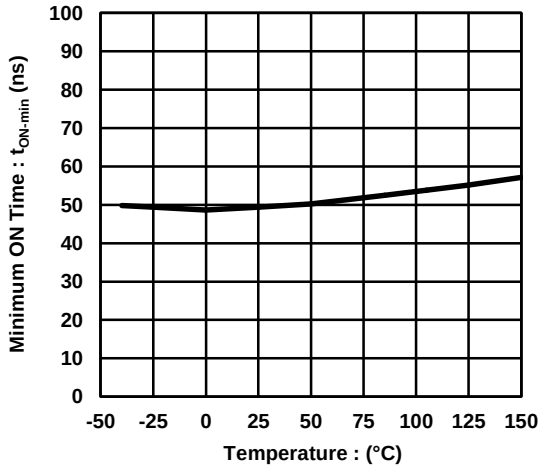
Soft Start Time vs. Temperature
(V^+=12V, V_{FB_SOFT}=V_{FB}×0.9)



Minimum OFF Time vs. Temperature
(V^+=12V)

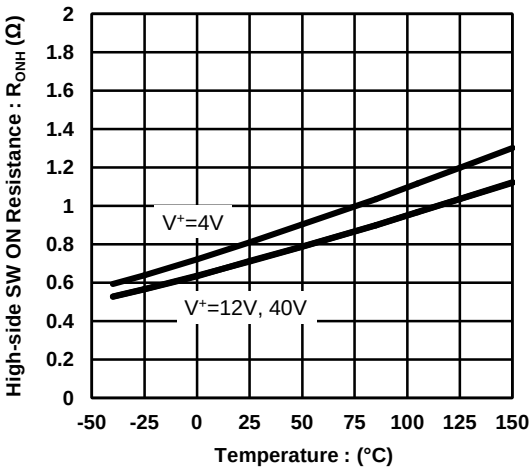


Minimum ON Time vs. Temperature
(V^+=12V)

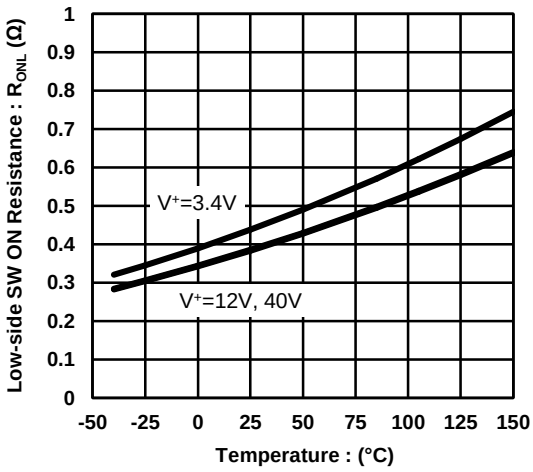


■ TYPICAL CHARACTERISTICS

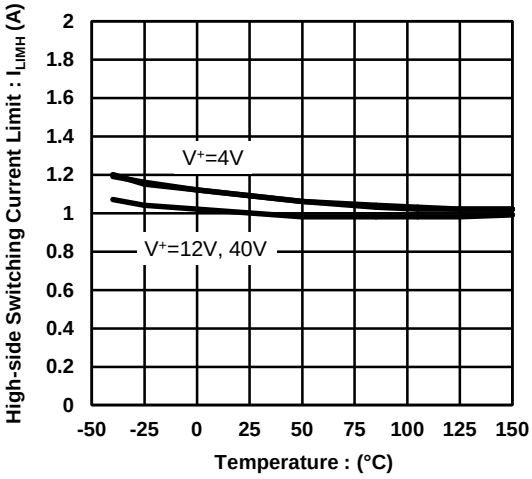
High-side SW ON Resistance vs. Temperature
(I_{SW}=−600mA)



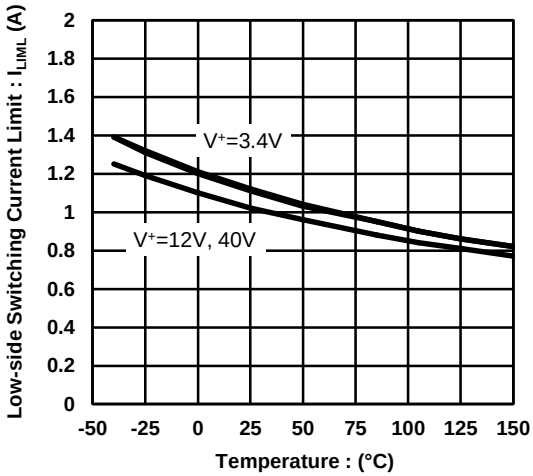
Low-side SW ON Resistance vs. Temperature
(I_{SW}=600mA)



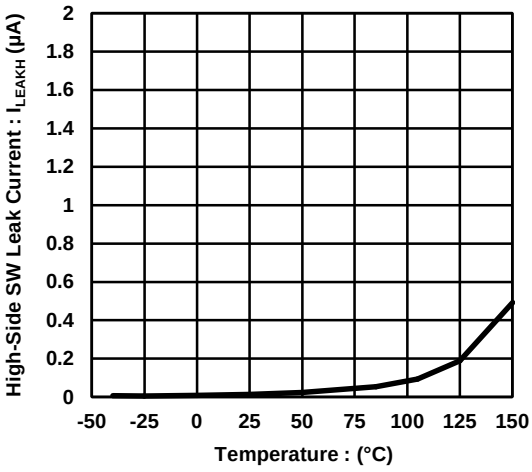
High-side Switching Current Limit vs. Temperature



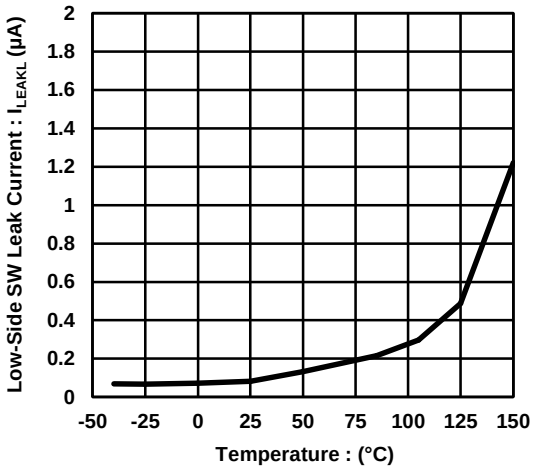
Low-side Switching Current Limit vs. Temperature
(SW to GND)



High-Side SW Leak Current vs. Temperature
(V^+=40V, V_{SW}=0V)

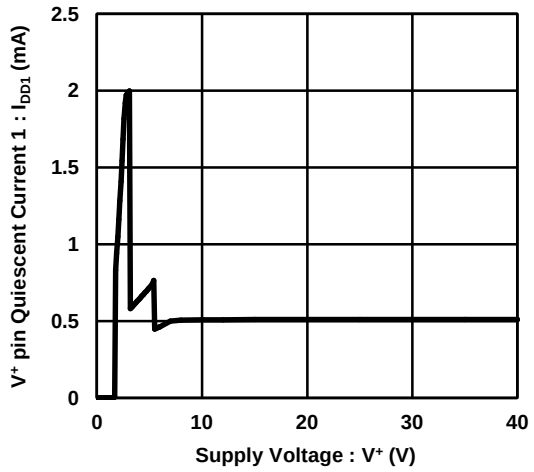


Low-Side SW Leak Current vs. Temperature
(V^+=40V, V_{SW}=40V)

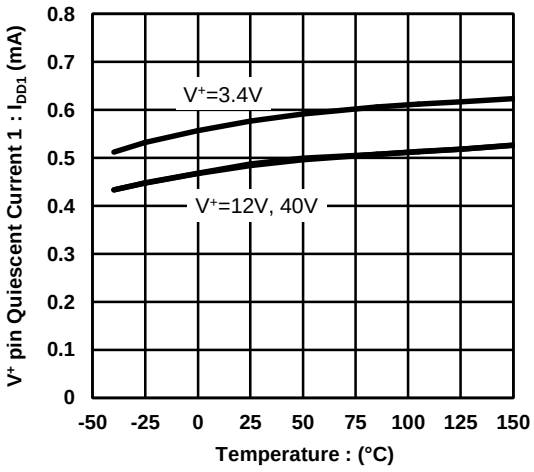


■ TYPICAL CHARACTERISTICS

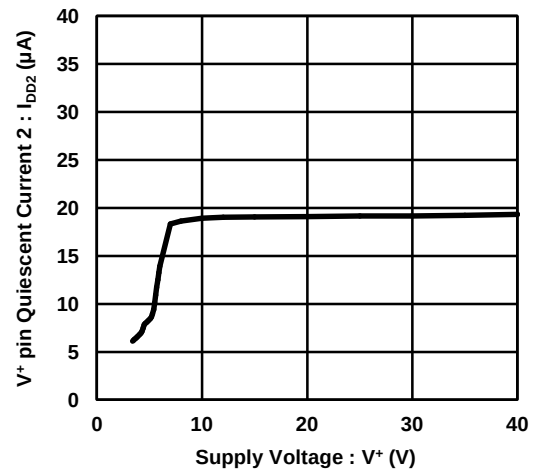
V⁺ pin Quiescent Current 1 vs. Supply Voltage
($V_{MODE/SYNC}$=12V, R_L=No Load, Not Switching, T_a=25°C)



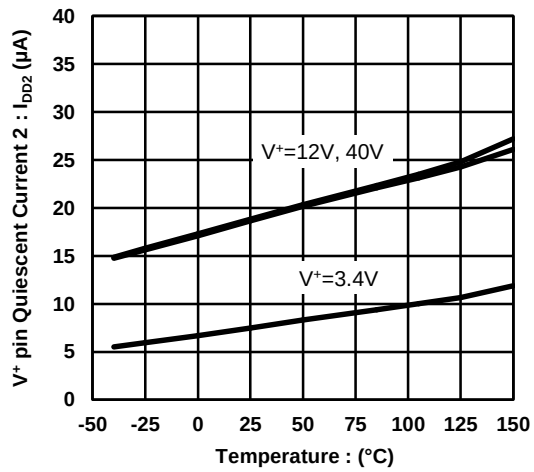
V⁺ pin Quiescent Current 1 vs. Temperature
($V_{MODE/SYNC}$=12V, R_L=No Load, Not Switching)



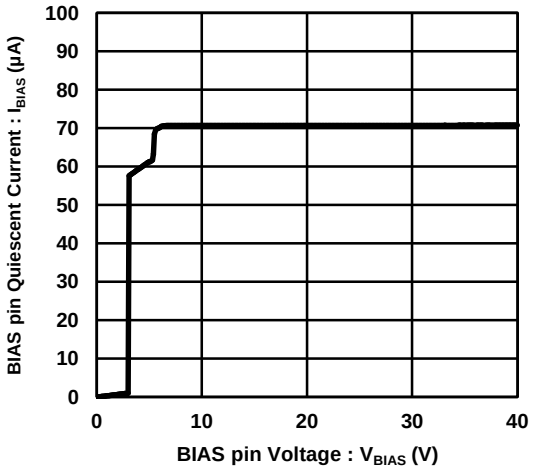
V⁺ pin Quiescent Current 2 vs. Supply Voltage
($V_{MODE/SYNC}$=0V, R_L=No Load, Not Switching, T_a=25°C)



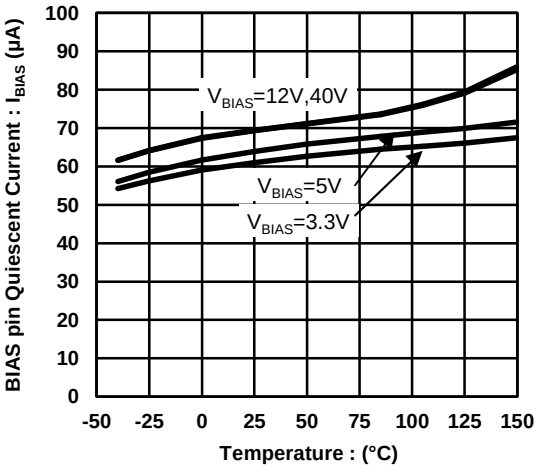
V⁺ pin Quiescent Current 2 vs. Temperature
($V_{MODE/SYNC}$=0V, R_L=No Load, Not Switching)



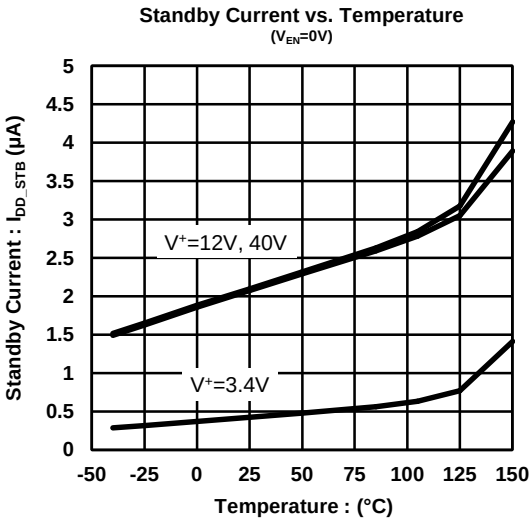
BIAS pin Quiescent Current vs. BIAS pin Voltage
(V^+=12V, $V_{MODE/SYNC}$=0V, R_L=No Load, Not Switching, T_a=25°C)



BIAS pin Quiescent Current vs. Temperature
(V^+=12V, $V_{MODE/SYNC}$=0V, R_L=No Load, Not Switching)



■ TYPICAL CHARACTERISTICS



■ APPLICATION NOTE

PIN DESCRIPTIONS

PIN NAME	PIN NUMBER	FUNCTION
SW	1	Switch Output pin of Power MOSFET
GND	2	GND pin
BIAS	3	Power supply pin to internal regulator
FB	4	Detect Output Voltage pin. In the case of fixed Output Voltage type, Connect to V_{OUT}. In the case of adjustable Output Voltage type, Input the output voltage by dividing it into resistors so that the FB pin voltage becomes V_{FB}.
PG	5	Power Good output pin. An open drain output that goes high impedance when the FB pin voltage is stable around ±10%.
MODE/SYNC	6	Select the Operation mode pin. This pin is pulled down by a resistor. It operates in forced continuous mode at high level and in PWM / PFM switching mode at low level or open. Also, by inputting a clock signal, it operates at an oscillation frequency synchronized with the clock signal.
EN	7	The IC enable pin. This pin is pulled down by a resistor. It operates at the high level and goes into standby at the low level or open.
V+	8	Power supply pin to the IC. Connect an input capacitor near the IC to reduce the impedance of the power supply.
Exposed PAD	–	The back side PAD should be connected to the ground and soldered to the PCB.

Description of each block Features

1. Light Load Mode

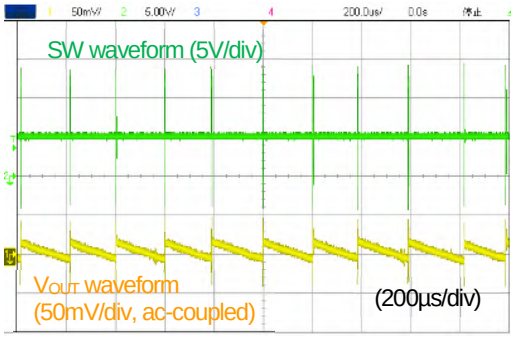
NJW4175 has a light load mode to improve efficiency at light load.
When the load current decreases, the NJW4175 automatically switches from PWM operation to PFM operation. At this time, the IC goes to sleep and the current consumption drops to 20 µA typ. (When the bias function is enabled) Therefore, it is possible to minimize the input current of the application.

To switch the light load mode, the peak of the switch current must be approximately 100mA typ. or less. In the light load mode, the oscillation frequency becomes lower due to PFM operation, so the ripple voltage rises slightly compared to normal operation. Fig.1 shows an example waveform.

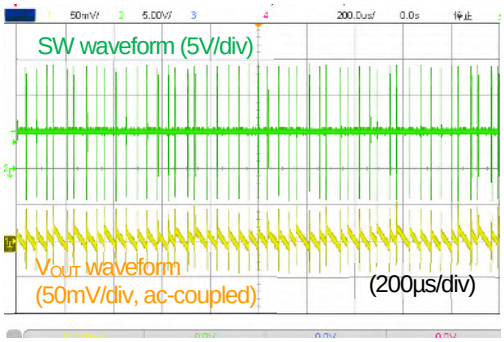
By using a large inductor value, the switching stop period becomes longer, which further improves efficiency at light loads.

Table 1 shows the operation mode selection by the MODE/SYNC pin. Set the MODE / SYNC pin to Low level or open to enable the light load mode. Set the MODE / SYNC pin to High level disables the light load mode.
During external synchronization operation, the light load mode is stopped and operates at the input clock frequency. If the MODE/SYNC pin is set to High level or a CLK signal is input during light load mode operation, the light load mode is switched to normal operation mode.

Changes in the switching frequency under light load affect the ripple frequency. For loads that are sensitive to the effects of ripple, set the MODE/SYNC pin to High level and disable the light load mode.



a) I_{OUT}=1mA



b) I_{OUT}=5mA

Fig.1. Waveform at light load mode

Table 1. Operation mode selection by MODE / SYNC pin

MODE/SYNC PIN	OPERATION MODE	OSCILLATING FREQUENCY
1.6V to V^+	Forced PWM mode operation	Built-in fixed frequency
0V to 0.5V	PWM / PFM switching operation at light load	Built-in fixed frequency
External clock	Forced PWM mode operation	External clock frequency

Description of each block Features (Continued)

2. Basic function

Error amplifier (Error AMP)

A high-precision reference voltage of 0.8V ± 1% is connected to the non-inverting input of the error amplifier block. By inputting the output of the converter to the inverting input (FB pin) of the amplifier, The NJW4175 can easily design applications from an output voltage of 0.8V. The NJW4175 has a lineup of fixed and adjustable output voltage types. The fixed output voltage type has built-in output voltage setting resistors, and products with 3.3V or 5V output can be selected. For the adjustable output voltage type, if the output voltage is 0.8V or higher, the output voltage is set by resistance division. Since the optimum feedback circuit is built in the amplifier block, the application circuit can be configured with the minimum number of external components.

Oscillating circuit (OSC), PWM Comparator (PWM)

The NJW4175 operates with a fixed frequency current mode control scheme. The oscillation frequency differs depending on the version and is set to 2100kHz typ. in the A version. The PWM comparator outputs a PWM signal by feedback of the output voltage and the slope-compensated switching current. The maximum duty is set to 100% to minimize the dropout voltage between input and output. The minimum ON time $t_{ON\text{-}min}$ of NJW4175 is limited to 50ns typ., and the minimum OFF time $t_{OFF\text{-}min}$ is limited to 100ns typ. The ON time of the buck converter circuit is determined by the following formula.

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{OSC}} [s]$$

V_{IN} means the input voltage V_{OUT} means the output voltage and f_{OSC} means oscillation frequency. If the ON time is less than $t_{ON\text{-}min}$, pulse skip operation may be performed to keep the output voltage stable.

Power MOSFET

The built-in power MOSFET supplies power to the inductor. The overcurrent protection limits the switching current that the power MOSFET can supply to I_{LIMH} = 0.85A min.

Power supply, GND (V+, GND)

With the switching operation, a current corresponding to the frequency flows through the IC. If the power supply line impedance is high, the power supply becomes unstable and the IC performance will not be fully exhibited. Insert a bypass capacitor near the V+ pin and GND pin to decrease the high frequency impedance.

Description of each block Features (Continued)

3. Protection circuit, additional function

Under voltage lockout (UVLO)

If the power supply voltage is low, the UVLO circuit stops the IC operation, and when the power supply voltage is 3.25V typ. or higher, the UVLO circuit is released and the IC starts operating. A hysteresis voltage width of 100 mV typ. is provided to prevent UVLO release and chattering of operation.

Soft start

The soft start function gradually raises the output voltage of the converter to the set value. The soft start time is 1ms typ., which is defined as the time until the error amplifier reference voltage reaches 0 to V_{FB} x 0.9V. (Fig.2) The soft start circuit operates after UVLO release and recovery from thermal shutdown. It is controlled to a low oscillation frequency until the FB pin becomes V_{FB} x 0.81V, and operates at 800kHz typ.

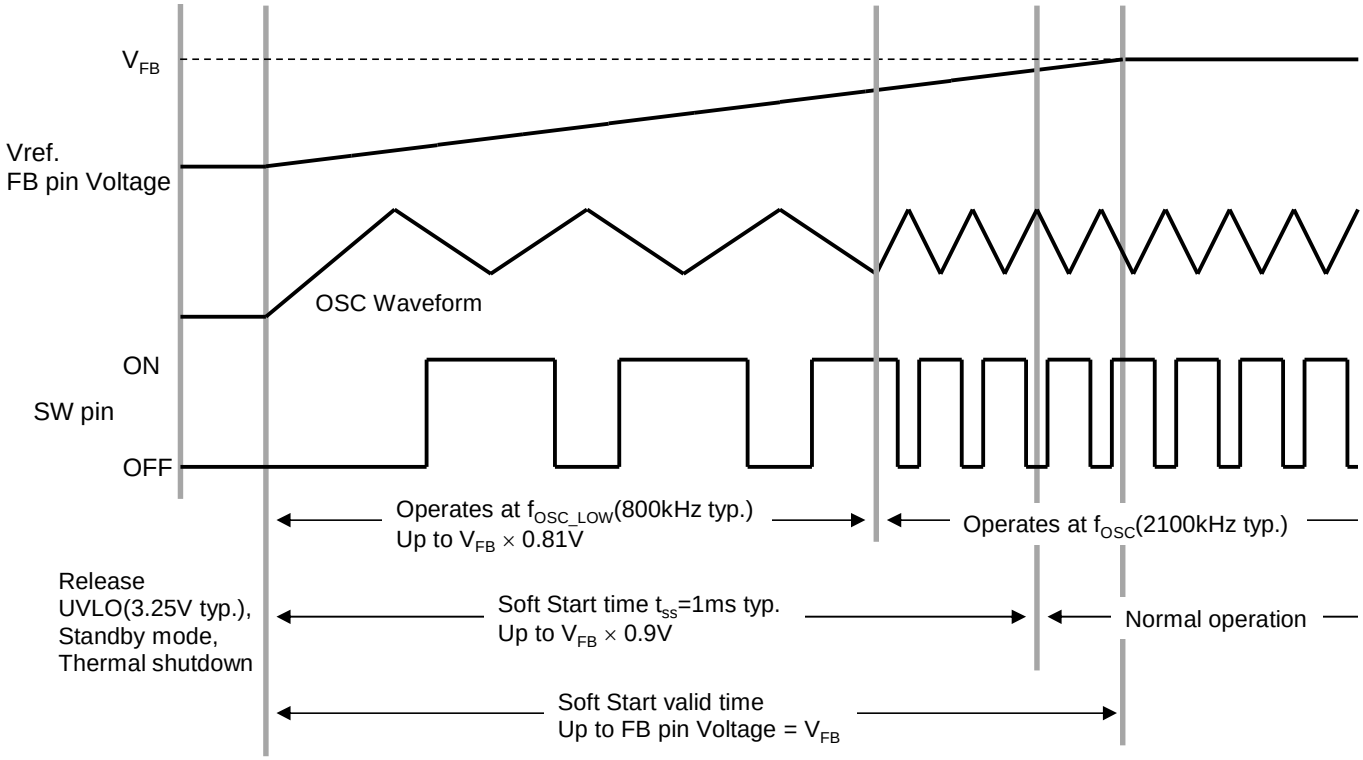


Fig.2 soft start timing chart

Description of each block Features (Continued)

Over current protection (OCP)

The NJW4175 has a built-in Hiccup overcurrent protection function. It reduces heat generation during overload and automatically restores the output voltage of the switching regulator when recovering from an overcurrent state. Fig.3 shows the OCP timing chart. When a current higher than I_{LIMH} flows through the built-in power MOSFET, the OCP turns off the power MOSFET and restores the switching operation in the next cycle. When the FB pin voltage becomes V_{FB} x 0.62V or less and overcurrent detection is continued for 128 pulses, the switching operation is stopped. After that, after a cool down time t_{COOL} of 110ms typ., It will be restarted by soft start.

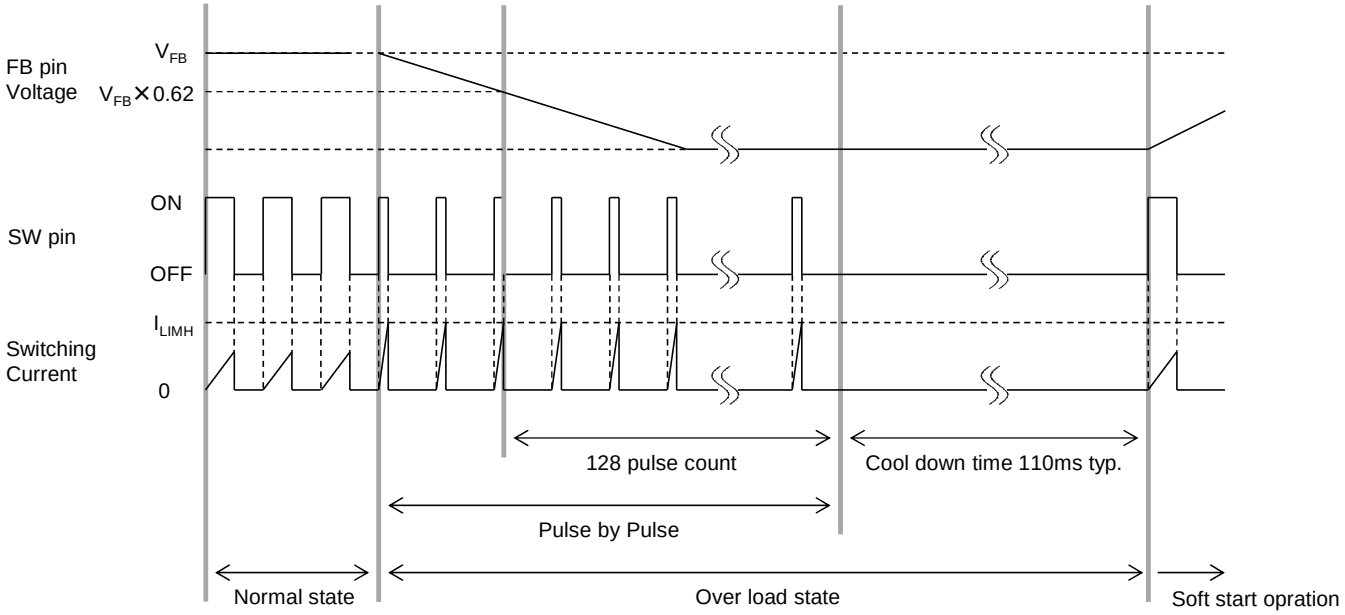


Fig.3 OCP timing chart

Thermal shutdown (TSD)

When the junction temperature exceeds 165°C *, the switching operation is stopped by thermal shutdown. When the junction temperature decrease below 145°C *, the switching operation by soft start starts. The thermal shutdown function is a protection circuit to prevent thermal runaway of the IC at high temperatures, not to supplement improper thermal design. It is recommended to set a sufficient margin for the junction temperature rating (150°C max.) of the IC. (*Reference value)

Standby function

By setting the EN pin voltage to 0.5V max. or less, the NJW4175 will stop functioning and enter the standby state. It is pulled down by a resistor inside the IC, and shifts to standby mode even when the pin is open. When not using the standby function, connect the EN pin to V^+.

Bias function

The NJW4175 has a function to supply power from the V_{OUT} to the internal regulator to improve efficiency.
When the output voltage is 3.3V or higher, efficiency is improved by connecting the BIAS pin to VOUT and supplying power to the internal regulator.
Connect the BIAS pin to GND when the output voltage is less than 3.3V or when the bias function is not used.

Description of each block Features (Continued)

External clock synchronization

By inputting a square wave to the MODE/SYNC pin, the oscillation frequency of the NJW4175 can be synchronized with the external clock frequency. Square waves must meet the specifications in Table 2. The switching operation during external synchronization triggers the rising edge of the input signal. In addition, at the switching point between standby state and asynchronous operation and external synchronous operation, a delay time of about 5µs to 10µs is set to prevent malfunction as shown in Fig.4.

Table 2. Square wave input to MODE/SYNC pin.

	CONDITION (A version)
Input frequency	1950kHz to 2500kHz
Duty cycle	40% to 60%
Voltage amplitude	1.6V or higher (High level) 0.5V or less (Low level)

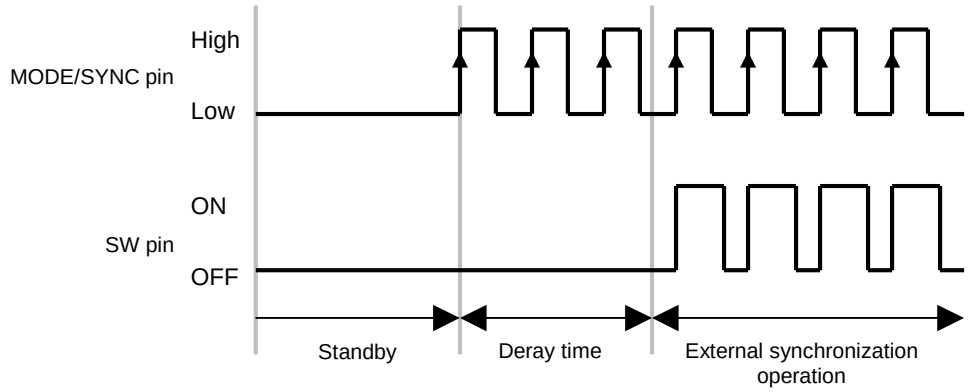


Fig.4 switching operation by external clock

Power Good, Over voltage protection

It monitors the output status and outputs a signal from the open drain PG pin. When the FB pin is stable at ± 10% of the feedback voltage, the Power Good output is high impedance. When the Power Good output is at Low level, it indicates that the FB pin is out of the set voltage. High level Power Good detection doubles as an overvoltage protection function. If the FB pin voltage exceeds the High level detection voltage due to an application error, the power MOSFET is turned off with the highest priority. In order to prevent the malfunction of the Power Good output, a hysteresis of 2% typ. and a delay time of about 20µs to 30µs are provided for the voltage change of the FB pin.

Application Information

Inductor (L)

Since a large current flows through the inductor, it is necessary to have a current capacity that does not saturate. Since the NJW4175 has built-in phase compensation, the optimum L value is determined by the output voltage. Table 3 shows an example of inductor settings.

$$\frac{V_{IN}}{1.45}\times(D_{ON}-0.34) < L < \frac{V_{IN}}{2.42}\times(D_{ON}+2.68)\ [\mu H]$$

D_{ON} : On duty cycle, V_{OUT}/V_{IN}

Table 3. Inductor setting example

OUTPUT VOLTAGE [V]	INDUCTOR : L [μH]	PARTS EXAMPLE
3.3	3.3	LQH44PH_PR (Murata) CLF5030NI-D (TDK)
5.0	4.7	
8.0	6.8	
12	10	
15	10	

As the L value decreases, as shown in Fig.5, the peak current with respect to the output current increases and the conversion efficiency tends to decrease. It should also be noted that the output current is limited because the overcurrent limit is likely to operate. The peak current (I_{PK}) is calculated by the following formula.

$$L=\frac{(V_{IN}-V_{OUT})\times V_{OUT}}{\Delta I_L \times V_{IN}\times f_{OSC}}\ [H]$$

$$I_{PK}=I_{OUT}+\frac{\Delta I_L}{2}\ [A]$$

The optimum value will differ depending on the application specifications, parts, etc., so make the final adjustment on the actual machine.

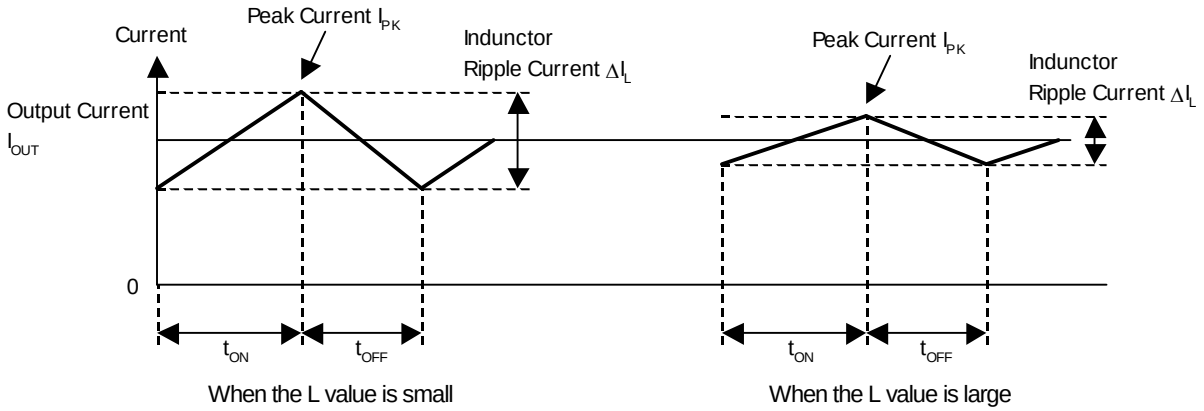


Fig.5 Inductor current status (continuous conduction mode)

Application Information (Continued)

Input capacitor (C_{IN})

A transient current flows through the input of the switching regulator according to the frequency. If the power supply line impedance is high, the Input voltage will fluctuate and the NJW4175 performance will not be fully exhibited. Therefore, insert the input capacitor as close to the IC as possible. Ceramic capacitors are suitable for the input capacitors of NJW4175. The input effective current can be expressed by the following formula.

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}} [A]$$

The above formula is maximized when $V_{IN} = 2 \times V_{OUT}$, and the result at that time is $I_{RMS} = I_{OUT\,(MAX)} \div 2$.
When selecting an input capacitor, evaluate it in the application and use one with a sufficient margin.

Output capacitor (C_{OUT})

The output capacitor stores the power from the inductor and stabilizes the supply voltage to the output. The NJW4175 has phase compensation set so that low ESR output capacitors can be used, and the ceramic capacitors are best. Table 4 shows an example of setting the output capacitor.

Table4. Output capacitor setting example

OUTPUT VOLTAGE [V]	OUTPUT CAPACITOR : C_{OUT} [µF]	PARTS EXAMPLE
3.3	≥ 22µF/10V	GCM31CR71A226KE02L
5.0	≥ 10µF/16V	GCM21BC71C106KE36L
8.0	≥ 10µF/25V	GCM31CC71E106KA03L
12	≥ 10µF/25V	GCM31CC71E106KA03L
15	≥ 10µF/25V	GCM31CC71E106KA03L

Use an output capacitor with a capacity larger than the values shown in Table 4. Since the capacity of ceramic capacitors decreases due to DC voltage application and temperature changes, check the characteristics on the spec sheet.

When selecting an output capacitor, it is necessary to consider the characteristics of ESR (Equivalent Series Resistance), ripple current, and rated voltage. In the case of a low ESR type capacitor, the ripple voltage can be lowered. The output ripple voltage can be expressed by the following formula.

$$V_{ripple(p-p)} = \Delta I_L \times \left(ESR + \frac{1}{8 \times f_{OSC} \times C_{OUT}} \right) [V]$$

The effective value (I_{rms}) of the ripple current flowing through the capacitor can be expressed by the following formula.

$$I_{rms} = \frac{\Delta I_L}{2\sqrt{3}} [Arms]$$

Application Information (Continued)

Output voltage setting

The output voltage V_{OUT} of NJW4175GM1-33A and NJW4175GM1-05A is fixed at 3.3V and 5V, respectively. For NJW4175GM1-JA, the output voltage V_{OUT} is determined by the ratio of the output voltage setting resistor R1 and R2 as shown in the formula below. If the resistor value is small, the reactive current increases, which affects the efficiency at light load. Use a large resistor value for R1 and R2 to reduce loss at light loads.

$$V_{OUT} = \left(\frac{R2}{R1} + 1 \right) \times V_{FB} \ [V]$$

R2 and compensation capacitor C_{FB} generate a zero point (f_{Z1}) that compensates for the phase of the switching regulator as shown in Fig.6. The zero point can be expressed by the following formula.

$$f_{Z1} = \frac{1}{2 \times \pi \times R2 \times C_{FB}} \ [Hz]$$

Set f_{Z1} to about 70kHz as a guide. Table 5 shows an example of setting the output voltage setting resistor and compensation capacitor.

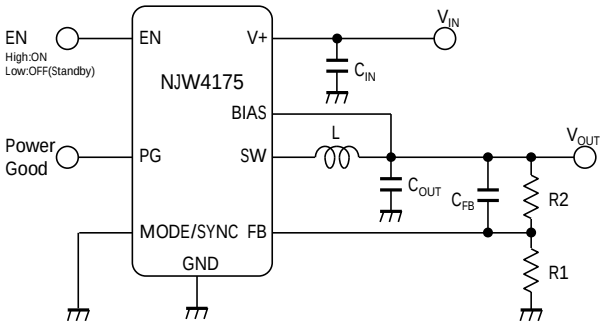


Fig.6 Circuit example of variable output voltage type

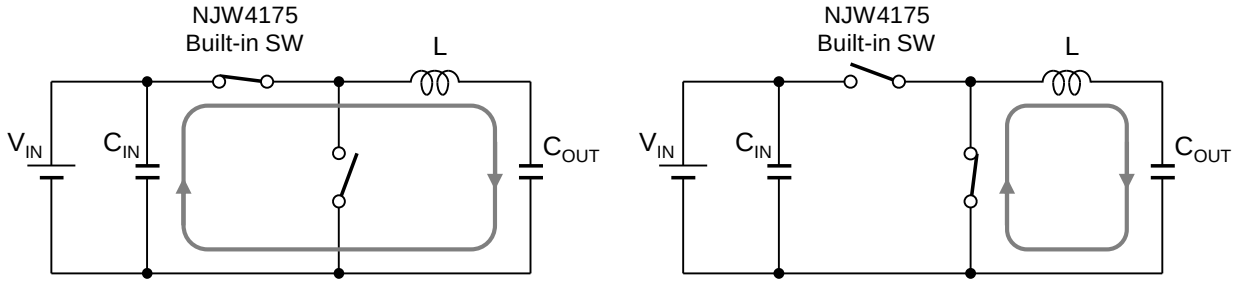
Table 5. Output voltage setting resistor, compensation capacitor setting example

OUTPUT VOLTAGE [V]	R1 [kΩ]	R2 [kΩ]	C_{FB} [pF]
3.3	237	750	3
5.0	154	820	3
8.0	82	750	3
12	56	787	3
15	51	910	2

Application Information (Continued)

Board layout

The switching regulator supplies power to the output by charging and discharging the inductor. The layout of the board (PCB) is important because the current flows according to the oscillation frequency. The high current path should be thick and short to minimize the loop area. Fig.7 shows the current loop in the buck converter circuit. Especially, should lay out high priority the loop of CIN-SW-GND that occurs rapid current change in the switching. It is effective in reducing spike noise generated by parasitic inductors.



(a) Buck Converter SW. ON (b) Buck Converter SW. OFF

Fig.7. Current Loop at Buck Converter

The GND line should be connected single point ground, separating the power system and signal system. Also, keep the voltage detection feedback line as far away from the inductor as possible. Since this line has high impedance, it may be affected by noise due to leakage flux from the inductor. Fig.8 shows an example of wiring in a buck converter circuit, and Fig.9 shows an example of layout.

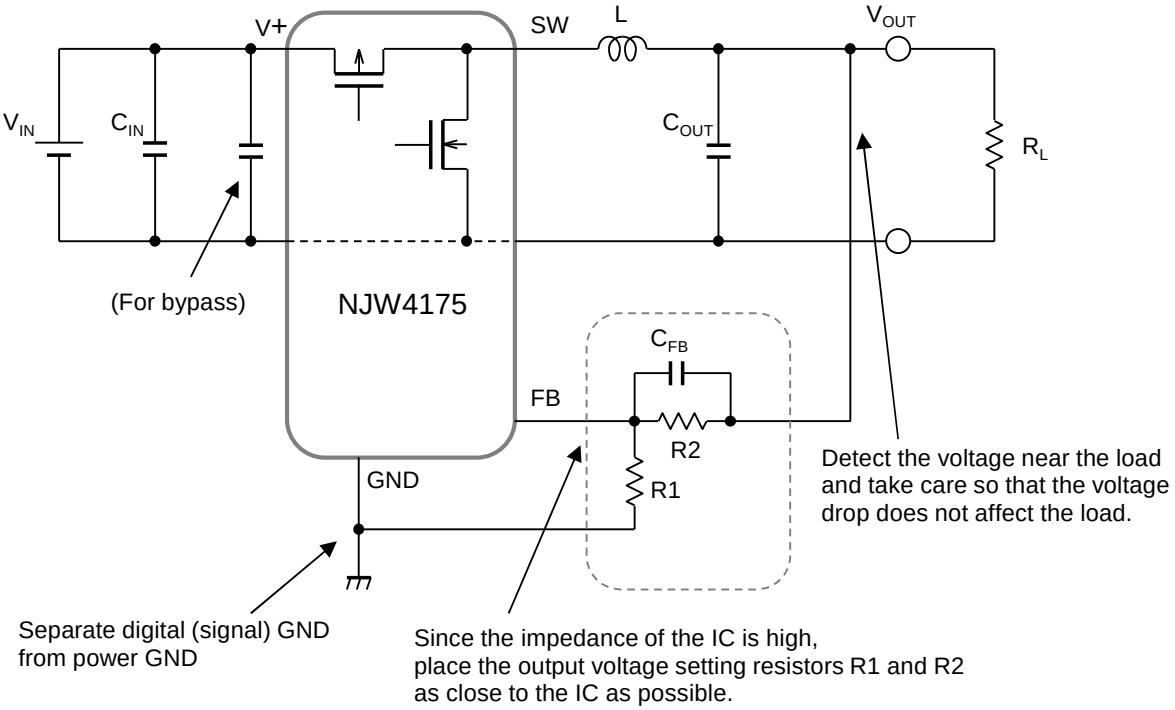


Fig.8. Wiring example of buck converter

Application Information (Continued)

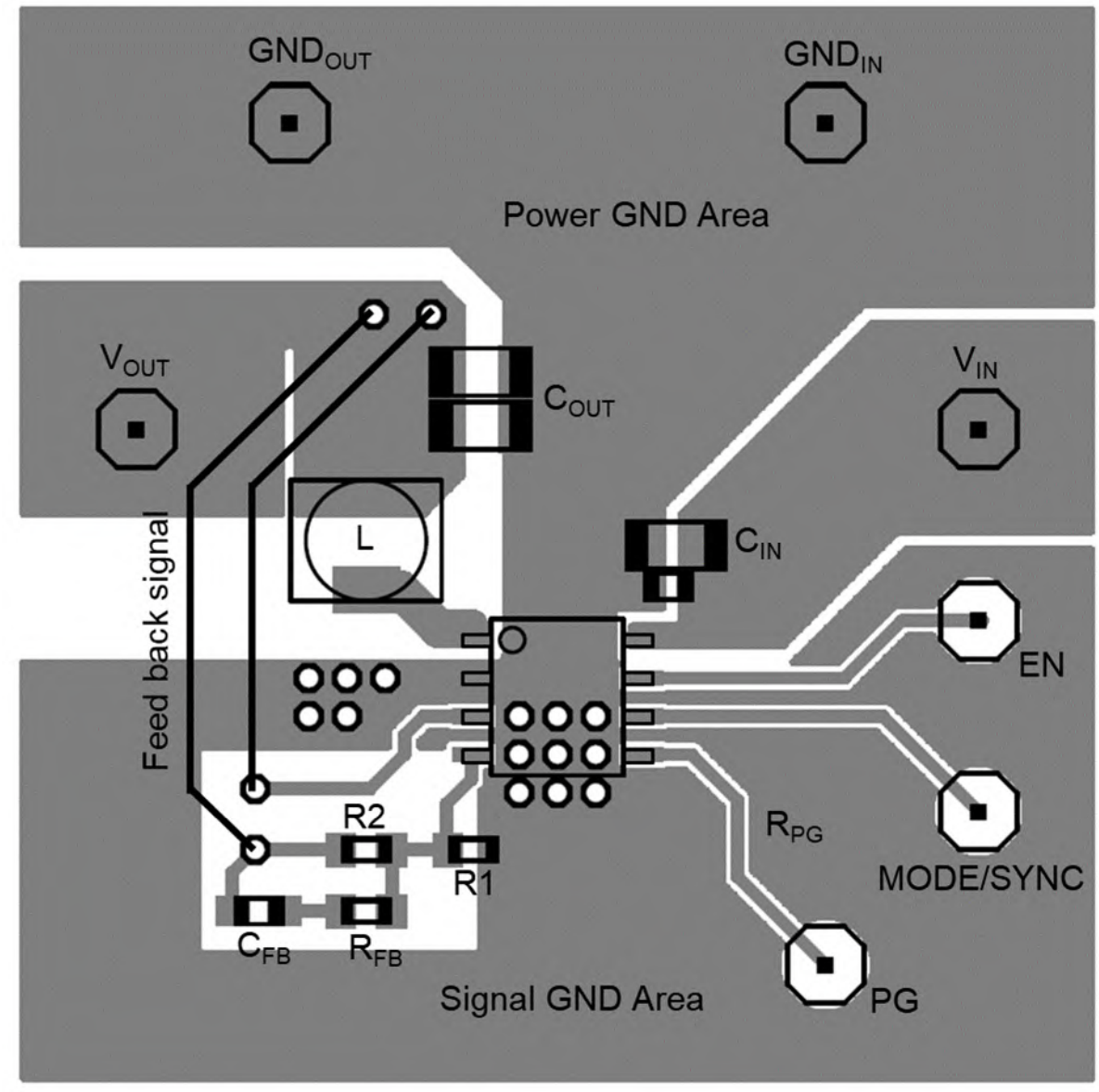


Fig.9. Layout example (Top pattern)

Calculation of package power

Most of the step-down circuit loss is caused by the NJW4175 power MOSFETs that perform the switch operation. Therefore, consider the loss of NJW4175 using the following formula as a guide.

Input power	: $P_{IN} = V_{IN} \times I_{IN}$	[W]
Output power	: $P_{OUT} = V_{OUT} \times I_{OUT}$	[W]
NJW4175 power dissipation	: $P_{LOSS} = P_{IN} - P_{OUT}$	[W]

Where,

V_{IN}	: Input voltage of buck converter	I_{IN}	: Input current of buck converter
V_{OUT}	: Output voltage of buck converter	I_{OUT}	: Output current of buck converter

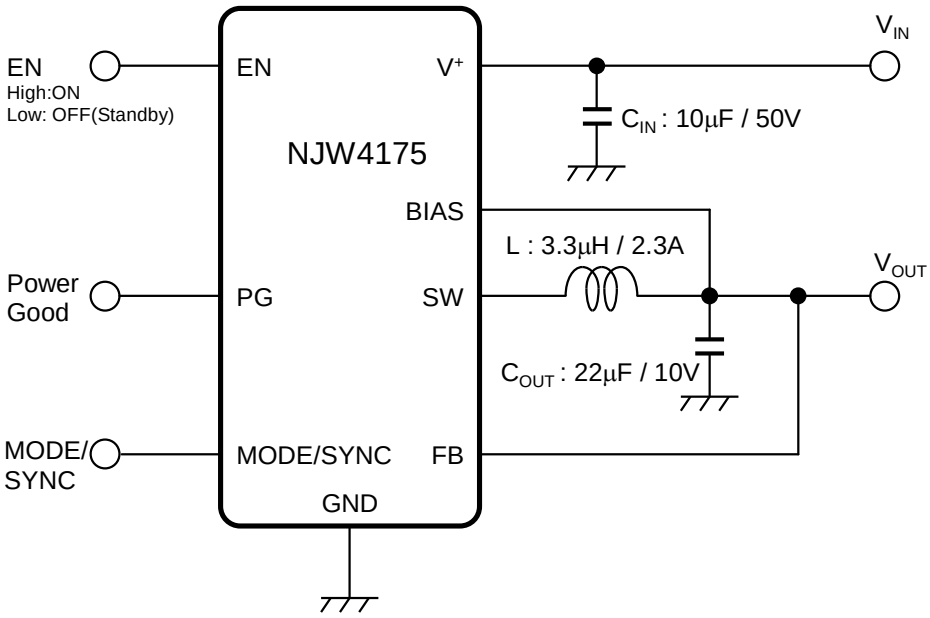
Conversion efficiency η is calculated by the following formula.

$$\eta = (P_{OUT} \div P_{IN}) \times 100 \ [\%]$$

Consider the temperature derating for the calculated power consumption P_{LOSS}. Check if it fits within the rating by referring to the "Power Dissipation vs. Ambient Temperature" characteristic example.

Application design example (V_{OUT} = 3.3V)

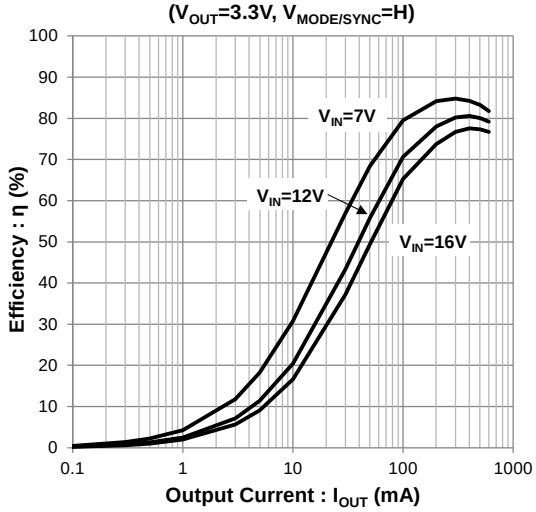
IC	: NJW4175GM1-33A
Input Voltage	: V_{IN} = 12V
Output Voltage	: V_{OUT} = 3.3V
Output Current	: I_{OUT} = 600mA
Oscillating frequency	: f_{OSC} = 2100kHz



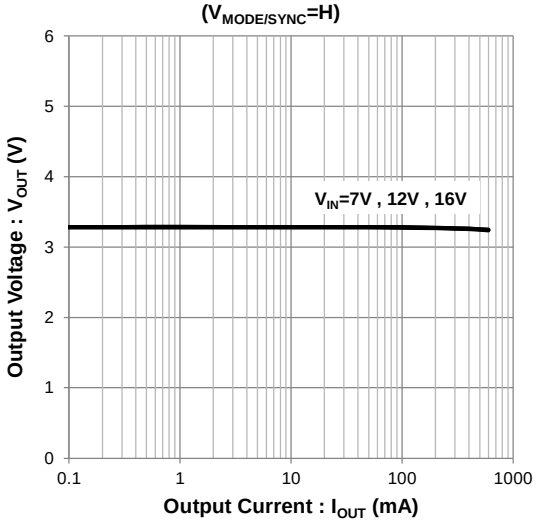
SYMBOL	Qty.	PART NUMBER	DESCRIPTION	MANUFACTURE
IC	1	NJW4175GM1-33A	Internal 600mA MOSFET SW.REG. IC	New JRC
L	1	LQH44PH3R3MPR	Inductor 3.3µH, 2.3A	Murata
C_{IN}	1	UMK325BJ106MM	Ceramic Capacitor 3225 10µF, 50V, X5R	Taiyo Yuden
C_{OUT}	1	GCM31CR71A226KE02L	Ceramic Capacitor 3216 22µF, 10V, X7R	Murata

Application characteristics (V_{OUT} = 3.3V)

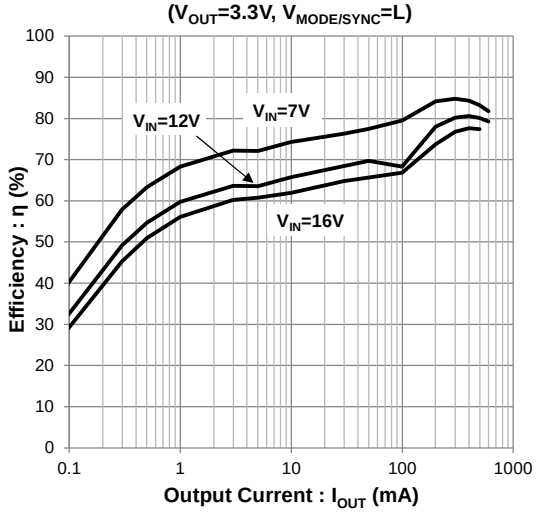
Efficiency vs. Output Current
(V_{OUT}=3.3V, $V_{MODE/SYNC}$=H)



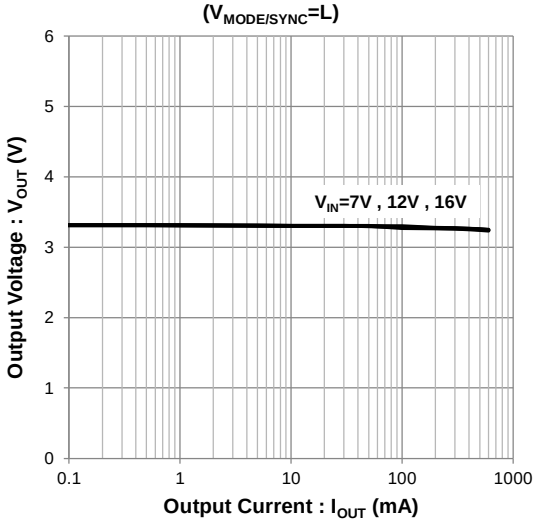
Load Regulation
($V_{MODE/SYNC}$=H)

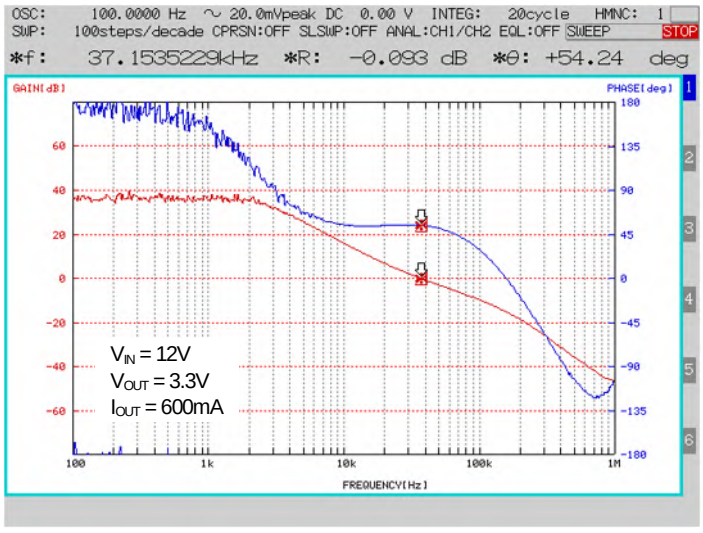


Efficiency vs. Output Current
(V_{OUT}=3.3V, $V_{MODE/SYNC}$=L)



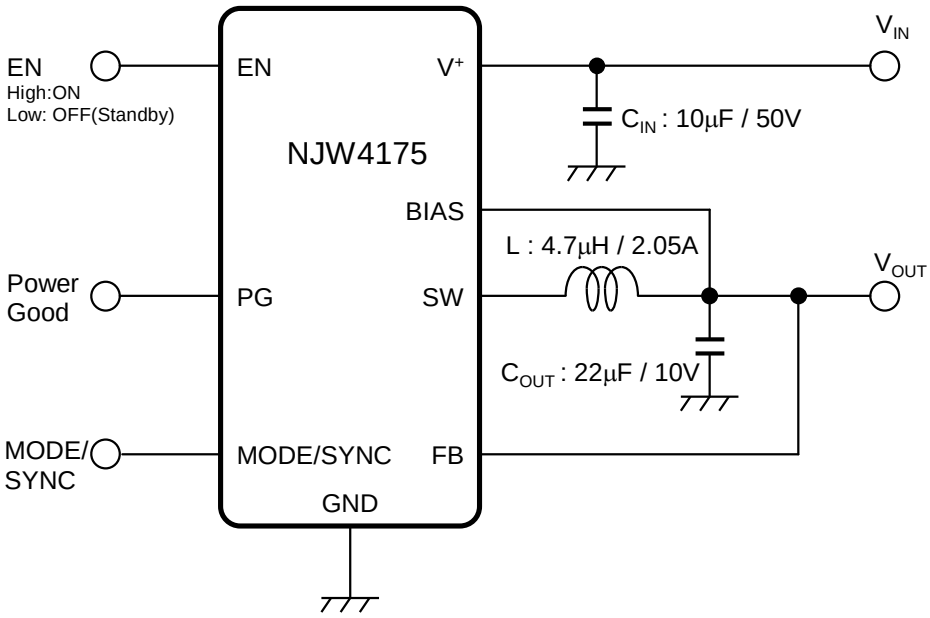
Load Regulation
($V_{MODE/SYNC}$=L)





Application design example (V_{OUT} = 5V)

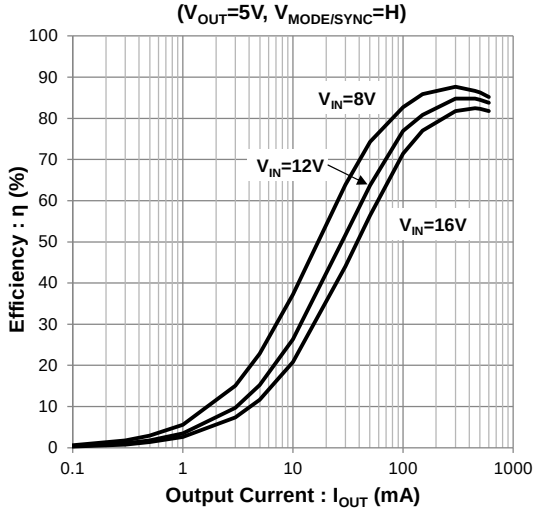
IC	: NJW4175GM1-05A
Input Voltage	: V_{IN} = 12V
Output Voltage	: V_{OUT} = 5V
Output Current	: I_{OUT} = 600mA
Oscillating frequency	: f_{OSC} = 2100kHz



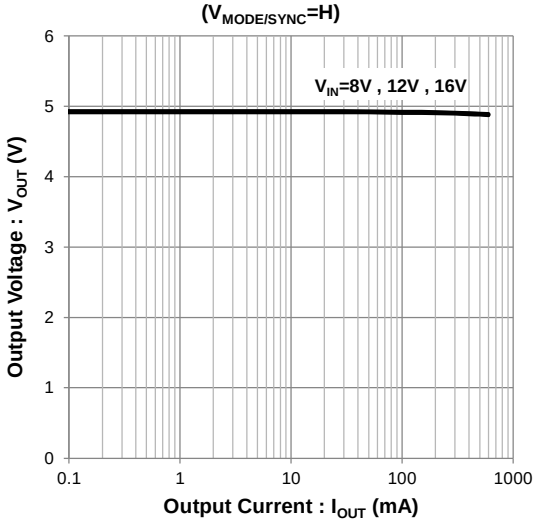
SYMBOL	Qty.	PART NUMBER	DESCRIPTION	MANUFACTURE
IC	1	NJW4175GM1-05A	Internal 600mA MOSFET SW.REG. IC	New JRC
L	1	LQH44PH4R7MPR	Inductor 4.7µH, 2.05A	Murata
C_{IN}	1	UMK325BJ106MM	Ceramic Capacitor 3225 10µF, 50V, X5R	Taiyo Yuden
C_{OUT}	1	GCM31CR71A226KE02L	Ceramic Capacitor 3216 22µF, 10V, X7R	Murata

Application characteristics (V_{OUT} = 5V)

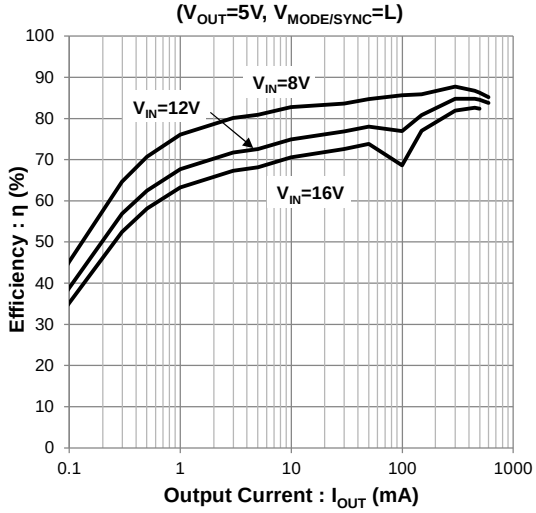
Efficiency vs. Output Current
(V_{OUT}=5V, $V_{MODE/SYNC}$=H)



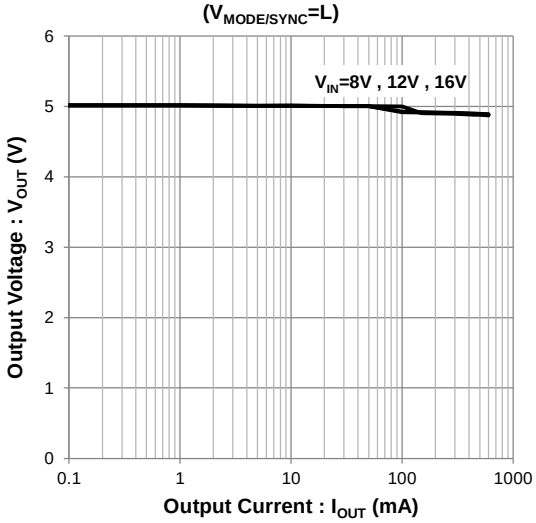
Load Regulation
($V_{MODE/SYNC}$=H)

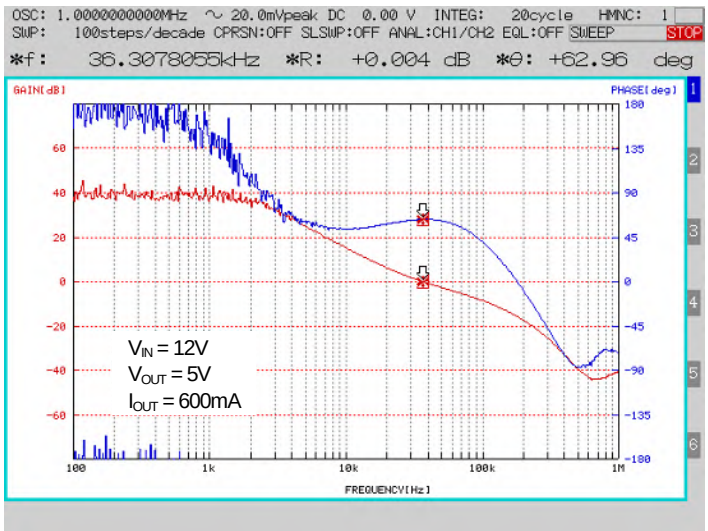


Efficiency vs. Output Current
(V_{OUT}=5V, $V_{MODE/SYNC}$=L)



Load Regulation
($V_{MODE/SYNC}$=L)

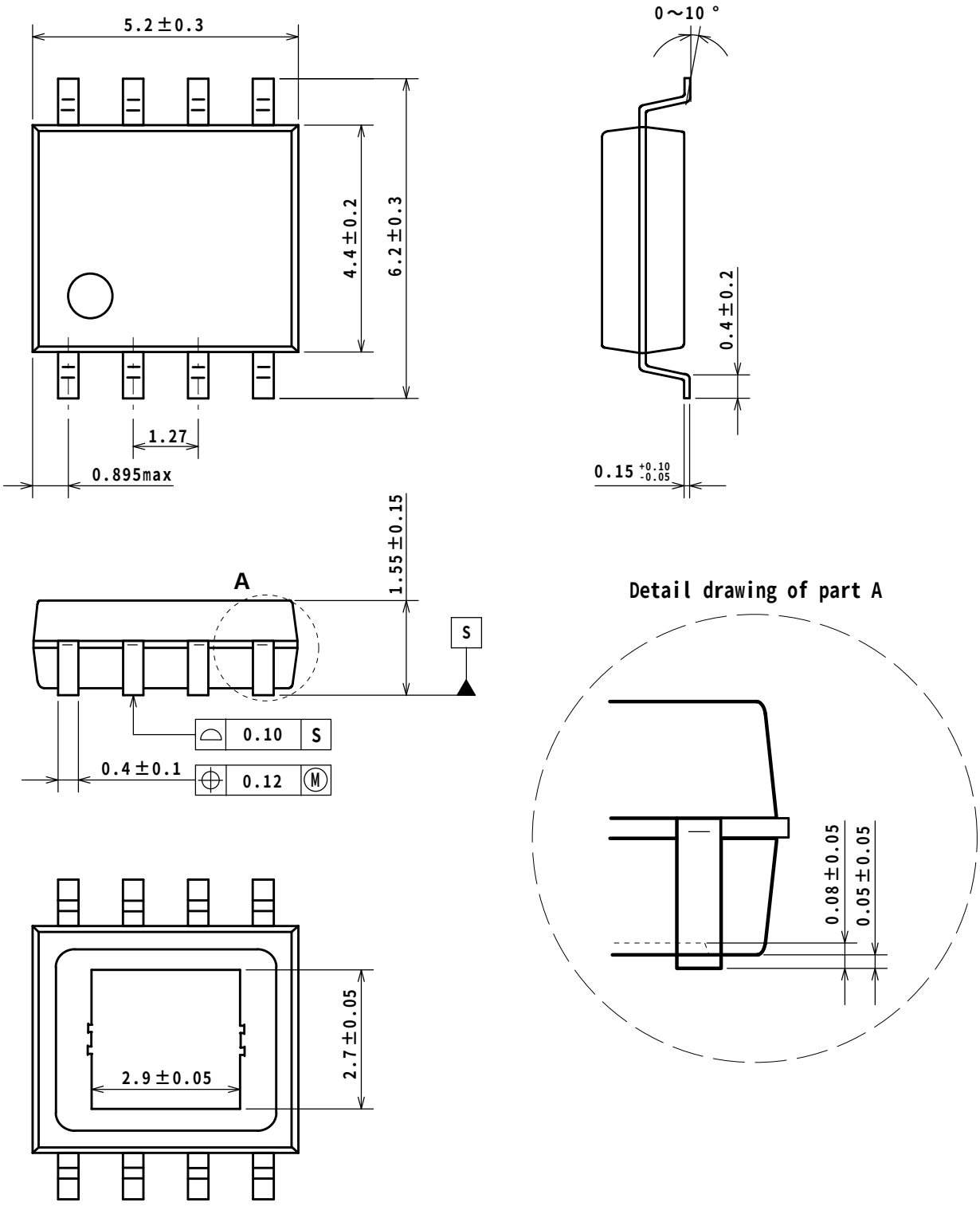




HSOP8

Unit: mm

■PACKAGE DIMENSIONS



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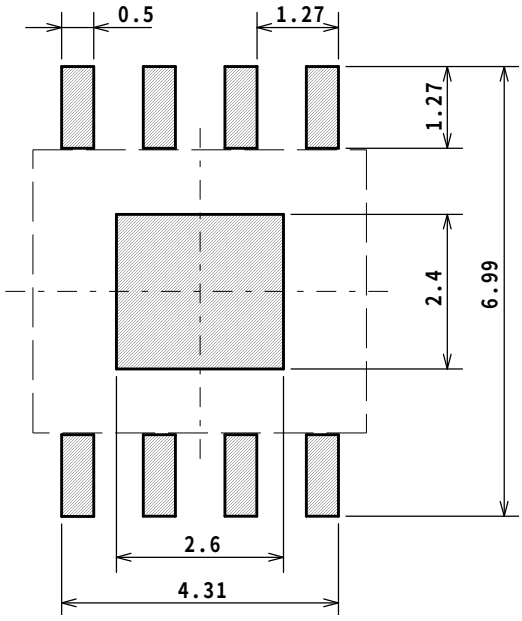
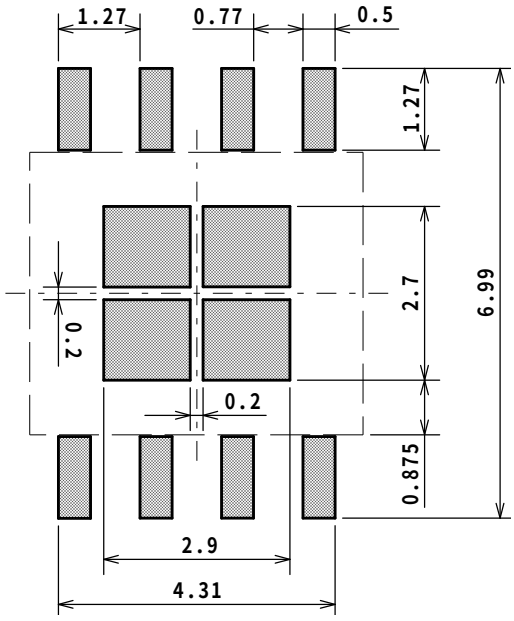
Unit: mm

■EXAMPLE OF SOLDER PADS DIMENSIONS



<Solder pattern>



<Metal mask>

<Instructions for mounting>

Please note the following points when you mount HSOP-8 package IC because there is a standoff on the backside electrode.

(1) Temperature profile of lead and backside electrode.

It is necessary that both re-flow temperature profile of lead and backside electrode are higher than preset temperature.

When solder wet temperature is lower than lead/backside electrode temperature, there is possibility of defect mounting.

(2) Design of foot pattern / metal mask

Metal mask thickness of solder pattern print is more than 0.13mm.

(3) Solder paste

The mounting was evaluated with following solder paste, foot pattern and metal mask.

Because mounting might be greatly different according to the manufacturer and the product number even if the solder composition is the same.

We will strongly recommend to evaluate mounting previously with using foot pattern, metal mask and solder paste.

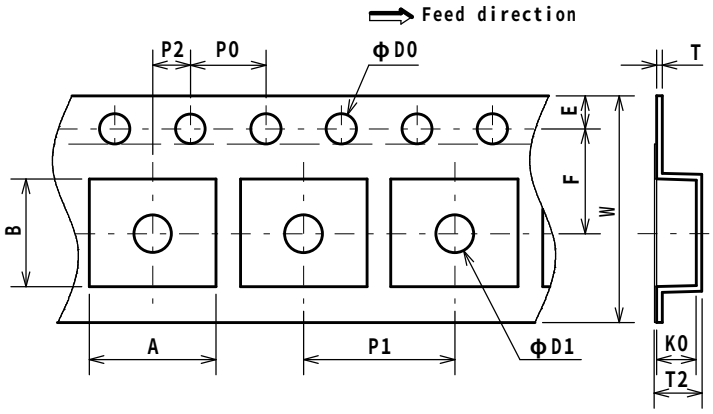
Solder paste composition	Sn37Pb (Senju Metal Industry Co., Ltd：OZ7053-340F-C)
	Sn3Ag0.5Cu (Senju Metal Industry Co., Ltd：M705-GRN350-32-11)

HSOP8

■PACKING SPEC

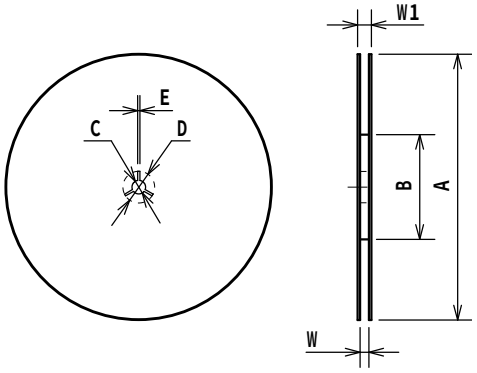
Unit: mm

TAPING DIMENSIONS



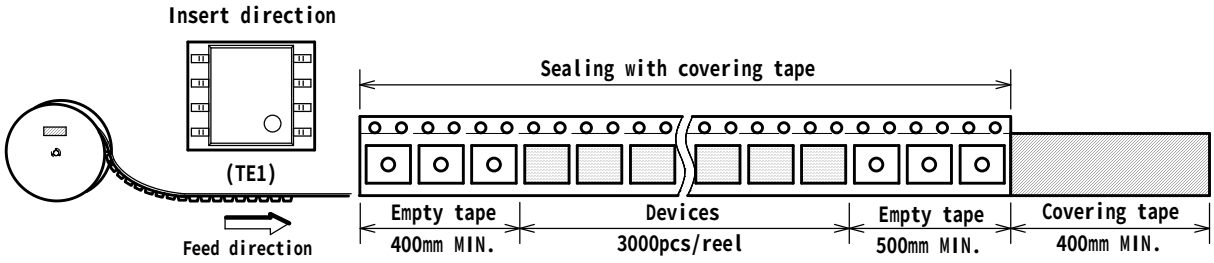
SYMBOL	DIMENSION	REMARKS
A	6.7±0.1	
B	5.55±0.1	
D0	1.55±0.05	
D1	2.05±0.05	
E	1.75±0.1	
F	5.5±0.05	
P0	4.0±0.1	
P1	8.0±0.1	
P2	2.0±0.05	
T	0.3±0.05	
T2	2.47	
K0	2.1±0.1	
W	12.0±0.2	

REEL DIMENSIONS

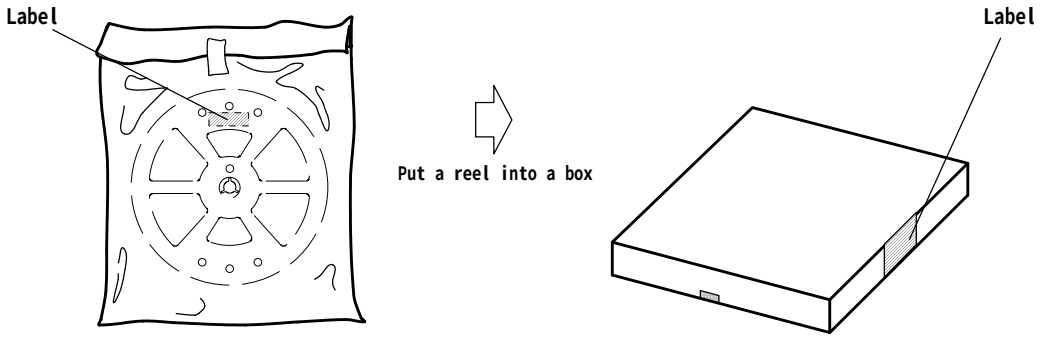


SYMBOL	DIMENSION
A	φ330±2
B	φ 80±1
C	φ 13±0.2
D	φ 21±0.8
E	2±0.5
W	13.5±0.5
W1	17.5±1

TAPING STATE

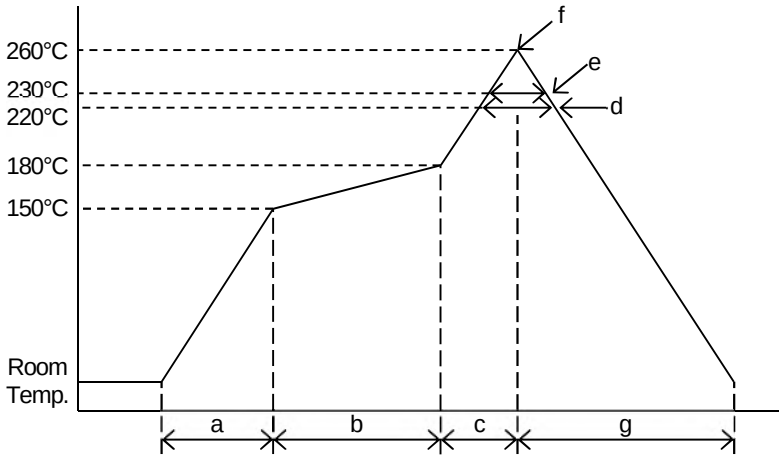


PACKING STATE



■ RECOMMENDED MOUNTING METHOD

INFRARED REFLOW SOLDERING PROFILE



a	Temperature ramping rate	1 to 4°C/s
b	Pre-heating temperature Pre-heating time	150 to 180°C 60 to 120s
c	Temperature ramp rate	1 to 4°C/s
d	220°C or higher time	shorter than 60s
e	230°C or higher time	shorter than 40s
f	Peak temperature	lower than 260°C
g	Temperature ramping rate	1 to 6°C/s

The temperature indicates at the surface of mold package.

■ **REVISION HISTORY**

DATE	REVISION	CHANGES
October 4, 2021	Ver.1.0	Initial release

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   - Power Generator Control Equipment (Nuclear, steam, hydraulic, etc.)
   - Life Maintenance Medical Equipment
   - Fire Alarms / Intruder Detectors
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9. The product specifications and descriptions listed in this datasheet are subject to change at any time, without notice.