BUCK SWITCHING REGULATOR WITH VOLTAGE CORRECTION CIRCUIT

■ FEATURES

- Output Current 2.4 A
- Default Output Voltage Accuracy V_{O_SENSE} ±1%
- Output Voltage Correction
  V_O + 253 mV (typ), 0 A to 2.0 A at R_{ADJ} = 10 kΩ
- Soft-Start Adjustable with external capacitors
- External Synchronization 290 kHz to 500 kHz
- Error Flag Output (FAULT)
- Error Flag Output Delay for Hot Plug 1.4 msec (typ)
- Power-Good Output
- V^+ Short Detection
- ON/OFF Control
- Discharge at OFF-State
- Overcurrent Protection (Hiccup type)
  Adjustable limit value with external resistance
- Short-Circuit Protection
- Undervoltage Lockout
- Thermal Shutdown Circuit with Hysteresis
- Package HTSSOP24-P1

■ APPLICATIONS

- Car Infotainment
- USB Chargers

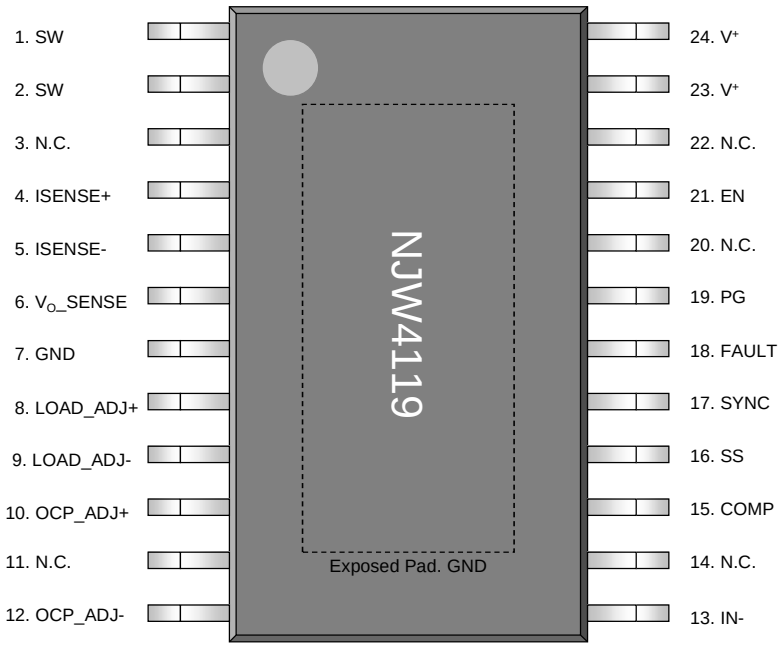
■ DESCRIPTION

The NJW4119 is a buck switching regulator with voltage correction circuit that delivers up to 2.4 A of output current.

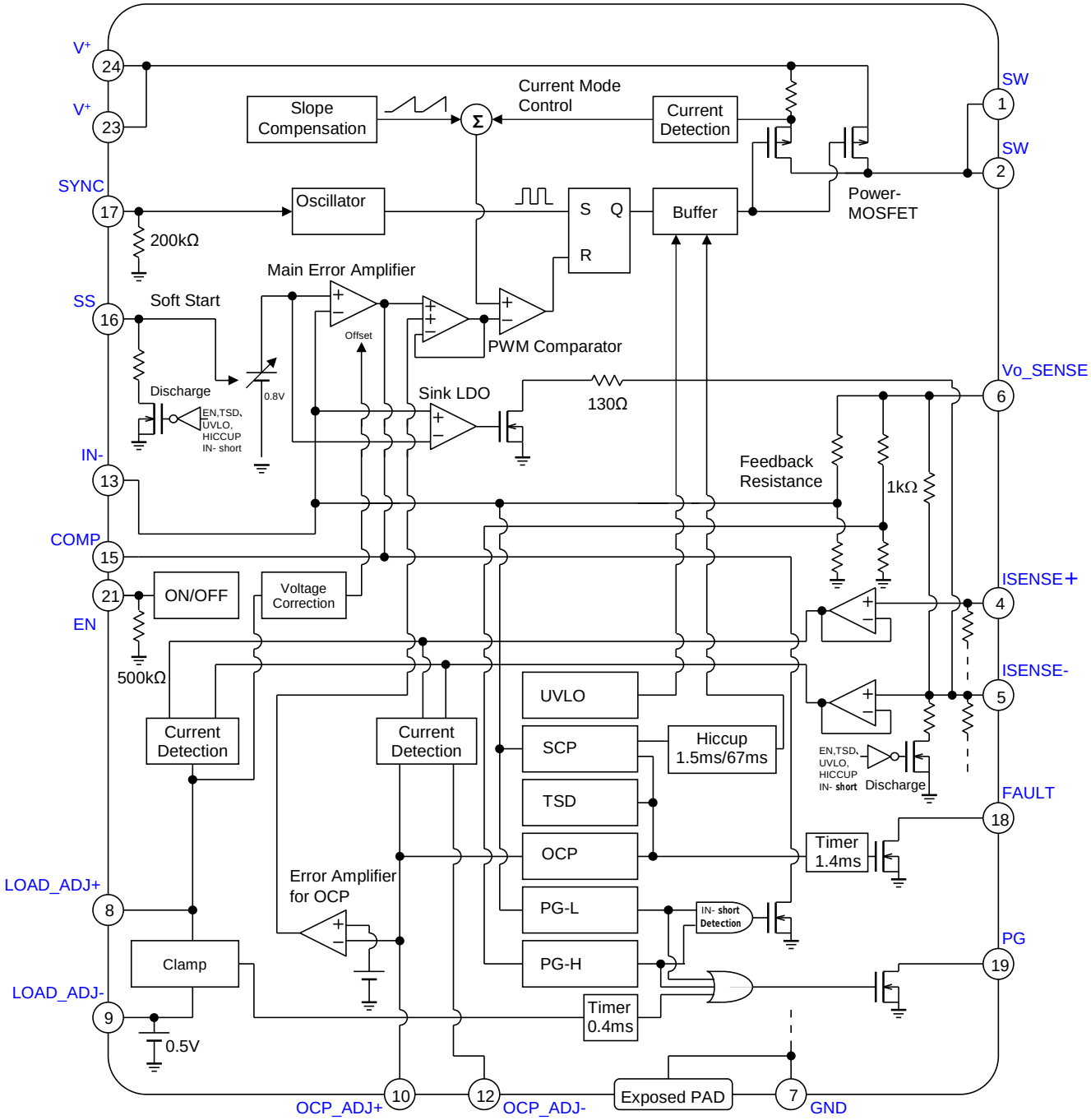
The voltage correction (cable drop compensation) raises the output voltage in proportion to the load current. This function corrects the voltage drop due to cable or writing board resistance.

Unique features, such as soft-start, power-good output and error flag output make the NJW4119 ideal for portable devices charged with USB cable.

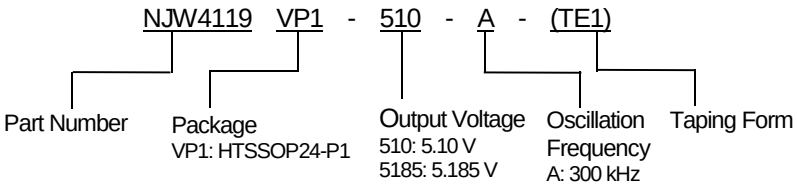
■ PIN CONFIGURATION (HTSSOP24-P1)



■ BLOCK DIAGRAM



■ PRODUCT NAME INFORMATION



■ ORDER ING FORMATION

PRODUCT NAME	PACKAGE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ (pcs)
NJW4119VP1-510A (TE1)	HTSSOP24-P1	Yes	Yes	Ni/Pd/Au	19A10	83	2500
NJW4119VP1-5185A (TE1)	HTSSOP24-P1	Yes	Yes	Ni/Pd/Au	19A185	83	2500

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Input Voltage	V^+	−0.3 to 45	V
V^+-SW Pin Voltage	$V_{V^+\text{-SW}}$	−0.3 to 45	V
EN Pin Voltage	V_{EN}	−0.3 to 45	V
V_O_SENSE Pin Voltage	V_{Vo_SENSE}	−0.3 to 16	V
ISENSE+/− Pin Voltage	$V_{ISENSE+/-}$	−0.3 to 16	V
SYNC Pin Voltage	V_{SYNC}	−0.3 to 6	V
FAULT Pin Voltage	V_{FLT}	−0.3 to 6	V
PG Pin Voltage	V_{PG}	−0.3 to 6	V
Power Dissipation (T_a = 25°C) HTSSOP24-P1	P_D	2-Layer (1) / 4-Layer (2) 1200 / 3300	mW
Junction Temperature	T_j	−40 to 150	°C
Operating Temperature	T_{opr}	−40 to 125	°C
Storage Temperature	T_{stg}	−50 to 150	°C

(1) 2-Layer: Mounted on glass epoxy board (114.5 mm × 101.5 mm × 1.6 mm: based on EIA/JEDEC standard, 2-layer FR-4).
(2) 4-Layer: Mounted on glass epoxy board (114.5 mm × 101.5 mm × 1.6 mm: based on EIA/JEDEC standard, 4-layer FR-4).
(For 4-layer: Applying 99.5 mm × 99.5 mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5.)

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Input Voltage	V^+	6.5 to 40	V
EN Pin Voltage	V_{EN}	0 to 40	V
PG Pin Voltage	V_{PG}	0 to 5.5	V
FAULT Pin Voltage	V_{FLT}	0 to 5.5	V
External Clock Input	f_{SYNC}	290 to 500	kHz

■ ELECTRICAL CHARACTERISTICS

$V^+ = V_{EN} = 12$ V, $C_{IN} = 10$ µF, $R_{ADJ} = 10$ kΩ, $C_{LOAD} = 2.2$ nF, $C_{SS} = 0.047$ µF, $R_{OCP} = 10$ kΩ, SYNC = IN− = COMP = OPEN, $T_a = 25$°C, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
GENERAL CHARACTERISTICS							
Quiescent Current	I_{DD}	R_L = no load, $V_{Vo\_SENSE} = V_{ISENSE+} = V_{ISENSE-} = 5.3$ V, No Switching		-	3.0	4.5	mA
Quiescent Current at OFF-State	I_{DD_STB}	$V_{EN} = 0$ V		-	-	10	µA
Output Voltage	ΔV_{ISENSE}	ΔV_{ISENSE} (3) = 0 mV	$V_O = 5.10$ V	5.05	5.10	5.15	V
			$V_O = 5.185$ V	5.135	5.185	5.235	
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T_a$	T_a = −40°C to 85°C, ΔV_{ISENSE} (3) = 0 mV		-	±50	-	ppm/°C
Load Regulation 1	$\Delta V_O/\Delta I_O1$	R_{ADJ} = 18 kΩ, ΔV_{ISENSE} (3) = 0 to 100 mV, $V_{ISENSE-}$ = 5.550 V (510) / $V_{ISENSE-}$ = 5.635 V (5185)		+414	+449	+484	mV
Load Regulation 2	$\Delta V_O/\Delta I_O2$	R_{ADJ} = 14 kΩ, ΔV_{ISENSE} (3) = 0 to 100 mV, $V_{ISENSE-}$ = 5.450 V (510) / $V_{ISENSE-}$ = 5.535 V (5185)		+317	+351	+385	mV
Load Regulation 3	$\Delta V_O/\Delta I_O3$	R_{ADJ} = 10 kΩ, ΔV_{ISENSE} (3) = 0 to 100 mV, $V_{ISENSE-}$ = 5.350 V (510) / $V_{ISENSE-}$ = 5.435 V (5185)		+221	+253	+285	mV
Output Clamp Voltage	V_{O_CLAMP}	R_{ADJ} = 18 kΩ, R_{OCP} = 0 kΩ, ΔV_{ISENSE} (3) = 0 to 300 mV, $V_{ISENSE-}$ = 6 V (510) / $V_{ISENSE-}$ = 5.800 V (5185)	$V_O = 5.10$ V	5.80	6.05	6.30	V
			$V_O = 5.185$ V	5.88	6.14	6.38	
V_O_SENSE Pin Bias Current	I_{VO_SENSE}	$V_{Vo\_SENSE} = 5.0$ V		-	50	140	µA
ISENSE+ Pin Bias Current	I_{SENSE+}	$V_{ISENSE+} = 5.0$ V		-	130	220	µA
ISENS− Pin Bias Current	I_{SENSE-}	$V_{ISENSE-} = 5.0$ V		-	20	80	µA
Soft-Start Time	t_{SS}	$C_{SS} = 0.047$ µF, from (V_{EN} = high) to ($V_O = V_O \times 0.9$)		-	4.3	7.0	ms
SS Pin Charge Current	I_{SS}	$V_{SS} = 0.4$ V		6	8	10	µA
ON/OFF CONTROL							
EN ON Voltage	$V_{EN\,(ON)}$	V_{EN} = SWEEP UP		1.6	-	-	V
EN OFF Voltage	$V_{EN\,(OFF)}$	V_{EN} = SWEEP DOWN		-	-	0.5	V
EN Pin Bias Current	I_{EN}	$V_{EN} = 12$ V		-	30	50	µA

(3) ΔV_{ISENSE} is the potential difference between the ISENSE+ and ISENSE- pins: (ΔV_{ISENSE} = (ISENSE+) − (ISENS−))
0 mV to 100 mV is equal to the current flowing from 0 A to 2 A at external current detection resistance (50 mΩ).

■ ELECTRICAL CHARACTERISTICS

$V^+ = V_{EN} = 12$ V, $C_{IN} = 10$ µF, $R_{ADJ} = 10$ kΩ, $C_{LOAD} = 2.2$ nF, $C_{SS} = 0.047$ µF, $R_{OCP} = 10$ kΩ, SYNC = IN− = COMP = OPEN, $T_a = 25$°C, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
PROTECTION CIRCUIT CHARACTERISTICS							
OVERCURRENT PROTECTION (OCP)							
OCP Threshold Voltage 1	V_{OCP1}	R_{OCP} = 16 kΩ, $V_{Vo\_SENSE} = V_{ISENSE-}$ = 5.1 V, $V_{OCP1} = \Delta V_{ISENSE}$ (3)		75	94	113	mV
OCP Threshold Voltage 2	V_{OCP2}	R_{OCP} =10 kΩ, $V_{Vo\_SENSE} = V_{ISENSE-}$ = 5.1 V, $V_{OCP2} = \Delta V_{ISENSE}$ (3)		120	150	180	mV
OCP Threshold Voltage 3	V_{OCP3}	R_{OCP} = 8.2 kΩ, $V_{Vo\_SENSE} = V_{ISENSE-}$ = 5.1 V, $V_{OCP3} = \Delta V_{ISENSE}$ (3)		150	185	225	mV
FAULT OCP Judge Threshold Voltage	$V_{OCP\_DET\_FLT}$			$V_{OCP(N)}$ × 0.80	$V_{OCP(N)}$ × 0.88	$V_{OCP(N)}$ × 0.95	mV
SHORT-CIRCUIT PROTECTION (SCP)							
SCP ON Threshold Voltage	V_{OSCP}	V_O_SENSE = SWEEP DOWN	V_O = 5.10 V	2.9	3.2	3.5	V
			V_O = 5.185 V	2.95	3.25	3.56	
SCP Release Hysteresis Width	V_{OSCP_HYS}	V_O_SENSE = SWEEP UP		-	+0.8	-	V
Hiccup Wait Time	t_{SCP}			-	1.5	-	ms
Cool-Down Time	t_{COOL}			-	67	-	ms
UNDERVOLTAGE LOCKOUT (UVLO)							
UVLO_ON Threshold Voltage	$V_{UVLO\,(ON)}$	V^+ = SWEEP UP		5.85	6.15	6.45	V
UVLO_OFF Threshold Voltage	$V_{UVLO\,(OFF)}$	V^+ = SWEEP DOWN		5.68	5.98	6.28	V
UVLO Hysteresis Width	V_{UVLO_HYS}			70	170	-	mV
POWER-GOOD							
V_O_SENSE Sweep Down Detection Level	V_{PG_THL}	V_O_SENSE = SWEEP DOWN	V_O = 5.10 V	3.7	4.0	4.3	V
			V_O = 5.185 V	3.76	4.07	4.37	
V_O_SENSE Sweep Up Detection Level	V_{PG_THH}	V_O_SENSE = SWEEP UP		6.45	6.70	6.95	V
PG_THL Hysteresis Width	$V_{PG\_THL\_HYS}$			-	+0.4	-	V
PG_THH Hysteresis Width	$V_{PG\_THH\_HYS}$			-	-0.15	-	V
PG Output ON-Resistance	R_{ON_PG}	I_{PG} = 10 mA		-	5	25	Ω
PG Pin Leak Current	I_{LEAK_PG}	V_{PG} = 6 V, PG = High		-	-	0.1	µA
PG Output Delay Time at Output Clamp	$td_{\_VoCLAMP}$	From "V_O CLAMPED" to "Error Flag Output"		-	0.4	-	ms
ERROR FLAG (FAULT)							
FAULT Output Delay Time	td	From “Error Occurred” to “Error Flag Output”		0.7	1.4	1.8	ms
FAULT Output ON-Resistance	R_{ON_FLT}	I_{FLT} = 10 mA		-	5	25	Ω
FAULT Pin Leak Current	I_{LEAK_FLT}	V_{FLT} = 6 V, FAULT = High		-	-	0.1	µA

(3) ΔV_{ISENSE} is the potential difference between the ISENSE+ and ISENSE− pins: (ΔV_{ISENSE} = (ISENSE+) − (ISENSE−))
0 mV to 100 mV is equal to the current flowing from 0 A to 2 A at external current detection resistance (50 mΩ).

■ ELECTRICAL CHARACTERISTICS

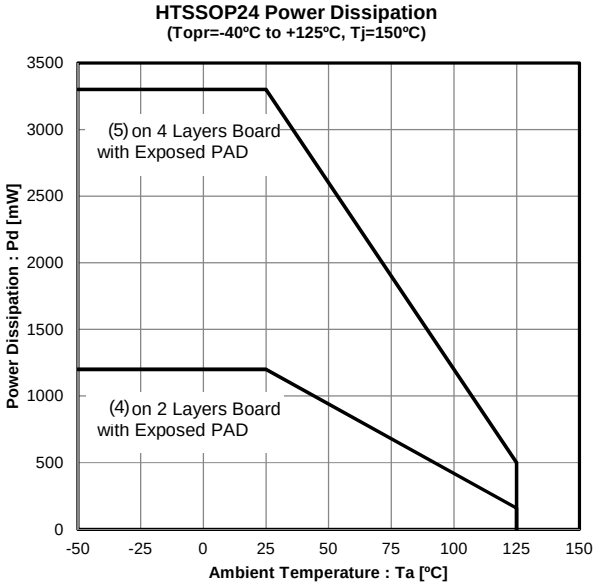
$V^+ = V_{EN} = 12$ V, $C_{IN} = 10$ µF, $R_{ADJ} = 10$ kΩ, $C_{LOAD} = 2.2$ nF, $C_{SS} = 0.047$ µF, $R_{OCP} = 10$ kΩ, SYNC = IN− = COMP = OPEN, $T_a = 25$°C, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWITCHING REGULATOR CHARACTERISTICS						
OSCILLATOR						
Oscillation Frequency	f_{OSC}		270	300	330	kHz
Oscillate Supply Voltage Fluctuations	f_{DV}	$V^+ = 6.5$ V to 40 V	-	1	-	%
Oscillate Temperature Fluctuations	f_{DT}	$T_a = -40$°C to 85°C	-	5	-	%
SYNC Pin High-Level Detection Voltage	V_{THH_SYNC}		1.6	-	5.5	V
SYNC Pin Low-Level Detection Voltage	V_{THL_SYNC}		0	-	0.3	V
SYNC Pin Bias Current	I_{SYNC}	$V_{SYNC} = 6$ V	-	30	60	µA
PWM COMPARATOR						
Maximum Duty Cycle	$MAXDUTY$	$V_{VO\_SENSE} = 4.5$ V	92	95	-	%
Minimum ON-Time 1 (Using internal oscillator)	$t_{ON\text{-}min1}$		-	200	300	ns
Minimum ON-Time 2 (Using external clock)	$t_{ON\text{-}min2}$	$f_{SYNC} = 400$ kHz	-	200	300	ns
POWER MOSFET OUTPUT						
Power MOSFET Limiting Current	I_{LIM}		4.5	6	7.5	A
Power MOSFET ON-Resistance	R_{ON}	$I_{SW} = 3$ A	-	0.15	0.3	Ω
Power MOSFET Leak Current	I_{LEAK}	$V_{EN} = 0$ V, $V^+ = 40$ V, $V_{SW} = 0$ V	-	-	4	µA

■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	VALUE	UNIT
Junction-to-Ambient Thermal Resistance HTSSOP24-P1	θ_{ja}	2-Layer (4) / 4-Layer (5) 115 / 45	°C/W
Junction-to-Top of Package Characterization Parameter HTSSOP24-P1	Ψ_{jt}	2-Layer (4) / 4-Layer (5) 14 / 7	°C/W

■ POWER DISSIPATION vs. AMBIENT TEMPERATURE



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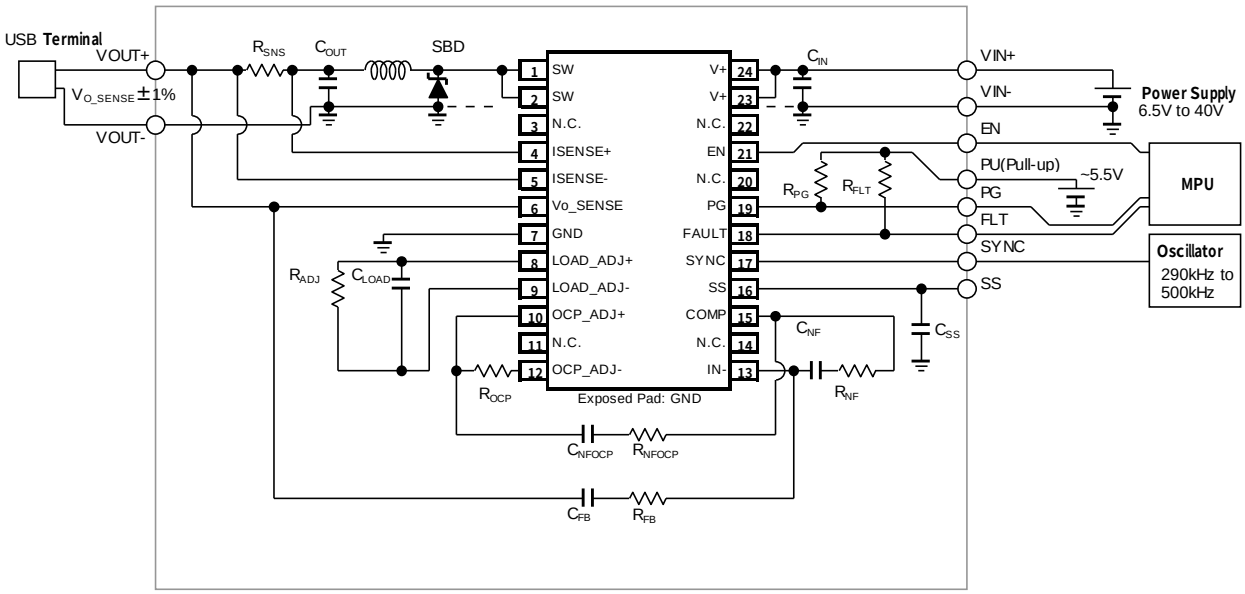
(5) 4-Layer: Mounted on glass epoxy board (114.5 mm × 101.5 mm × 1.6 mm: based on EIA/JEDEC standard, 4-layer FR-4).
(For 4-layer: Applying 99.5 mm × 99.5 mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5.)

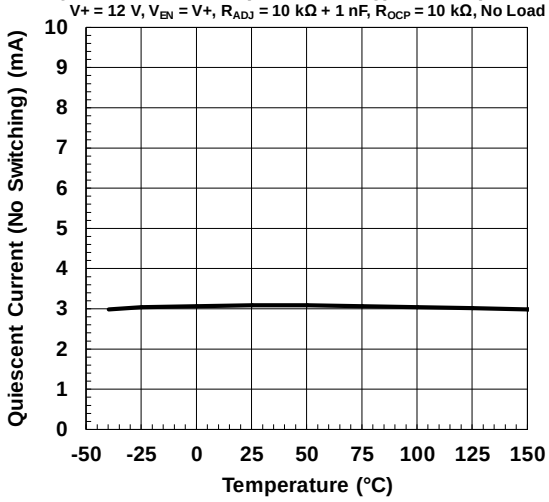
■ APPLICATION CIRCUIT



■ TYPICAL CHARACTERISTICS

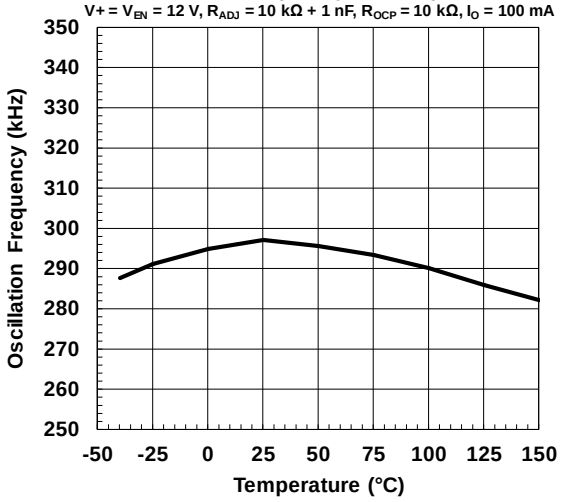
Quiescent Current (No Switching) vs. Temperature

V+ = 12 V, V_{EN} = V+, R_{ADJ} = 10 kΩ + 1 nF, R_{OCP} = 10 kΩ, No Load



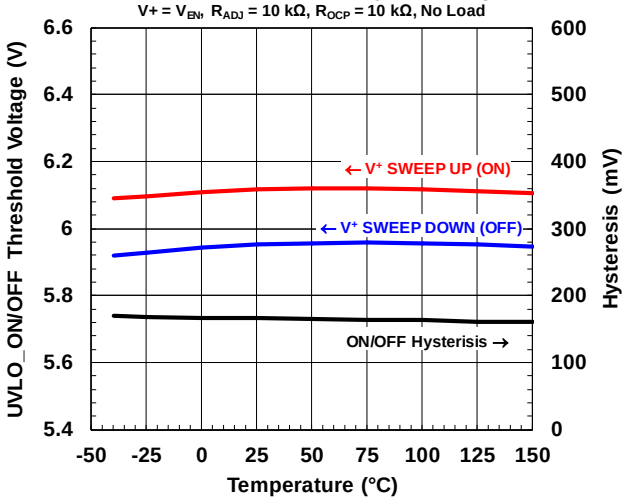
Oscillation Frequency vs. Temperature

V+ = V_{EN} = 12 V, R_{ADJ} = 10 kΩ + 1 nF, R_{OCP} = 10 kΩ, I_O = 100 mA



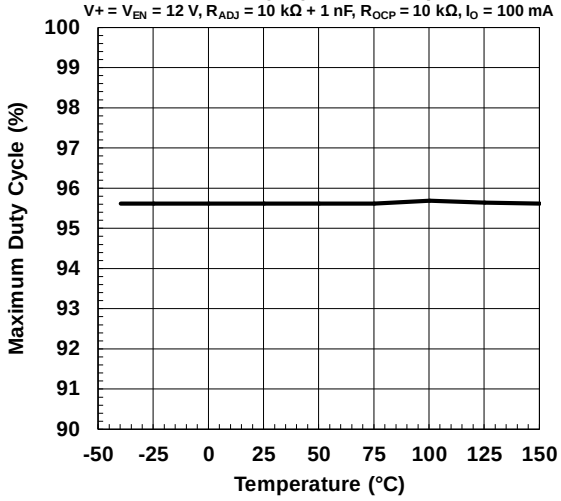
UVLO_ON/OFF Threshold Voltage vs. Temperature

V+ = V_{EN}, R_{ADJ} = 10 kΩ, R_{OCP} = 10 kΩ, No Load



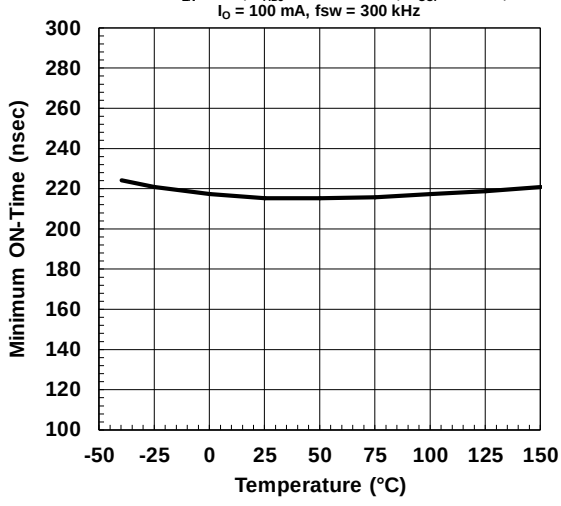
Maximum Duty Cycle vs. Temperature

V+ = V_{EN} = 12 V, R_{ADJ} = 10 kΩ + 1 nF, R_{OCP} = 10 kΩ, I_O = 100 mA



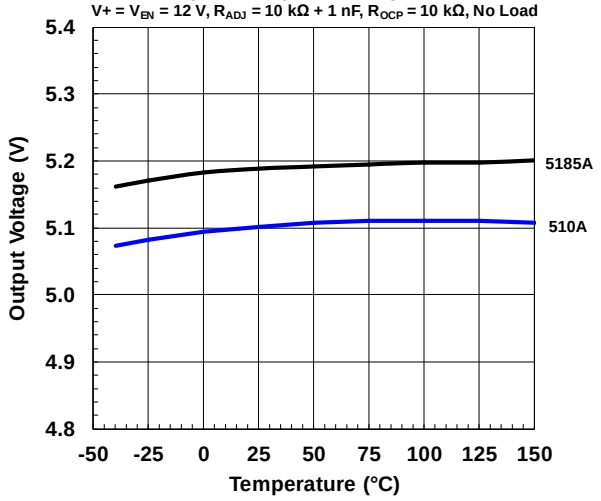
Minimum ON-Time vs. Temperature

V+ = V_{EN} - 12 V, R_{ADJ} = 10 kΩ + 1 nF, R_{OCP} = 10 kΩ,
I_O = 100 mA, fsw = 300 kHz

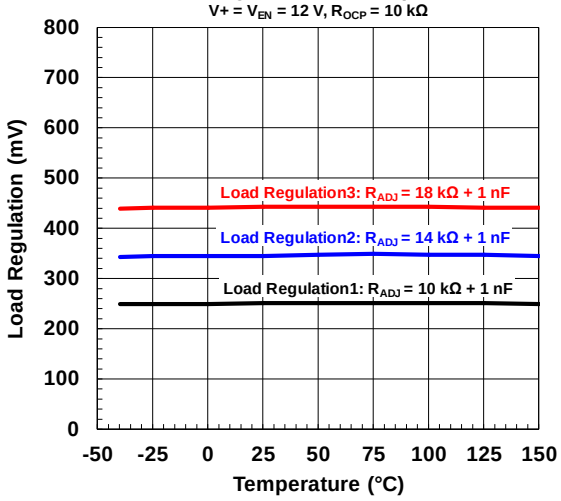


■ TYPICAL CHARACTERISTICS

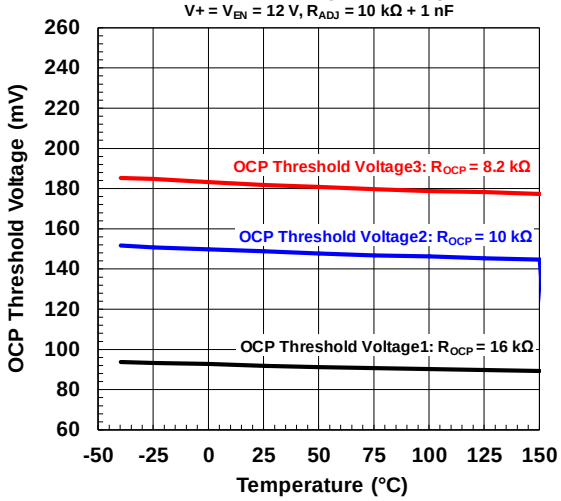
Output Voltage vs. Temperature
V+ = V_{EN} = 12 V, R_{ADJ} = 10 kΩ + 1 nF, R_{OCP} = 10 kΩ, No Load



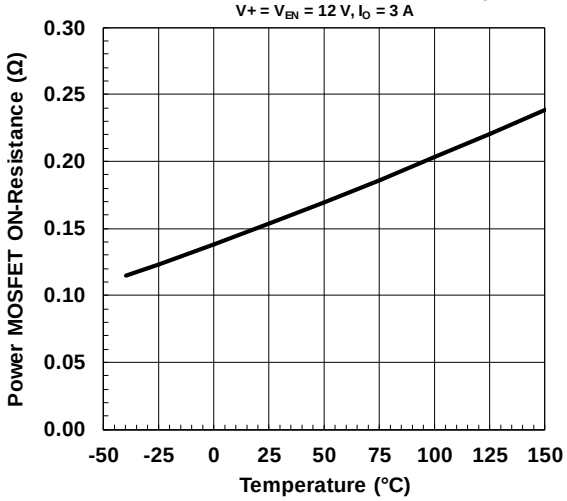
Load Regulation vs. Temperature
V+ = V_{EN} = 12 V, R_{OCP} = 10 kΩ



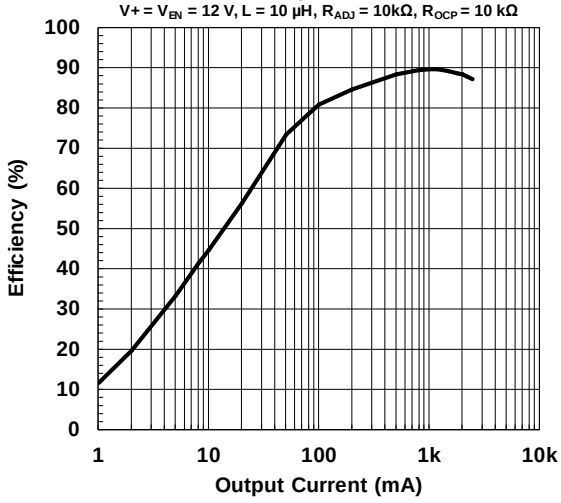
OCP Threshold Voltage vs. Temperature
V+ = V_{EN} = 12 V, R_{ADJ} = 10 kΩ + 1 nF



Power MOSFET ON-Resistance vs. Temperature
V+ = V_{EN} = 12 V, I_O = 3 A



NJW4119VP1-510A
Efficiency (include loss of RSNS)
vs. Output Current
V+ = V_{EN} = 12 V, L = 10 µH, R_{ADJ} = 10kΩ, R_{OCP} = 10 kΩ



■ PIN FUNCTIONS

PIN NO.	SYMBOL	RATING	DESCRIPTION
1, 2	SW	45 V	Switch output pin for P-channel power MOSFET. The maximum drain current is limited to 4.5 V (min). When SW pin voltage exceeds V^+ pin voltage, SBD must be connected between these pins because the SW pin is connected the V^+ pin through a body diode.
4, 5	ISENSE+/−	16 V	Monitor pin of difference voltage at R_{SNS}. Connect the RSNS as follows. ISENSE+: high potential side of RSNS (rectified circuit side). ISENSE−: low potential side of RSNS (load side). Consider the wiring design in order not to add the resistance element of the PCB wiring. The voltage correction and overcurrent protection (rectified) are performed using the electric potential difference, generated between ISENSE+ and ISENSE-. When EN = OFF, UVLO lock, thermal shutdown, hiccup cool-down or IN− ground fault is detected, the discharge transistor built-in the ISENSE− pin is turned on, and the output voltage is rapidly reduced.
6	V_O_SENSE	16 V	Voltage detection pin of feedback resistor. The node connected to this pin is feedback controlled to be V_{O_SENSE} (typ) + correction voltage. The feedback resistance total value is approximately 200 kΩ. Connect R_{FB} and C_{FB} between this pin and the COMP pin for phase compensation. An internal 1 kΩ resistor is connected between this pin and the ISENSE− pin to prevent the output voltage from going to the V^+ even if this pin is open; however, open use is not guaranteed.
7 (Exposed Pad)	GND	-	Ground pin. Connect to GND to improve heat dissipation.
8	LOAD_ADJ+	6 V	Voltage correction adjustment (load regulation) pin. The load regulation (0 A to 2.0 A) at R_{ADJ} = 10 kΩ is +253 mV (typ). Connect the C_{LOAD} in parallel to R_{ADJ} to prevent oscillations caused by voltage correction. A current proportional to the potential difference of the current detection resistor (R_{SNS}) is output to LOAD_ADJ+. When the voltage correction is not used, this pin must be shorted.
9	LOAD_ADJ−		
10	OCP_ADJ+	6 V	Overcurrent limit value adjustment pin. As the resistor value is increased, the overcurrent protection limit value gets smaller. The overcurrent protection limit value at R_{OCP} = 10 kΩ is 3 A (typ). Regardless of the R_{OCP} value, the maximum power transistor current is 4.5 A (min). For phase compensation during overcurrent protection, connect R_{NFOCP} and C_{NFOCP} between OCP_ADJ+ and COMP pins. When the overcurrent protection is not used, this pin must be shorted. The IC is protected by the power MOSFET current limit, but it depends on the supply voltage.
12	OCP_ADJ−		
13	IN−	6 V	Middle point of feedback resistor. For phase compensation, connect R_{NF} and C_{NF} between this pin and the COMP pin. To prevent the output voltage from going to the V^+ even if this pin shorts to ground, this pin is designed to stop the SW operation and discharge the soft start capacitor at the same time when a ground fault is detected.
15	COMP	6 V	Output pin of main error amplifier.
16	SS	6 V	Setting pin of soft start time. Charge C_{SS} with 8 µA (typ) and slowly increase the reference voltage of the main error amplifier. The soft start time when connected at 0.047 µF is 4.3 ms (typ). The C_{SS} is discharged during thermal shutdown, hiccup cooldown, EN = OFF, UVLO lock and IN− pin ground fault.
17	SYNC	6 V	Input pin for external clock. Available synchronization signals are as follows: f = 290 kHz to 500 kHz, duty = 20% to 80%, low ≤ 0.3 V, high ≥ 1.6 V. This pin is pulled down to GND with an internal resistance of 200 kΩ.

■ PIN FUNCTIONS

PIN NO.	SYMBOL	RATING	DESCRIPTION
18	FAULT	6 V	Error flag output pin. An error flag (low) is output during thermal shutdown, hiccup cooldown, and when the output current is 88% (typ) or more of the overcurrent protection value set by R_{OCP}. As soon as the abnormal state is released, the error flag is cleared (high). This pin is an open drain pin of the Nch FET. Connect to the power supply through a resistor. The ON resistance value of Nch FET is 25 Ω (max). Leave this pin open when not in use.
19	PG	6 V	Power-good pin. This pin outputs error flag when the V_O_SENSE pin voltage is ≤ 4.0 V, ≥ 6.7 V, EN = OFF or soft start. If the correction is strong and the V_O_SENSE pin reaches the output clamp voltage (6.05 V, typ), PG is switched to low after 0.4 ms (typ). It can be used for system control when R_{ADJ} is open. This pin is an open drain pin of the Nch FET. Connect to the power supply through a resistor. The ON-resistance value of Nch FET is 25 Ω (max). Leave this pin open when not in use.
21	EN	45 V	Enable pin. This pin is high active. When EN = OFF, the internal circuit is stopped and the current consumption is reduced to 10 µA. This pin is pulled down with an internal resistor of 500 kΩ and fixed to OFF when this pin is open. The range of 0.5 V < V_{EN} < 1.6 V is undefined area of ON/OFF.
23, 24	V+	45 V	Power supply pin. Insert the bypass capacitor as close to the device as possible. The potential of this pin is monitored by UVLO, and this device operates when it exceeds 6.15 V (typ).
3, 11, 14, 20, 22	N.C.	-	Not internally connected

■ APPLICATION NOTE

Voltage Correction (Load Regulation) Adjustment

The NJW4119 can adjust the load regulation by connecting R_{ADJ} between the LOAD_ADJ+ and the LOAD_ADJ− pins. The R_{ADJ} can be calculated using the following formula 1 or refer to Table 1. To prevent the deterioration in correction accuracy and overcurrent protection, 47 mΩ to 56 mΩ R_{SNS} value is recommended. The NJW4119 has an output voltage clamp function to prevent excess output voltage during voltage correction. This clamp voltage value is not in accordance with R_{ADJ} and/or R_{SNS} (Figure 1).

Table1. R_{ADJ}(kΩ) vs. Load Regulation Correspondence Table (0A to 2.0A) @25°C

R_{ADJ} (kΩ)	Load Regulation(mV) 0A to 2.0A
2.0	57
2.2	62
2.4	67
2.7	74
3.0	82
3.3	89
3.6	96
4.3	113
4.7	123
5.1	133
5.6	145
6.2	160
6.8	175
7.5	192
8.2	209
9.1	231
10	253
11	278
12	302
13	327
15	376
16	400
18	449
20	498

$$\Delta Vo / \Delta Io(mV) = 0.245 \times R_{SNS}(m\Omega) \times Io(A) \times (R_{ADJ}(k\Omega) + 0.33) \quad \text{...Formula 1}$$

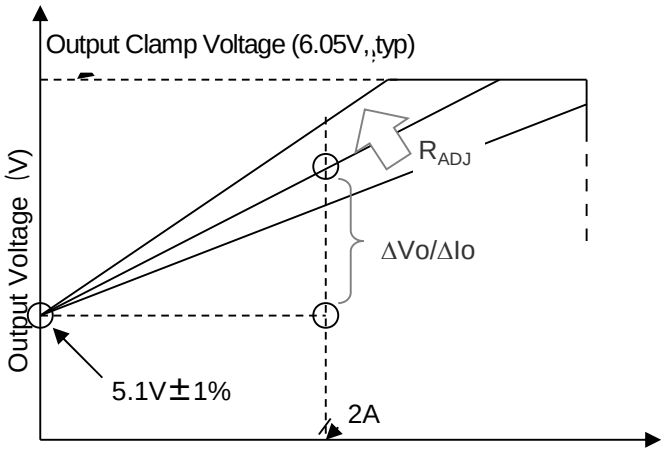


Figure 1. Output Clamp Voltage

Overcurrent Protection

The NJW4119 includes 2 types of overcurrent protection as follows:

(1) Power MOSFET Current Limit (I_{LIM})
Power MOSFET current limit monitors the current flowing in the power MOSFET every cycle, and when the current exceeds 4.5 A (min), this function stops the power MOSFET until the next cycle to protect the IC.

(2) Overcurrent Protection of Output Current after Rectification ($V_{OCP1/2/3}$)
When the potential voltage difference across the external current detection resistor (R_{SNS}) exceeds the threshold voltage set by R_{OCP}, feedback control is switched from constant voltage control to constant current control. The function protects the load by preventing the current exceeding the set current value from flowing (Figure 2 and Formula 2).

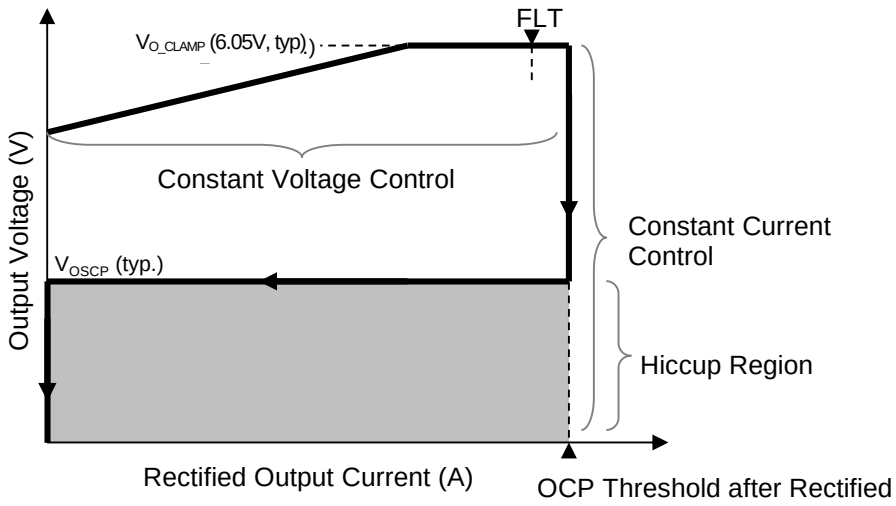


Figure 2. Overcurrent Protection of Output Current after Rectification

The NJW4119 power MOSFET switching current limit value (4.5 A, min) is constant regardless of R_{OCP}. It must be set not to exceed 4.5 A with considering V^+, inductance, and oscillation frequency.

Hiccup Type Short-Circuit Protection

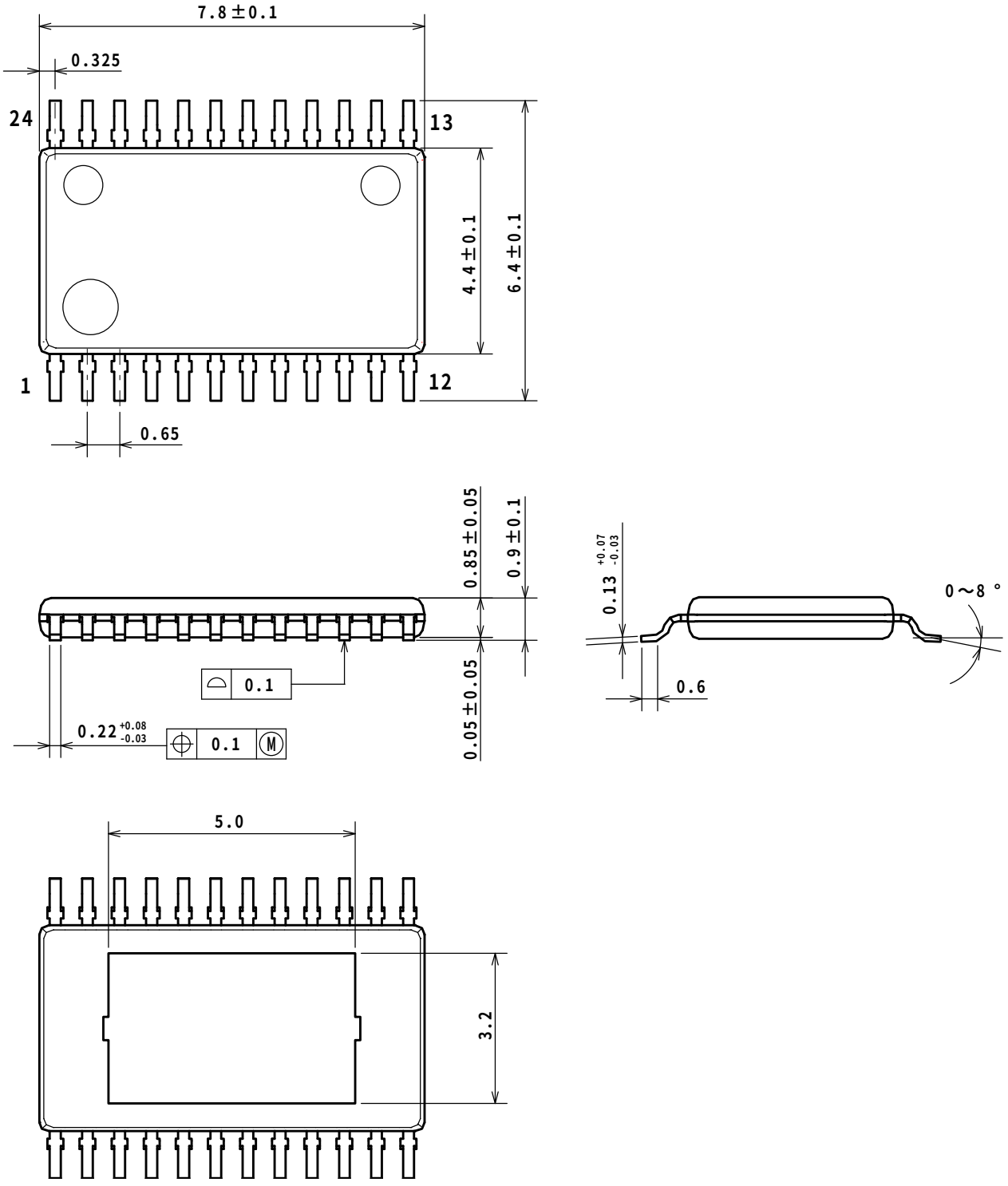
The NJW4119 turns off the power MOSFET for 67 ms (typ) after waiting 1.4 ms (typ) when overcurrent protection is operated and the output voltage falls below V_{OSCP}, and then restarts with soft-start. This operation is repeated until the short-circuit condition is released. The error flag (FAULT = low) is output during cool-down.

$$I\,\mathrm{lim}(A) = \frac{1500}{R_{SNS}(\Omega) \times R_{OCP}(\Omega)} \quad \text{…Formula 2}$$

HTSSOP24-P1

■ PACKAGE DIMENSIONS

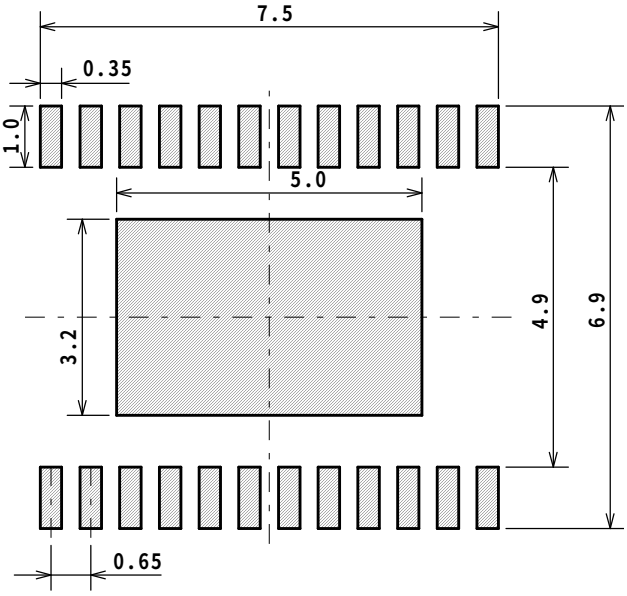
Unit: mm



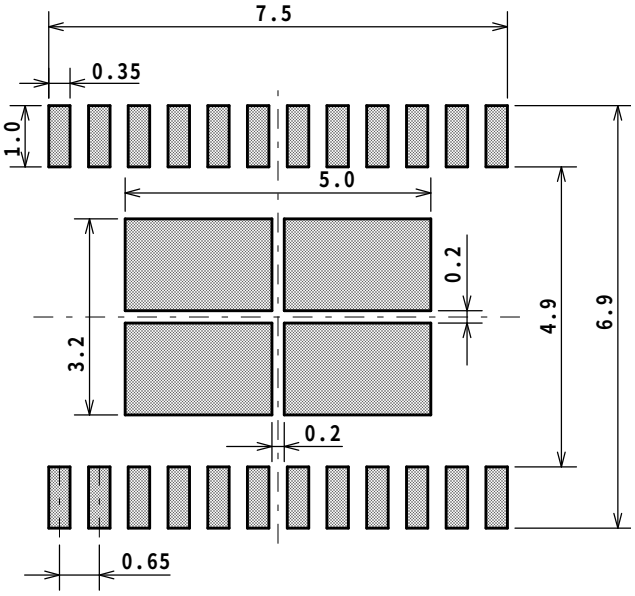
HTSSOP24-P1

■ EXAMPLE OF SOLDER PADS DIMENSIONS

Unit: mm



<Solder pattern>



<Metal mask>

＜Instructions for mounting＞

Please note the following points when you mount HTSSOP24-P1 package IC because there is a backside electrode.

(1) Temperature profile of lead and backside electrode.

It is necessary that both re-flow temperature profile of lead and backside electrodes are higher than preset temperature.

When solder wet temperature is lower than lead/backside electrode temperature, there is possibility of defect mounting.

(2) Design of foot pattern / metal mask

Metal mask thickness of solder pattern print is more than 0.13mm.

(3) Solder paste

The mounting was evaluated with following solder paste, foot pattern and metal mask. Because mounting might be greatly different according to the manufacturer and the product number even if the solder composition is the same. We will strongly recommend to evaluate mounting previously with using foot pattern, metal mask and solder paste.

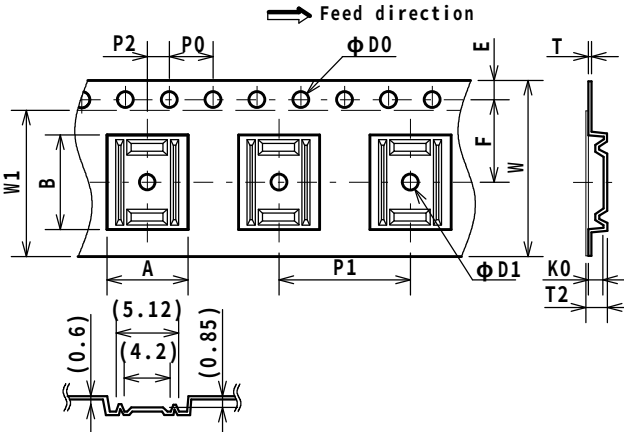
Solder paste composition	Sn3Ag0.5Cu (Senju Metal Industry Co., Ltd：M705-GRN350-32-11)

HTSSOP24-P1

■ PACKING SPEC

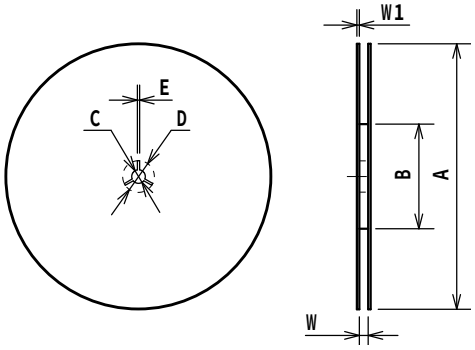
Unit: mm

TAPING DIMENSIONS



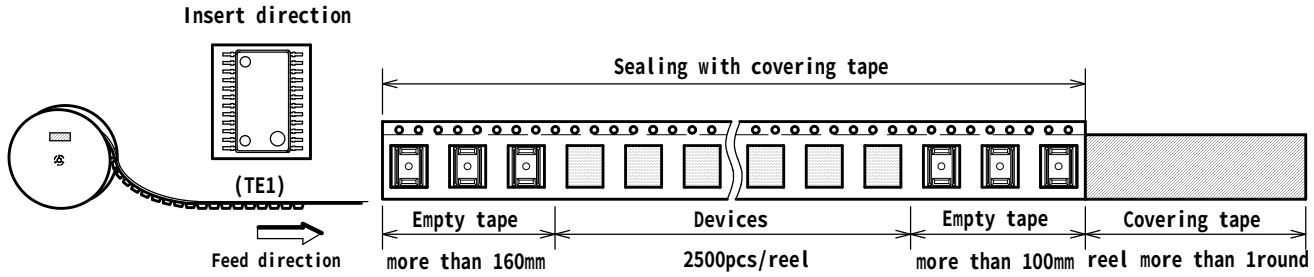
SYMBOL	DIMENSION	REMARKS
A	7.45±0.2	
B	8.60±0.1	
D0	$1.5^{+0.1}_{0}$	
D1	$1.5^{+0.1}_{0}$	
E	1.75±0.1	
F	7.5±0.1	
P0	4.0±0.1	
P1	12.0±0.1	
P2	2.0±0.1	
T	0.3±0.05	
T2	1.85	
K0	1.45±0.3	
W	16.0±0.3	
W1	13.3	THICKNESS 0.1max

REEL DIMENSIONS

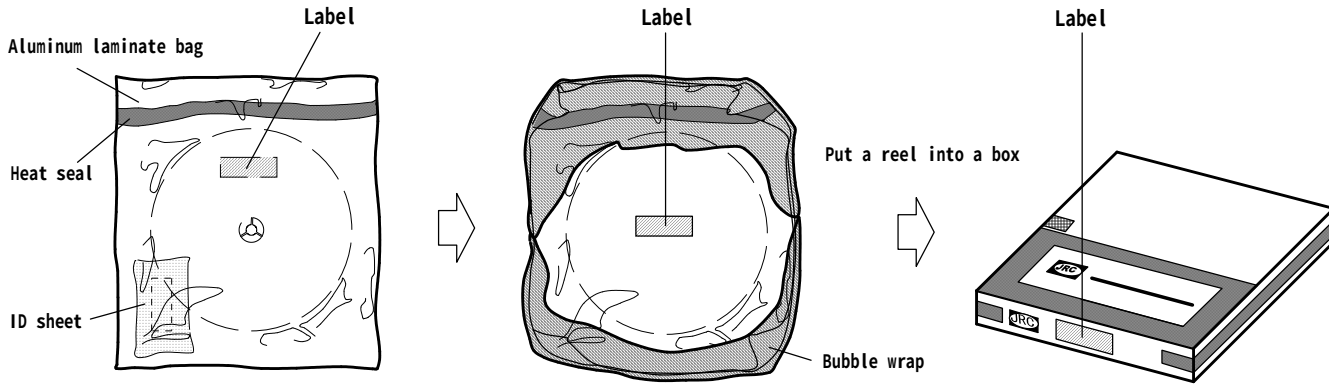


SYMBOL	DIMENSION
A	Φ330±2
B	Φ100±1
C	Φ 13±0.2
D	Φ 21±0.8
E	2±0.5
W	17.4±1
W1	2

TAPING STATE

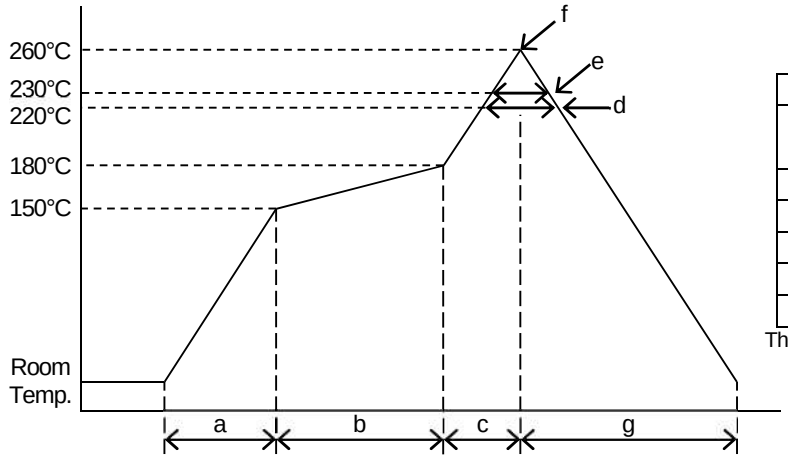


PACKING STATE



■ RECOMMENDED MOUNTING METHOD

INFRARED REFLOW SOLDERING PROFILE



a	Temperature ramping rate	1 to 4°C/s
b	Pre-heating temperature Pre-heating time	150 to 180°C 60 to 120s
c	Temperature ramp rate	1 to 4°C/s
d	220°C or higher time	shorter than 60s
e	230°C or higher time	shorter than 40s
f	Peak temperature	lower than 260°C
g	Temperature ramping rate	1 to 6°C/s

The temperature indicates at the surface of mold package.

■ REVISION HYSTORY

DATE	REVISION	CHANGES
November 16, 2020	Ver.1.0	Initial release due to datasheet format change

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