

Io=500mA LDO with Reset function

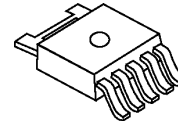
■ GENERAL DESCRIPTION

The NJW4116 is a 500mA output low dropout voltage regulator with reset function monitoring output voltage.

Reset Output Hold Time is adjustable by external capacitor.

Because of wide operate voltage range and wide temperature range, the NJW4113 suits for high reliability application such as automotive application.

■ PACKAGE OUTLINE

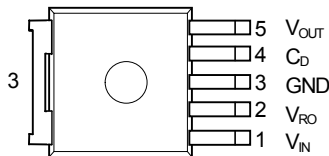


NJW4116DL3

■ FEATURES

- Wide Operating Voltage Range 4.0V to 40V
- Low Current Consumption 55 μ A typ.
- High Precision Output Voltage $V_o \pm 1.0\%$ ($T_a=25^\circ\text{C}$)
 $V_o \pm 2.0\%$ ($T_a=-40$ to $+125^\circ\text{C}$)
- High Precision Detection Voltage $V_{\text{DET}} \pm 1.0\%$ ($T_a=25^\circ\text{C}$)
 $V_{\text{DET}} \pm 2.0\%$ ($T_a=-40$ to $+125^\circ\text{C}$)
- Output Current $I_o(\text{min.})=500\text{mA}$
- Adjustable RESET Output Delay Hold Time with external capacitor
- Correspond to Low ESR capacitor (MLCC)
- Thermal Shutdown Protection
- Over Current Protection
- Package Outline TO-252-5

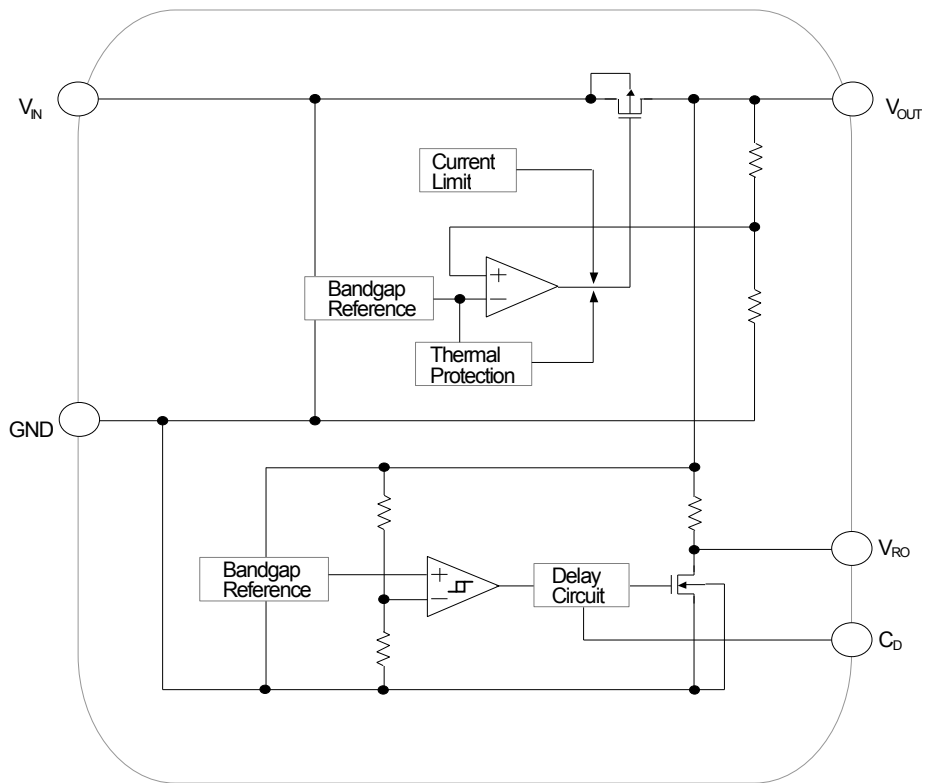
■ PIN CONFIGURATION



- | | |
|---------------------|---|
| 1. V_{IN} | Input Voltage Pin |
| 2. V_{RO} | Reset Output Pin |
| 3. GND | GND Pin |
| 4. C_{D} | External Capacitor Pin for setting RESET Output Delay Hold Time |
| 5. V_{OUT} | Output Voltage Pin |

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■ BLOCK DIAGRAM



■ PRODUCT CLASSIFICATION

Status	Device Name	Output Voltage	Detection Voltage
M.P.	NJW4116DL3-A46-T1	5.0V	4.6V
M.P.	NJW4116DL3-A41-T1	5.0V	4.1V
PLAN	NJW4116DL3-B03-T1	3.3V	3.0V

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Input Voltage	V _{IN}	-0.3 to +45	V
C _D pin Voltage	C _D	-0.3 to +6	V
Output Voltage	V _{OUT}	-0.3 to V _{IN} ≤ +6	V
RESET Output Voltage	V _{RO}	-0.3 to +6	V
Power Dissipation	P _D	1190(*1)	mW
		3125(*2)	
Junction Temperature	T _J	-40 to +150	°C
Operating Temperature	T _{opr}	-40 to +125	°C
Storage Temperature	T _{stg}	-40 to +150	°C

(*1): Mounted on glass epoxy board. (76.2×114.3×1.6mm: based on EIA/JDEC standard size, 2Layers, Cu area 100mm²)

(*2): Mounted on glass epoxy board. (76.2×114.3×1.6mm: based on EIA/JDEC standard, 4Layers)

(For 4Layers: Applying 74.2×74.2mm inner Cu area and thermal via holes to a board based on JEDEC standard JESD51-5)

■ Operating Voltage Range

V_{IN}=4.0 to 40V

■ ELECTRICAL CHARACTERISTICS

Unless otherwise noted, $V_{IN}=V_O+1V$, $C_{IN}=1.0\mu F$, $C_O=4.7\mu F$ ($V_O<3.4V$: $C_O=10\mu F$) $T_a=25^\circ C$

(Regulator Block)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Voltage	V_O	$I_O=30mA$	-1.0%	-	+1.0%	V
		$I_O=30mA$, $T_a=-40^\circ C$ to $+125^\circ C$	-2.0%	-	+2.0%	
Output Current	I_O	$V_O \times 0.9$	500	-	-	mA
		$V_O \times 0.9$, $T_a=-40^\circ C$ to $+125^\circ C$	500	-	-	
Line Regulation	$\Delta V_O/\Delta V_{IN}$	$V_{IN}=V_O+1V$ to $40V$, $I_O=30mA$	-	-	0.03	%V
		$V_{IN}=V_O+1V$ to $40V$, $I_O=30mA$, $T_a=-40^\circ C$ / $+125^\circ C$ (*4)	-	-	0.03	
Load Regulation	$\Delta V_O/\Delta I_O$	$I_O=0mA$ to $500mA$	-	-	0.006	%mA
		$I_O=0mA$ to $500mA$, $T_a=-40^\circ C$ / $+125^\circ C$ (*4)	-	-	0.008	
Ripple Rejection	RR	$V_{IN}=V_O+1V$, $e_{in}=200mV_{rms}$, $f=1kHz$, $I_O=10mA$, $V_O=5.0V$	-	55	-	dB
Dropout Voltage(*3)	ΔV_{IO}	$I_O=300mA$	-	0.27	0.42	V
		$I_O=300mA$, $T_a=-40$ to $+125^\circ C$	-	-	0.54	
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T_a$	$T_a=0^\circ C$ to $85^\circ C$, $I_O=30mA$	-	± 50	-	ppm/ $^\circ C$

(Voltage Detector Block)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Detection Voltage	V_{DET}		-1.0%	-	+1.0%	V
		$T_a=-40^\circ C$ to $+125^\circ C$	-2.0%	-	+2.0%	
Hysteresis Voltage	V_{HYS}		80	100	120	mV
		$T_a=-40^\circ C$ to $+125^\circ C$	50	-	150	
Low level RESET Output Voltage	V_{ROL}	$V_O=V_{DET}-0.5V$	-	0.2	0.4	V
		$V_O=V_{DET}-0.5V$, $T_a=-40^\circ C$ to $+125^\circ C$	-	-	0.4	
Average temperature coefficient of Detection Voltage	$\Delta V_{DET} / \Delta T_a$	$T_a=0^\circ C$ to $85^\circ C$	-	± 50	-	ppm/ $^\circ C$
Voltage Detector Block Operating Voltage	V_{OPL}		0.8	-	-	V
		$T_a=-40^\circ C$ to $+125^\circ C$	0.8	-	-	
RESET Output Voltage at Start up	V_{ROUV}	V_{IN} start up	-	0.05	-	V
Pull up resistor	R_{PU}		-	100	-	k Ω
RESET Output Delay Hold Time	t_d	$C_D=4.7nF$, $V_{RO}=L \rightarrow H$	8	10	12	ms
		$C_D=4.7nF$, $V_{RO}=L \rightarrow H$, $T_a=-40^\circ C$ to $+125^\circ C$	3	-	14	

(General Characteristics)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Quiescent Current	I_Q	$I_O=0mA$	-	55	90	μA
		$I_O=0mA$, $T_a=-40^\circ C$ to $+125^\circ C$	-	-	90	

(*3):Except Output Voltage Rank less than 3.8V.

(*4):These parameter are guaranteed with only $-40^\circ C$ and $+125^\circ C$.

The above specifications are common specifications for all output voltages. Therefore, it may be different from the individual specification for a specific output voltage.

* These parameters are tested by Pulse Measurement.

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■ THERMAL CHARACTERISTICS

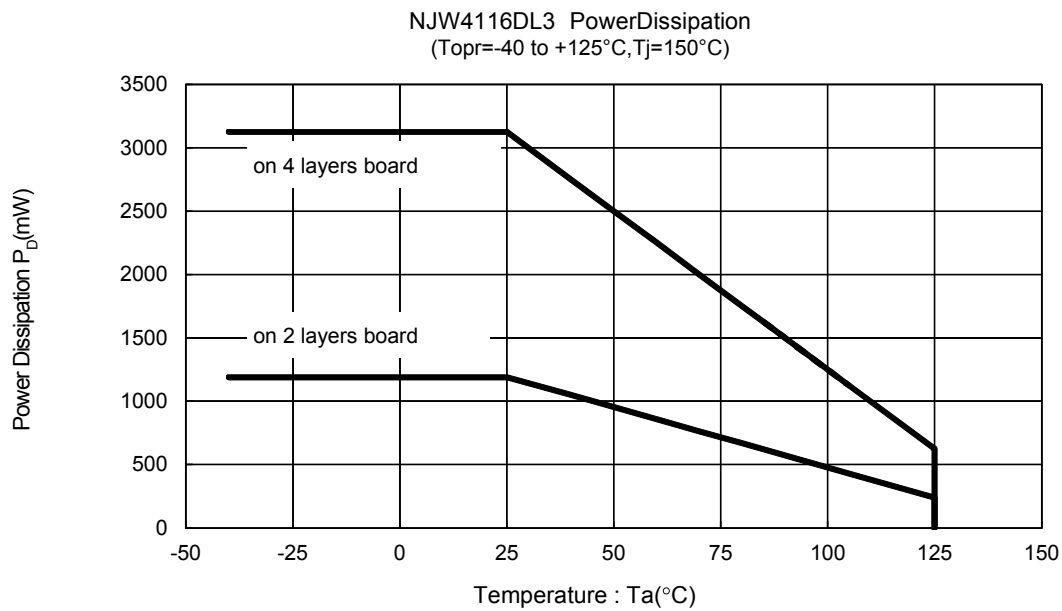
PARAMETER	SYMBOL	VALUE	UNIT
Junction-to-Ambient thermal resistance	θ_{ja}	105 (*5) 40 (*6)	$^{\circ}\text{C/W}$
Junction-to-Top of package characterization parameter	ψ_{jt}	17 (*5) 12 (*6)	$^{\circ}\text{C/W}$

(*5): Mounted on glass epoxy board. (76.2 × 114.3 × 1.6mm:based on EIA/JDEC standard size, 2Layers, Cu area 100mm²)

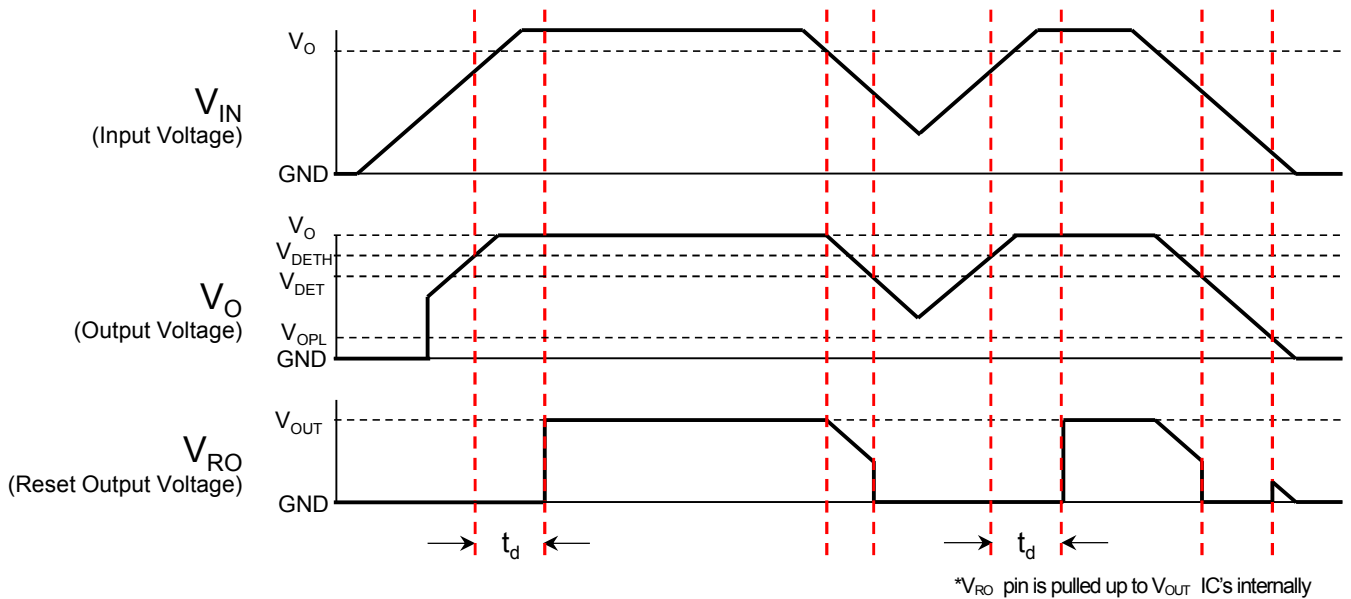
(*6): Mounted on glass epoxy board. (76.2 × 114.3 × 1.6mm:based on EIA/JDEC standard, 4Layers)

(For 4Layers: Applying 74.2 × 74.2mm inner Cu area and thermal via holes to a board based on JEDEC standard JESD51-5)

■ POWER DISSIPATION vs. AMBIENT TEMPERATURE



■ TIMING CHART



- RESET Output Delay Hold Time t_d

The NJW4116 has the RESET Output Delay Hold Time t_d till the RESET outputs "H" in order to prevent malfunction due to chattering after the Output Voltage V_O exceeds the RESET release voltage V_{DETH} ($=V_{DET}+V_{HYS}$).

The t_d is decided by capacitance connected to Cd pin as follows:

$$\text{External delay capacitor [nF]} = (\text{Required}) \text{ RESET Delay Hold Time } t_d [\text{ms}] / 10[\text{ms}] \times 4.7[\text{nF}]$$

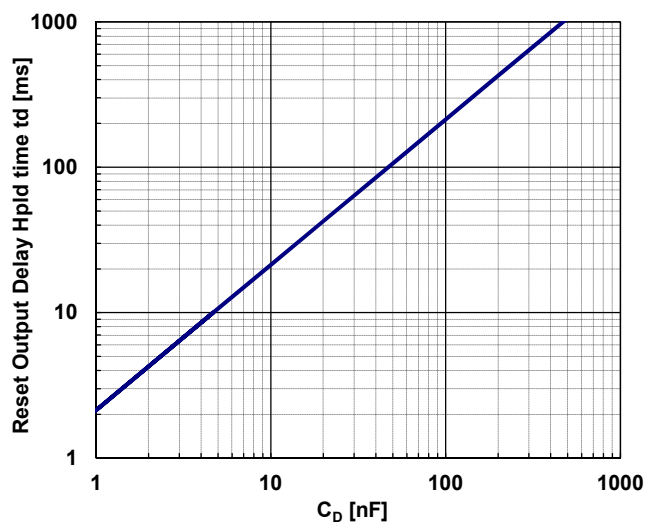
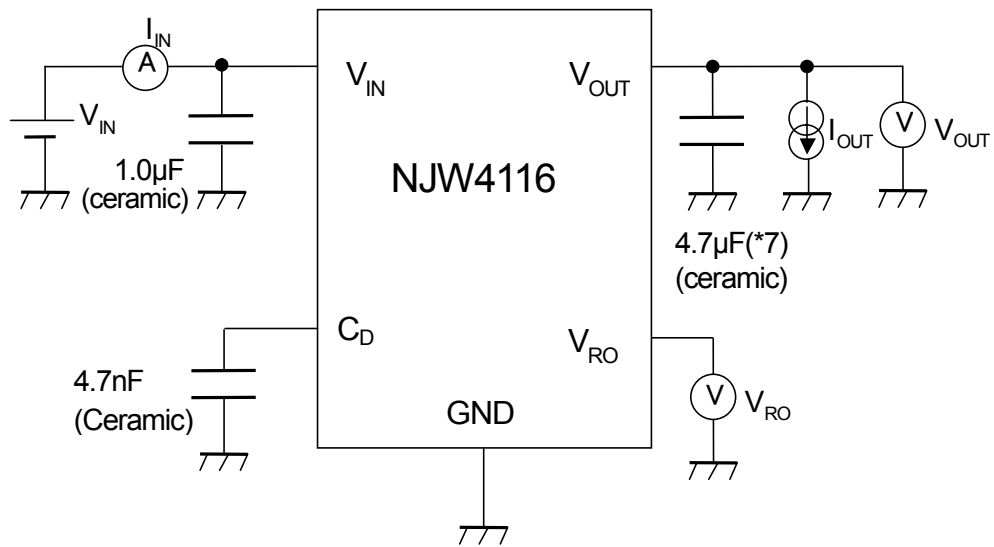


Fig.1) RESET Output Delay Hold Time vs External delay capacitor C_D

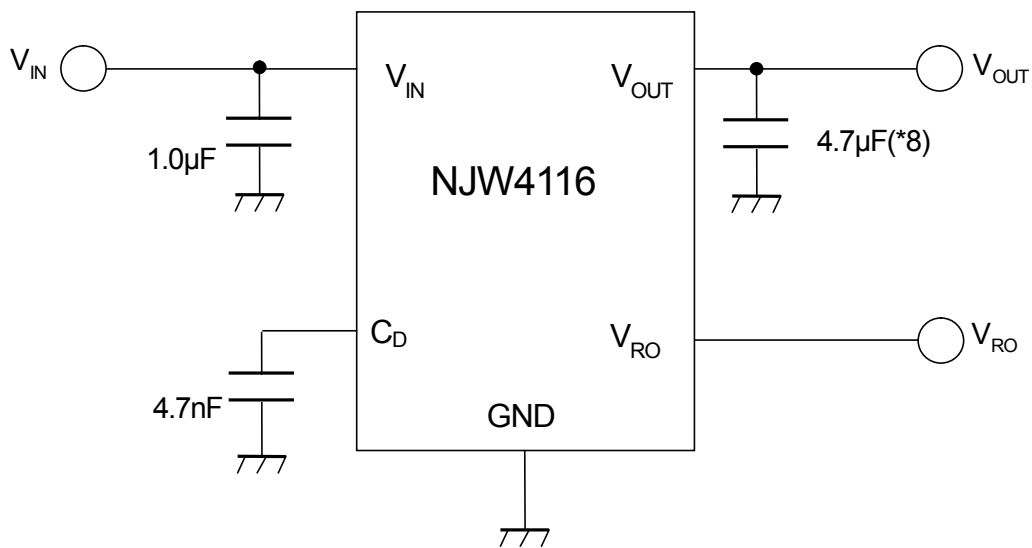
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TEST CIRCUIT



(*7) $V_o < 3.4\text{V}$ version : $C_o = 10\mu\text{F}$

TYPICAL APPLICATION



(*8) $V_o < 3.4\text{V}$ version : $C_o = 10\mu\text{F}$

*Input Capacitor C_{IN}

The input capacitor C_{IN} is required in order to prevent oscillation and reduce power supply ripple of applications when high power supply impedance or a long power supply line.

Therefore, the recommended capacitance (refer to conditions of ELECTRIC CHARACTERISTIC) or larger input capacitor, connected between V_{IN} and GND as short path as possible, is recommended in order to avoid the problem.

*Output Capacitor C_O

The output capacitor C_O is required for a phase compensation of the internal error amplifier, and the capacitance and the equivalent series resistance (ESR) influence stable operation of the regulator.

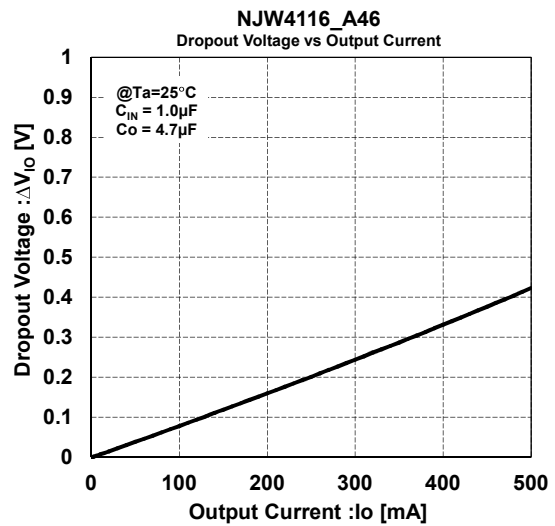
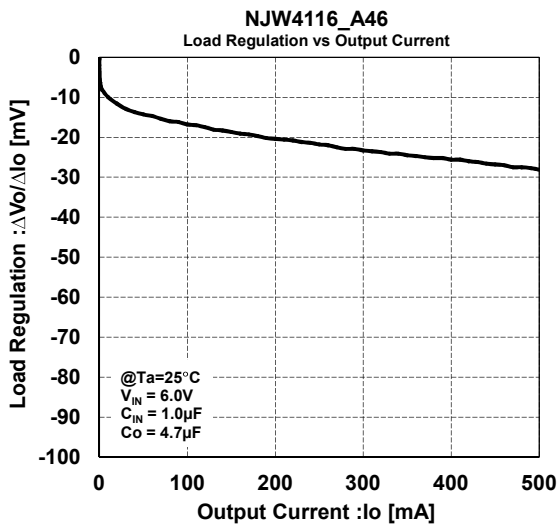
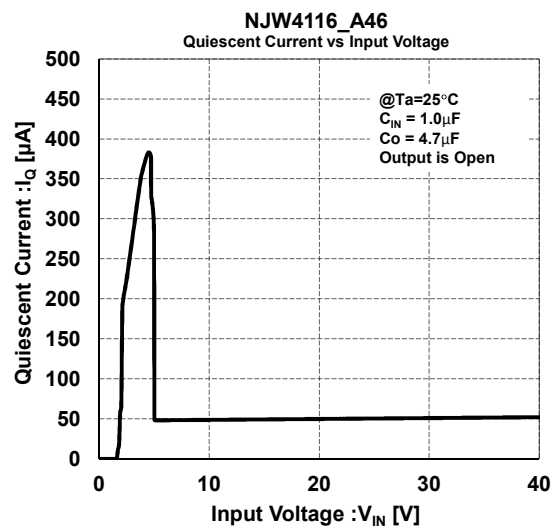
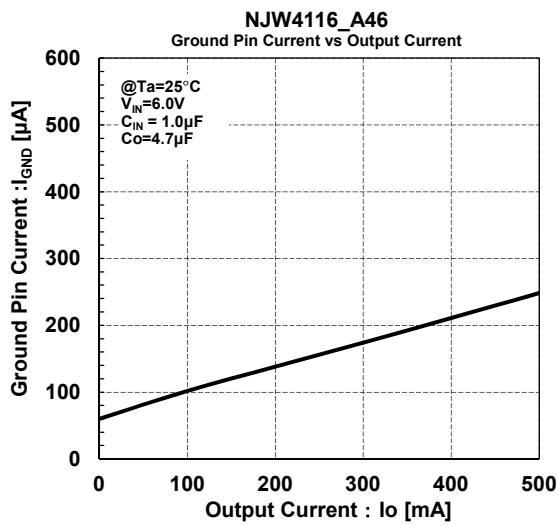
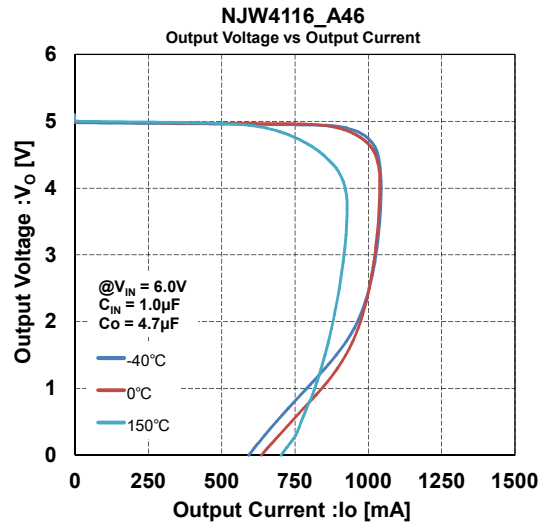
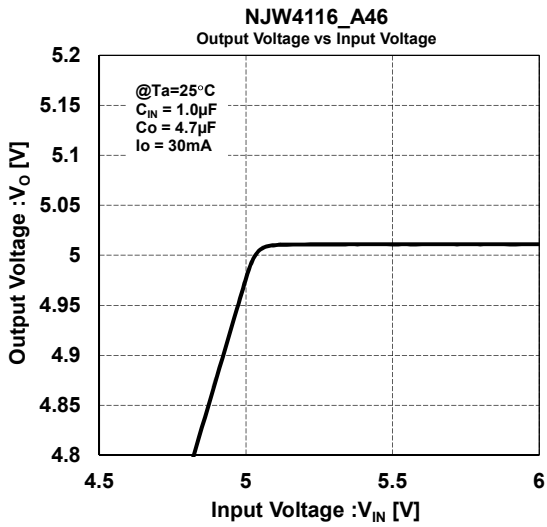
If use a smaller output capacitor than the recommended capacitance (refer to conditions of ELECTRIC CHARACTERISTIC), it may cause excess output noise or oscillation of the regulator due to lack of the phase compensation. Therefore, the recommended capacitance or larger output capacitor, connected between V_{OUT} and GND as short path as possible, is recommended for stable operation. The recommended capacitance may be different by output voltage, therefore confirm the recommended capacitance of the required output voltage.

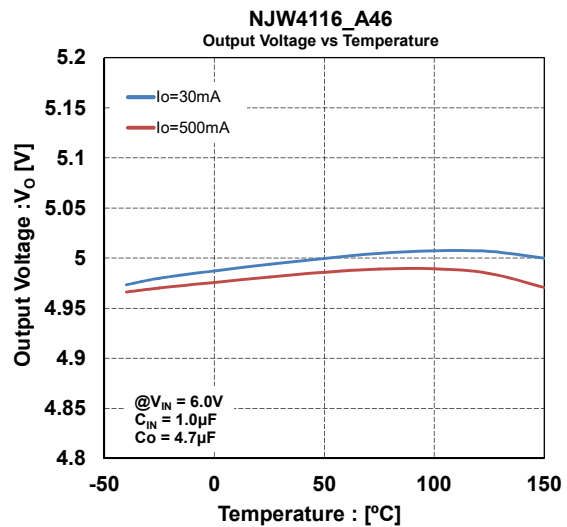
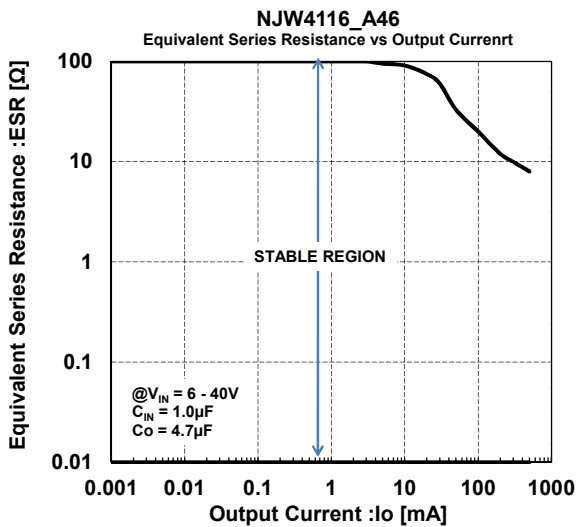
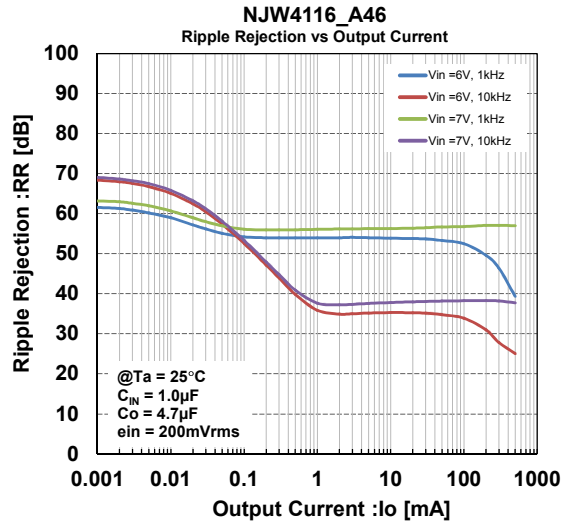
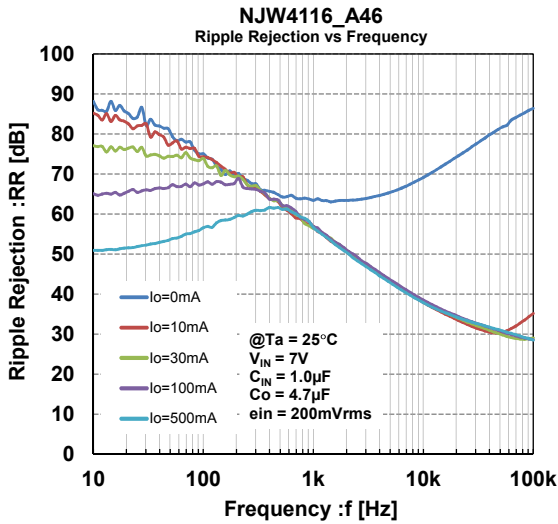
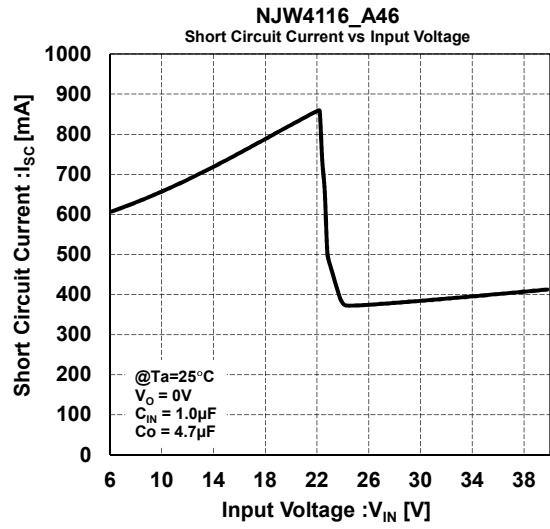
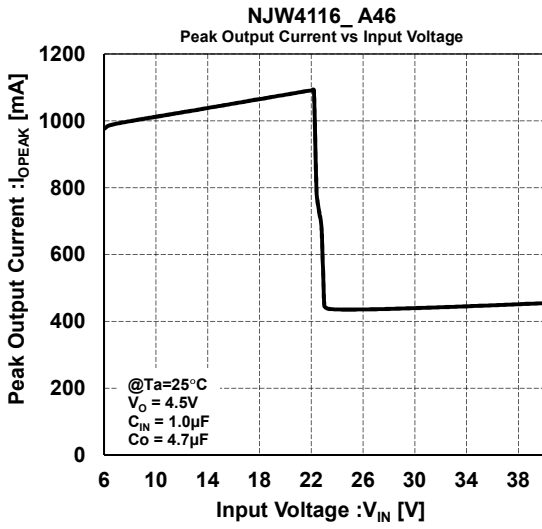
Furthermore, a larger output capacitor reduces output noise and ripple output, and also improves Output Transient Response when a load changes rapidly.

Selecting the output capacitor, should consider varied characteristics of a capacitor: frequency characteristics, temperature characteristics, DC bias characteristics and so on. Therefore, the capacitor that has a sufficient margin of the rated voltage against the output voltage and superior temperature characteristics, is recommended for C_O .

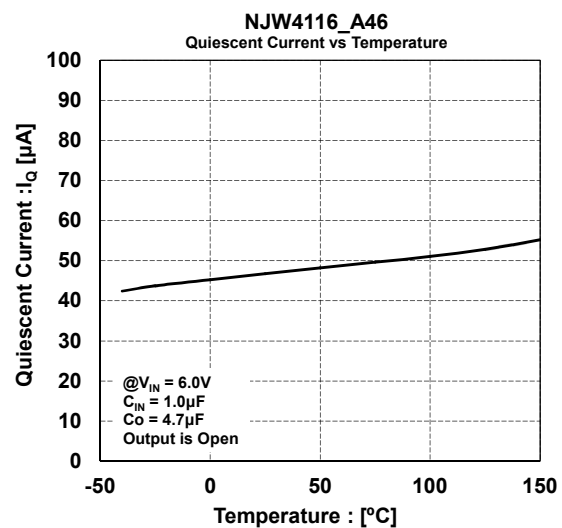
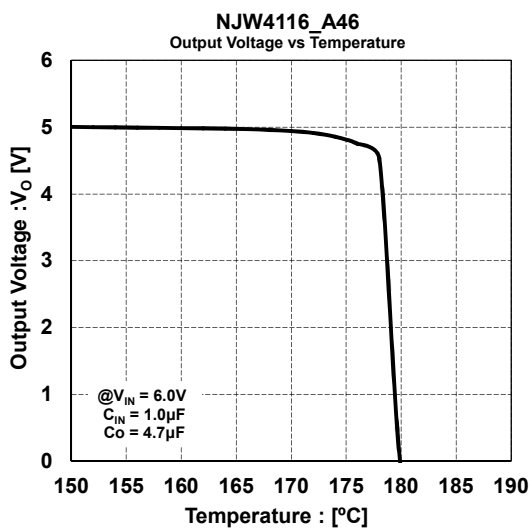
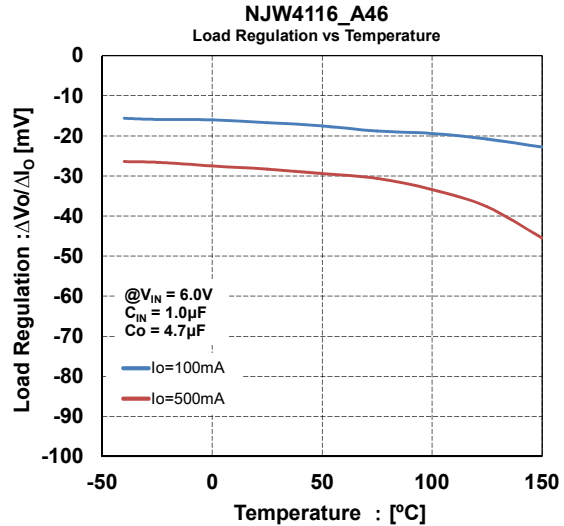
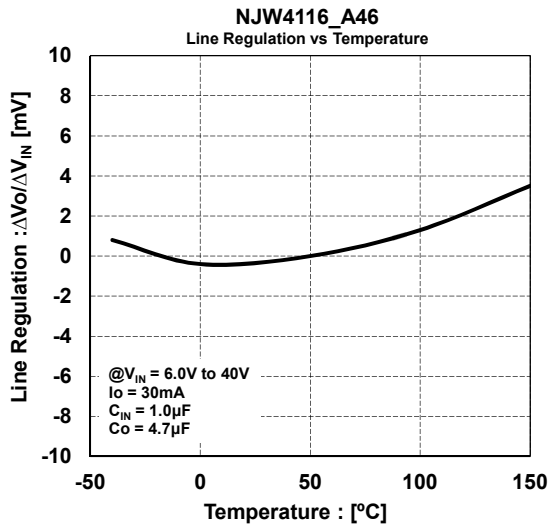
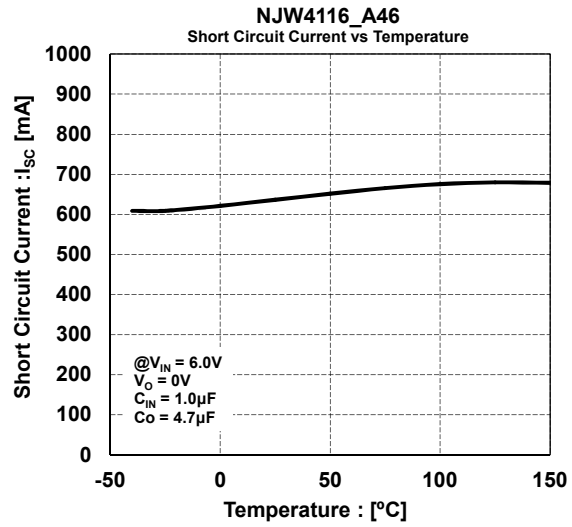
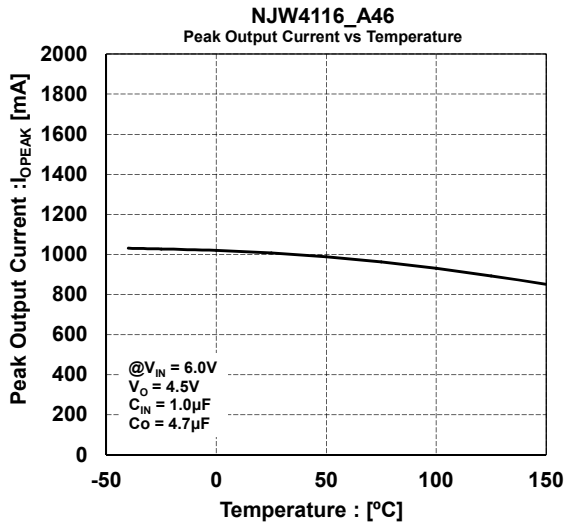
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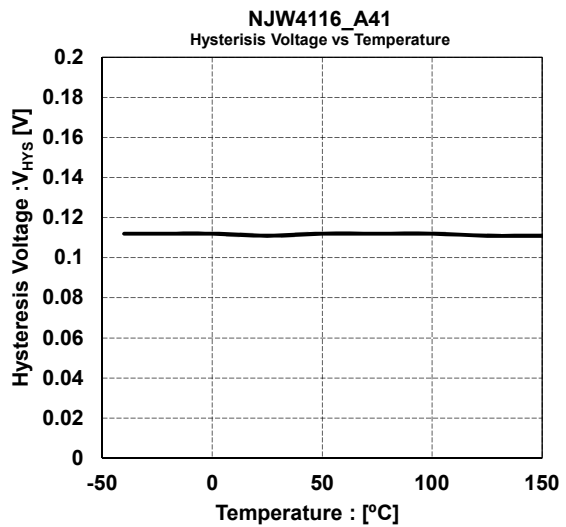
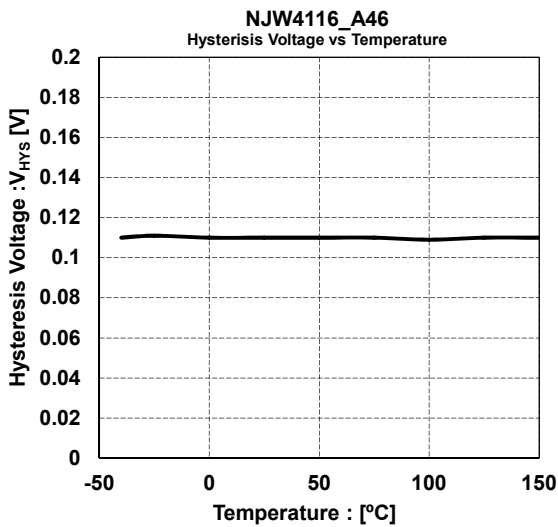
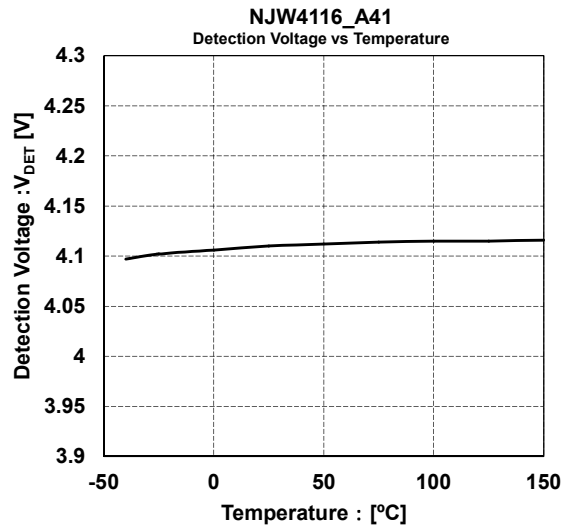
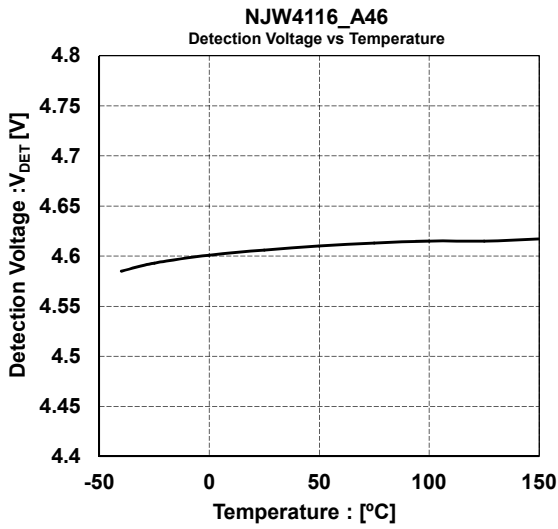
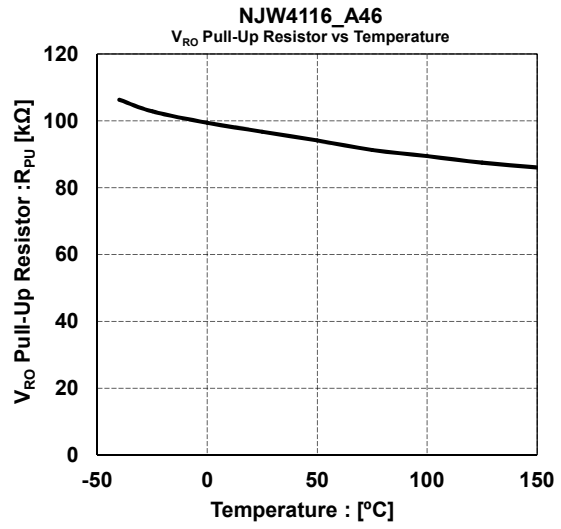
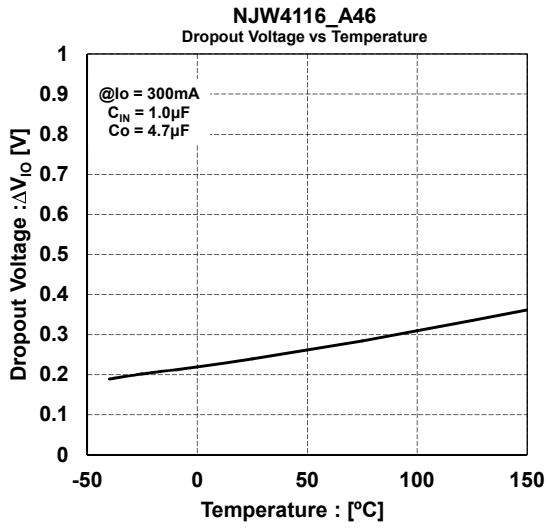
■ TYPICAL CHARACTERISTICS



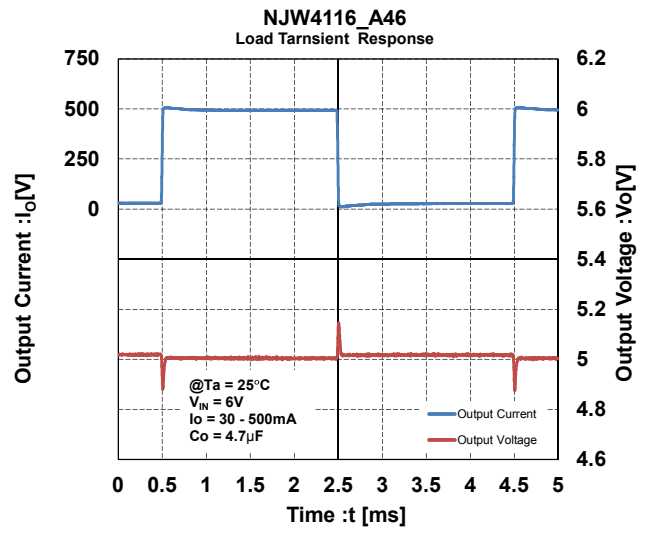
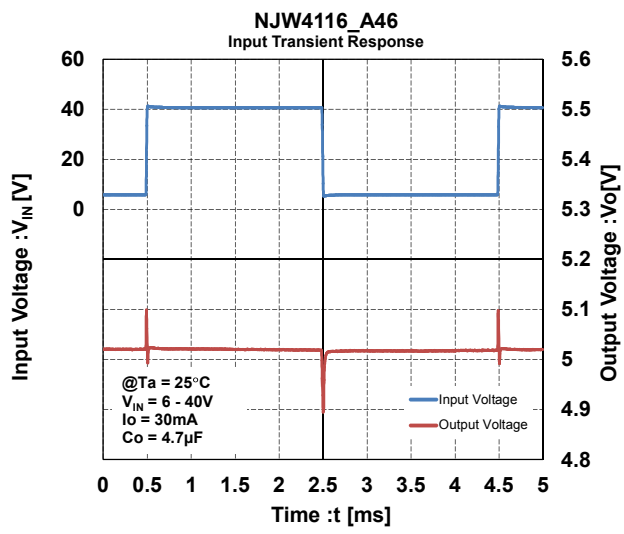


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