20V/µs, 10nV/√Hz, JFET Input Operational Amplifier

■ FEATURES (V+ / V− = ±15V, Typical value)

- High Slew Rate 20V/µs
- Low Noise 10nV/√Hz
- Low Distortion 0.0004%
- Gain Bandwidth 7MHz
- Supply Current at All Amplifiers 2.6mA
- High EMI Immunity EMIRR = 82dB (f = 1.8GHz)
- No Phase Reversal over Input Voltage Range
- Output Voltage close to V- Supply.
  - R_L = 2kΩ -14.8V to 14.1V
  - R_L = 600Ω -14.3V to 13.9V
- Common-Mode Input Voltage range -12.5V to 12.5V
- Supply Voltage ±4V to ±16V
- Unity-Gain Stable
- Package SOP8 (EMP8)

■ APPLICATIONS

- Sensor Amplifiers
- Amplifier for musical instruments
- Photodiode amplifier
- Active Filters

■ DESCRIPTION

NJM8087 is a JFET-Input high speed, low noise, low distortion operational amplifier achieved for high speed and high voltage applications.

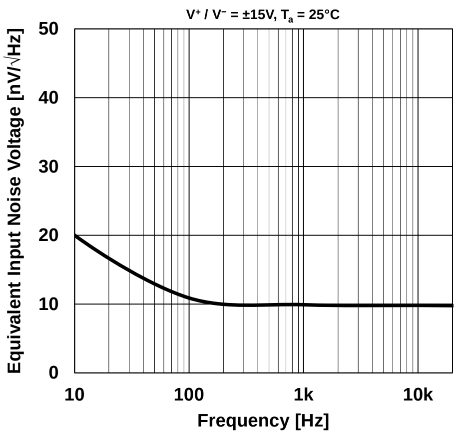
The features of 20V/µs slew rate, 10nV/√Hz noise, 0.0004% THD+N, 25pA input bias current and 2.6mA low supply current, make the NJM8087 ideal for various high performance applications.

NJM8087 operates dual supply range of ±4 to ±16V or single supply range of 8V to 32V. NJM8087 is unity gain stable for capacitive loads of 1000pF, and no phase reversal over input voltage which is up to supply range beyond the common mode range. Furthermore, low saturation output allows increasing dynamic range.

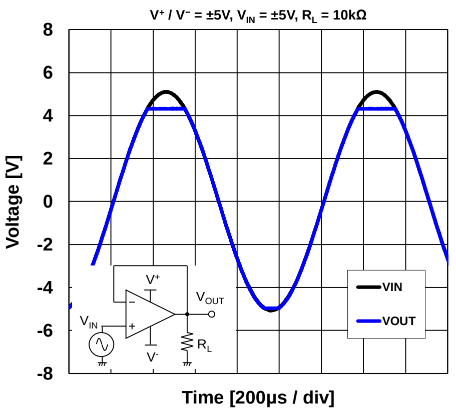
NJM8087 has high EMI immunity that can reduced malfunctions caused by R_F-noises from mobile phones and other electronic devices. This device operates from -40°C to 125°C, available in SOP8 (EMP8) package.

■ TYPICAL CHARACTERISTICS

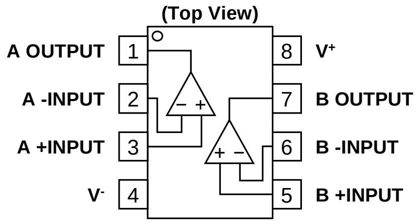
Low Noise
10nV/√Hz at f = 1kHz



No Phase Reversal
Over Input Voltage Range



■ PIN CONFIGURATION

PRODUCT NAME	NJM8087E
Package	SOP8 (EMP8)
Pin Functions	

■ PRODUCT NAME INFORMATION

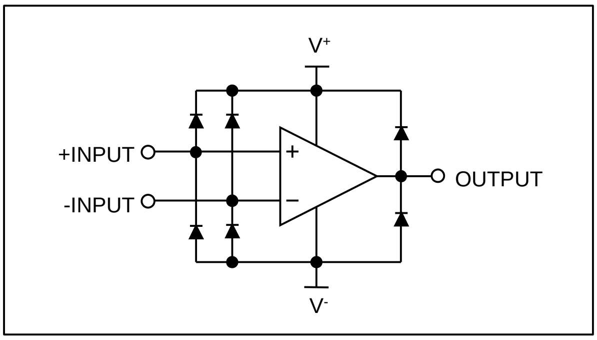
NJM8087 E (TE1)

Part Number — NJM8087
Package — E
Taping Form — (TE1)

■ ORDERING INFORMATION

PRODUCT NAME	PACKAGE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ (pcs)
NJM8087E (TE1)	SOP8 (EMP8)	Yes	Yes	Sn2Bi	8087	76	2000

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V^+ / V^-	±18	V
Input Voltage (1)	V_{IN}	$V^- - 0.3$ to $V^+ + 0.3$	V
Input Current (1)	I_{IN}	10	mA
Differential Input Voltage (2)	V_{ID}	±36	V
Output Short-Circuit Duration		Continuous ($T_a \leq 25°C$)	
Power Dissipation ($T_a = 25°C$)	P_D	2-Layer / 4-Layer (3)	
SOP8 (EMP8)		700 / 1000	mW
Storage Temperature	T_{stg}	-65 to 150	°C
Junction Temperature	T_j	150	°C

(1) Input voltages outside the supply voltage will be clamped by ESD protection diodes. If the input voltage exceeds the supply voltage, the current must be limited 10 mA or less by using a restriction resistance.
The normal operation will establish when any input is within the "Common-Mode Input Voltage Range" of electrical characteristics.
(2) Differential voltage is the voltage difference between +INPUT and −INPUT.
(3) 2-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 2-layer FR-4).
4-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 4-layer FR-4), internal Cu area: 74.2 mm × 74.2 mm.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNIT
Supply Voltage	V^+ / V^-	$T_a = 25°C$	±4 to ±16	V
Operating Temperature	T_{opr}		-40 to 125	°C

■ ELECTRICAL CHARACTERISTICS

($V^+ / V^- = \pm15V$, $V_{COM} = 0V$, $R_L = 2k\Omega$, $T_a = 25°C$, unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
Input Offset Voltage	V_{IO}		-	0.1	0.8	mV
Input Bias Current	I_B		-	25	80	pA
Input Offset Current	I_{IO}		-	6	75	pA
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$	$T_a = -40°C$ to $125°C$	-	1	-	μV/°C
Input Capacitance	C_{IN}		-	10	-	pF
Open-Loop Voltage Gain	A_V	$R_L = 2k\Omega$, $V_O = -13.5V$ to $13.5V$	90	100	-	dB
Common-Mode Rejection Ratio	CMR	$V_{ICM} = -12.5V$ to $12.5V$	86	108	-	dB
Common-Mode Input Voltage Range	V_{ICM}	CMR ≥ 86dB	-12.5	-	12.5	V
OUTPUT CHARACTERISTICS						
High-level Output Voltage	V_{OH}	$R_L = 2k\Omega$	13.8	14.1	-	V
		$R_L = 600\Omega$	13.5	13.9	-	V
Low-level Output Voltage	V_{OL}	$R_L = 2k\Omega$	-	-14.8	-14.4	V
		$R_L = 600\Omega$	-	-14.3	-13.8	V
Output Short-Circuit Current	I_{SC}	Sourcing, $V_O = 0V$	-	62	-	mA
		Sinking, $V_O = 0V$	-	50	-	mA
POWER SUPPLY						
Supply Current (All Amplifiers)	I_{SUPPLY}	No Signal	-	2.6	3.0	mA
Supply Voltage Rejection Ratio	SVR	$V^+ / V^- = \pm4V$ to $\pm16V$	86	110	-	dB
AC CHARACTERISTICS						
Slew Rate	SR	Gain = 1, $V_{IN} = 2V_{PP}$	-	20	-	V/μs
Unity Gain Frequency	f_T	$C_L = 10pF$	-	7	-	MHz
Settling Time	t_S	0.1%, 10V step, Gain = 1	-	0.7	-	μs
Settling Time	t_S	0.01%, 10V step, Gain = 1	-	1	-	μs
Phase Margin	Φ_M	$C_L = 10pF$	-	70	-	Deg
Total Harmonic Distortion + Noise	THD+N	Gain = 1, f = 1kHz, $V_O = 3Vrms$	-	0.0004	-	%
Equivalent Input Noise Voltage	V_{NI}	f = 0.1Hz to 10Hz	-	0.9	-	μV_{PP}
	e_n	f = 1kHz	-	10	-	nV/√Hz
Channel Separation	CS	f = 1kHz	-	138	-	dB

■ ELECTRICAL CHARACTERISTICS

($V^+ / V^- = \pm5V$, $V_{COM} = 0V$, $R_L = 2k\Omega$, $T_a = 25°C$, unless otherwise noted.)

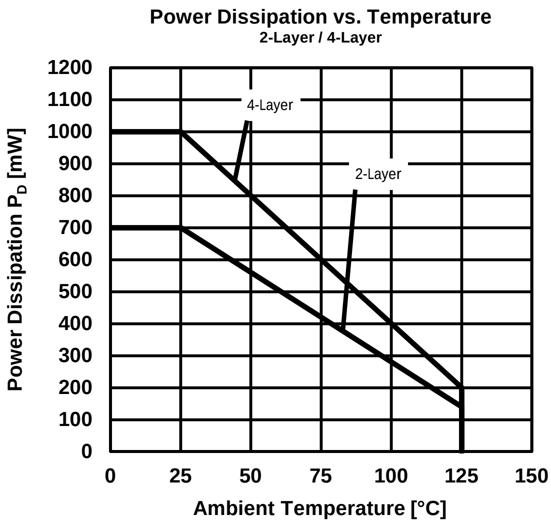
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
Input Offset Voltage	V_{IO}		-	0.1	0.8	mV
Input Bias Current	I_B		-	21	-	pA
Input Offset Current	I_{IO}		-	5	-	pA
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$	$T_a = -40°C$ to $125°C$	-	1	-	µV/°C
Input Capacitance	C_{IN}		-	10	-	pF
Common-Mode Rejection Ratio	CMR	$V_{ICM} = -2.5V$ to $2.5V$	86	108	-	dB
Common-Mode Input Voltage Range	V_{ICM}	CMR ≥ 86dB	-2.5	-	2.5	V
OUTPUT CHARACTERISTICS						
High-level Output Voltage	V_{OH}	$R_L = 2k\Omega$	3.9	4.2	-	V
		$R_L = 600\Omega$	3.7	4.1	-	V
Low-level Output Voltage	V_{OL}	$R_L = 2k\Omega$	-	-4.9	-4.5	V
		$R_L = 600\Omega$	-	-4.8	-4.3	V
Output Short-Circuit Current	I_{SC}	Sourcing, $V_O = 0V$	-	52	-	mA
		Sinking, $V_O = 0V$	-	44	-	mA
POWER SUPPLY						
Supply Current (All Amplifiers)	I_{SUPPLY}	No Signal	-	2.0	3.0	mA
AC CHARACTERISTICS						
Slew Rate	SR	Gain = 1, $V_{IN} = 2V_{PP}$	-	18	-	V/µs
Unity Gain Frequency	f_T	$C_L = 10pF$	-	7	-	MHz
Settling Time	t_s	0.1%, 4V step, Gain = 1	-	0.5	-	µs
Phase Margin	Φ_M	$C_L = 10pF$	-	65	-	Deg
Total Harmonic Distortion + Noise	THD+N	Gain = 1, f = 1kHz, $V_O = 1Vrms$	-	0.0005	-	%
Equivalent Input Noise Voltage	V_{NI}	f = 0.1Hz to 10Hz	-	0.9	-	$µV_{PP}$
	e_n	f = 1kHz	-	10	-	nV/√Hz
Channel Separation	CS	f = 1kHz	-	135	-	dB

■ THERMAL CHARACTERISTICS

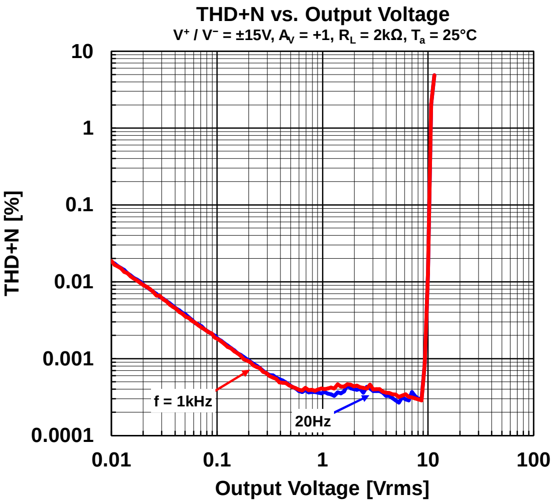
PACKAGE	SYMBOL	VALUE	UNIT
Junction-to-Ambient Thermal Resistance SOP8 (EMP8)	θ_{ja}	2-Layer / 4-Layer (4) 179 / 125	°C/W
Junction-to-Top of Package Characterization Parameter SOP8 (EMP8)	Ψ_{jt}	2-Layer / 4-Layer (4) 31 / 27	°C/W

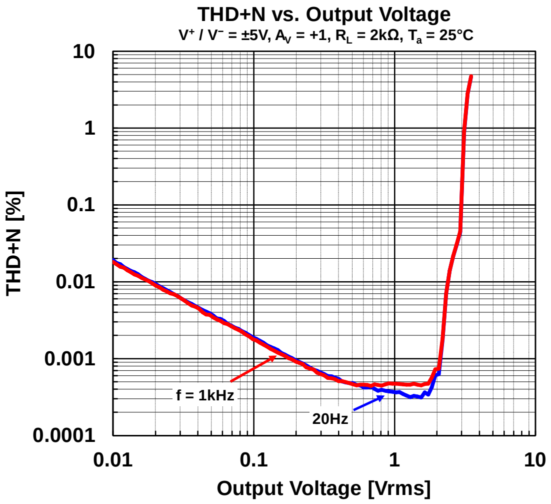
(4) 2-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 2-layer FR-4).
4-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 4-layer FR-4), internal Cu area: 74.2 mm × 74.2 mm.

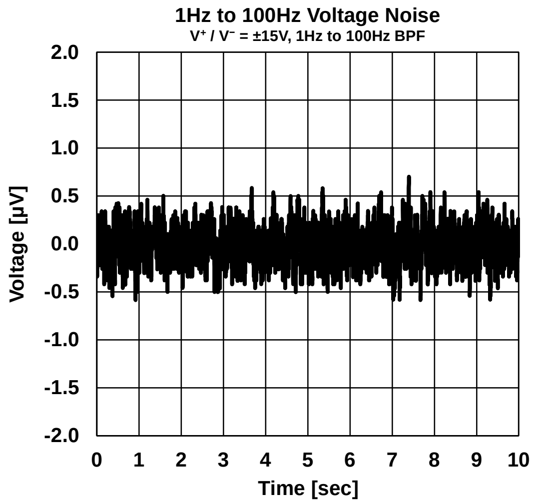
■ POWER DISSIPATION vs. AMBIENT TEMPERATURE

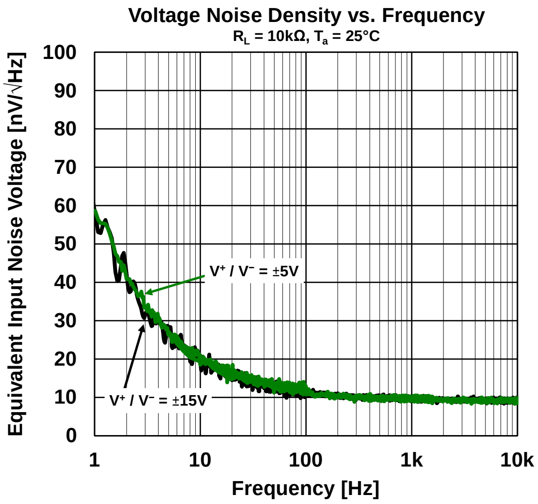


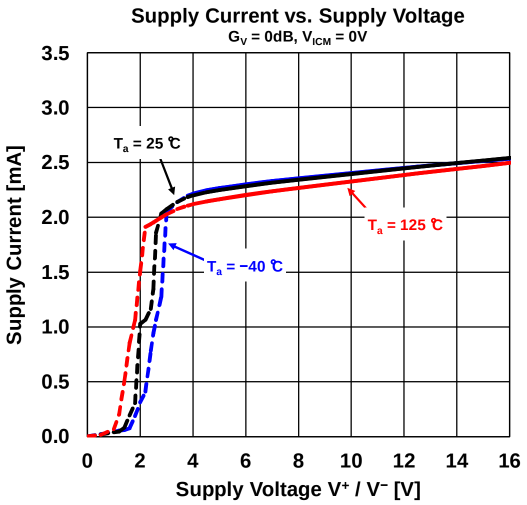
■ TYPICAL CHARACTERISTICS

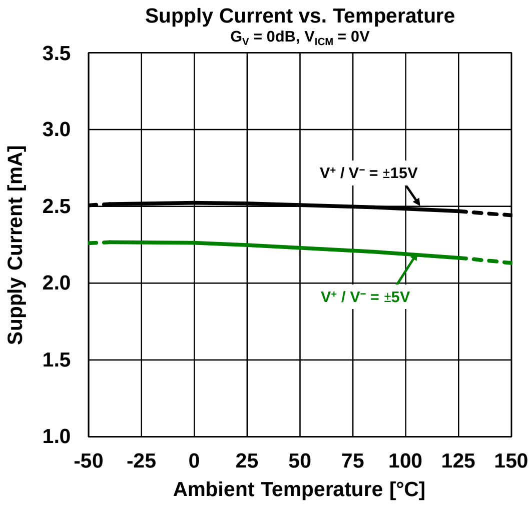




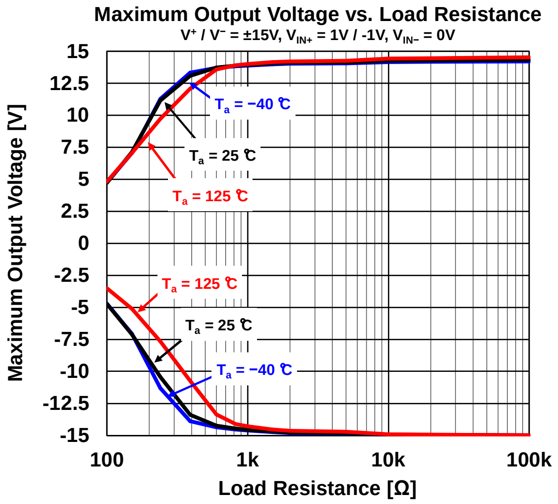


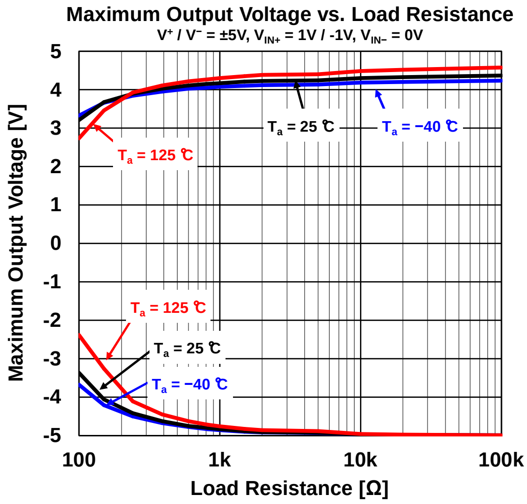


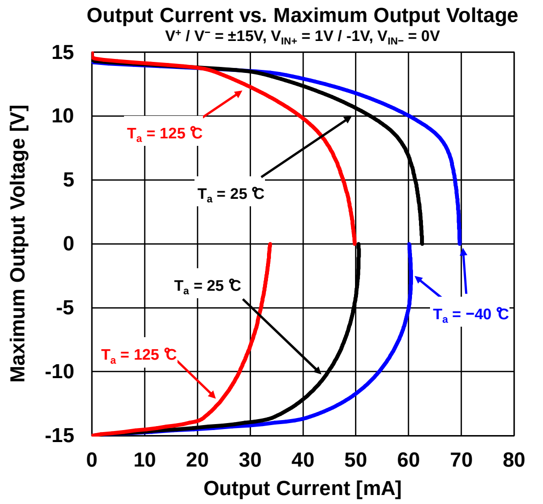


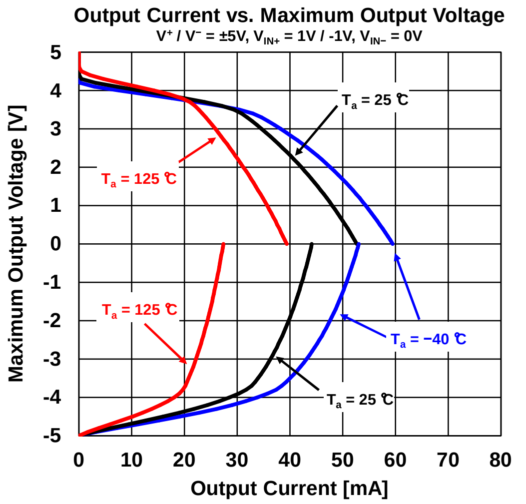


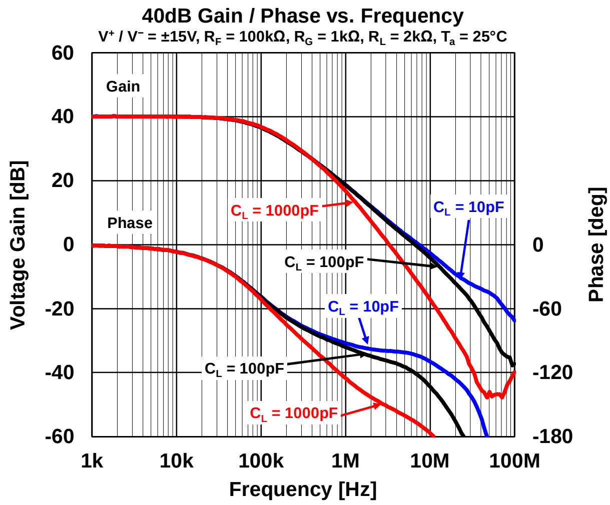
■ TYPICAL CHARACTERISTICS

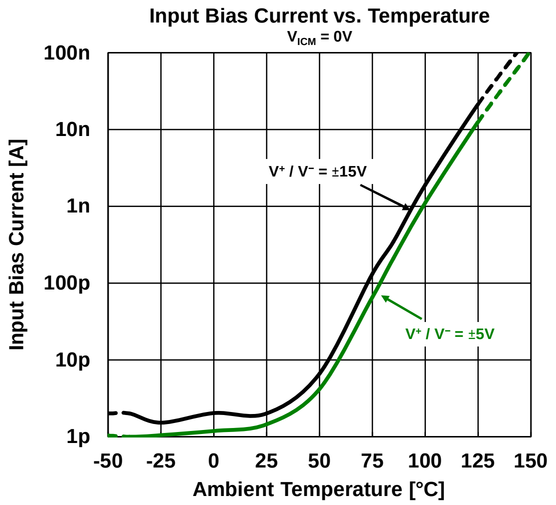






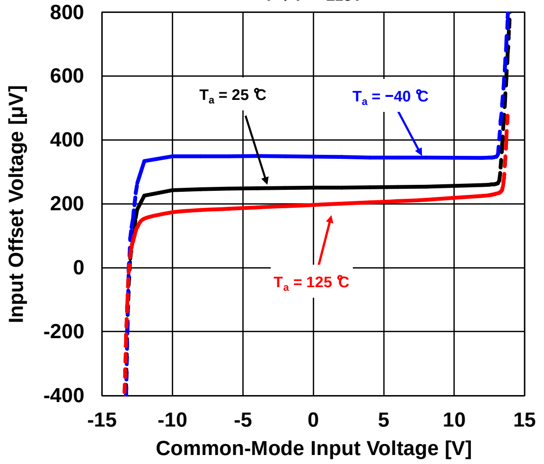




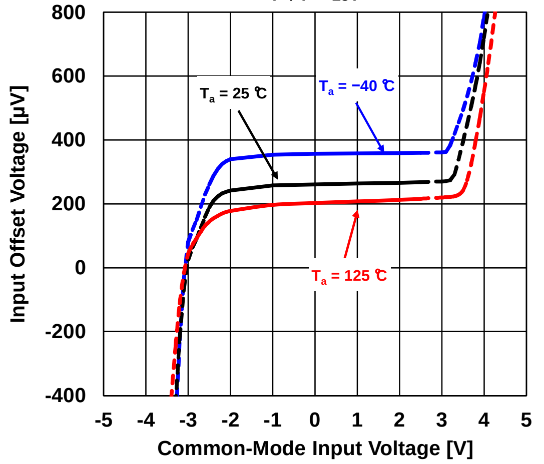


■ TYPICAL CHARACTERISTICS

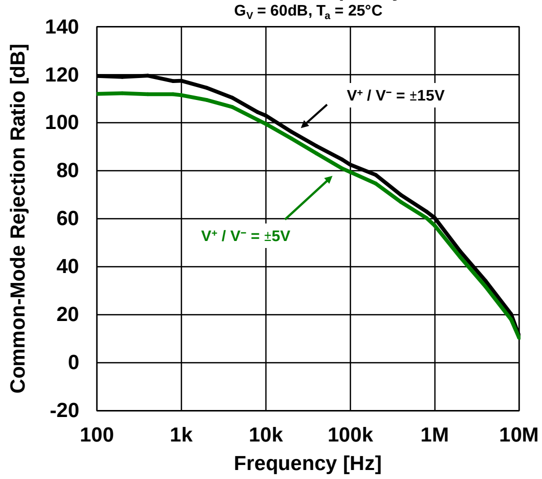
Input Offset Voltage vs. Common-Mode Input Voltage
$V^+ / V^- = \pm 15V$



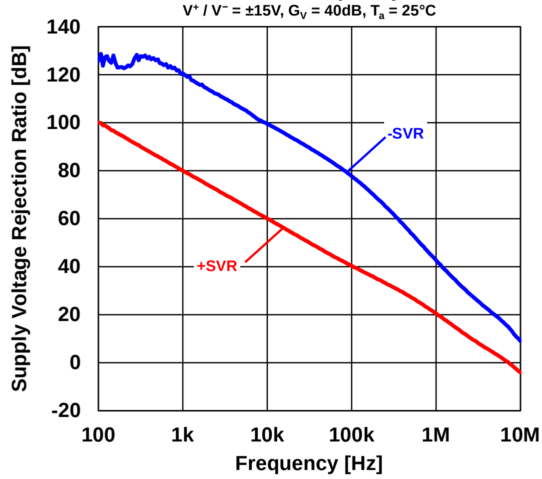
Input Offset Voltage vs. Common-Mode Input Voltage
$V^+ / V^- = \pm 5V$



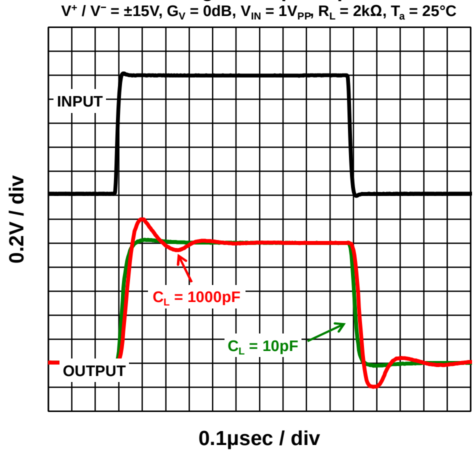
CMR vs. Frequency
$G_V = 60dB, T_a = 25°C$



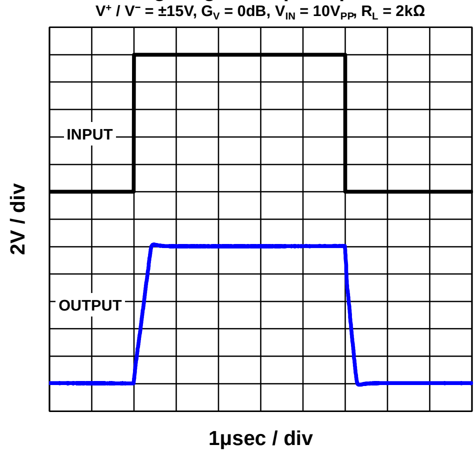
SVR vs. Frequency
$V^+ / V^- = \pm 15V, G_V = 40dB, T_a = 25°C$



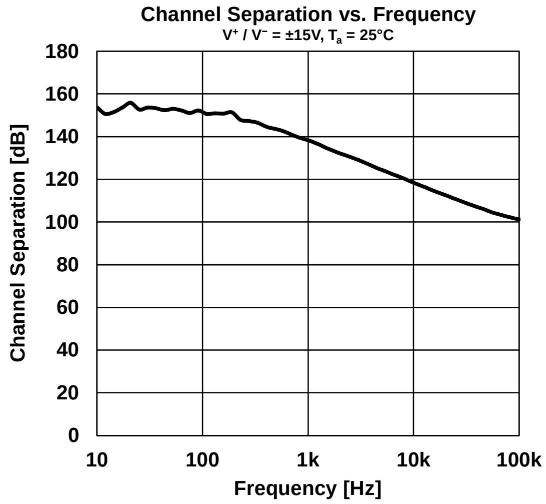
Small-Signal Step Response
$V^+ / V^- = \pm 15V, G_V = 0dB, V_{IN} = 1V_{PP}, R_L = 2k\Omega, T_a = 25°C$

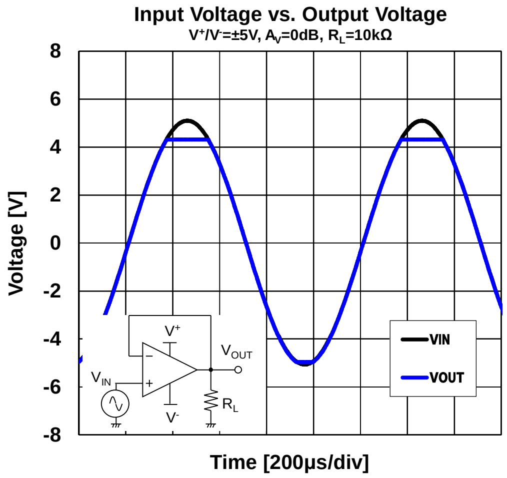


Large-Signal Step Response
$V^+ / V^- = \pm 15V, G_V = 0dB, V_{IN} = 10V_{PP}, R_L = 2k\Omega$



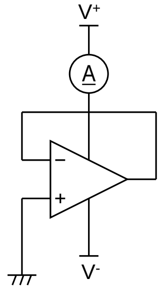
■ TYPICAL CHARACTERISTICS





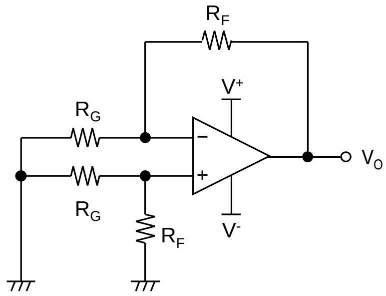
■ TEST CIRCUITS

● I_{SUPPLY}



● V_{IO}, CMR, SVR

R_G=50Ω, R_F=50kΩ



$$V_{IO}=\frac{R_G}{(R_G+R_F)}\times V_O$$

$$CMR=20\log\frac{\Delta V_{COM}\left(1+\frac{R_F}{R_G}\right)}{\Delta V_O}$$

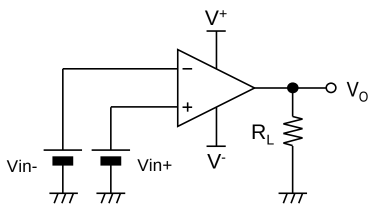
$$SVR=20\log\frac{\Delta V_S\left(1+\frac{R_F}{R_G}\right)}{\Delta V_O}$$

$V_S=V^+-V^-$

● V_{OH}, V_{OL}

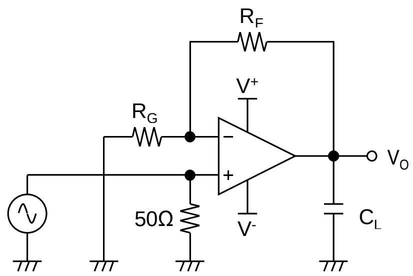
V_{OH}; Vin+ = 1V, Vin- =0V

V_{OL}; Vin+ = -1V, Vin- =0V



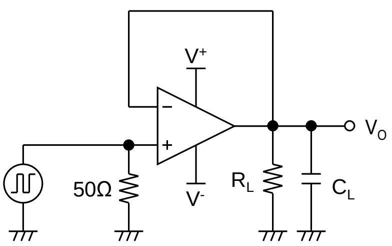
● GBW

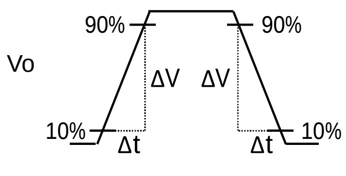
R_G=100Ω, R_F=10kΩ, C_L=open



● SR

R_L=2kΩ, C_L=10pF





$$SR=\frac{\Delta V}{\Delta t}$$

■ APPLICATION NOTE

Single and Dual Supply Voltage Operation

The NJM8087 works with both single supply and dual supply when the voltage supplied is between V^+ and V^-. These amplifiers operate from single 8V to 32V supply and dual ±4V to ±16V supply.

Common-Mode Input Voltage Range

When the supply voltage does not meet the condition of electrical characteristics, the range of common-mode input voltage is as follows:

V_{ICM} (typ.) = V^-+2.5V to V^+-2.5V (Ta = 25°C)

Difference of V_{ICM} when Temperature change, refer to typical characteristic graph.

During designing, consider variations in characteristics for use with allowance.

Maximum Output Voltage Range

When the supply voltage does not meet the condition of electrical characteristics, the range of the typ. value of the maximum output voltage is as follows:

V_{OM} (typ.) = V^-+0.2V to V^+-0.9V (R_L=2kΩ to V^+/2, Ta=25°C)

During designing, consider variations in characteristics and temperature characteristics for use with allowance. In addition, also note that the output voltage range becomes narrow as shown in typical characteristics graph when an output current increases.

No Phase Reversal

The NJM8087 is designed to prevent phase reversal at the input voltage above the common mode input voltage range. Figure1 shows no phase reversal characteristics with the input voltage exceeding the supply voltage. It is designed to prevent phase reversal at the input voltage above the supply voltage, but the input voltage should not exceed the absolute maximum rating of V^--0.3V or V^++0.3V. The range of normal operation is the common mode input voltage range shown in the electrical characteristics table.

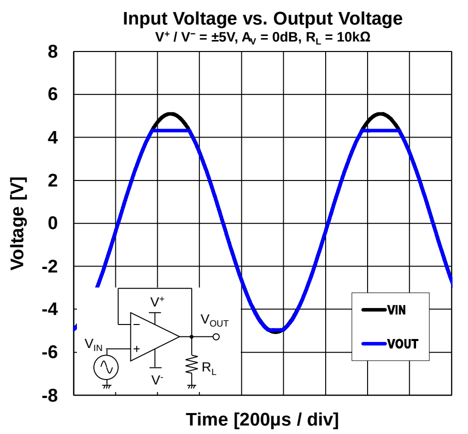


Figure1. No phase reversal

Capacitive load

The NJM8087 can use at unity gain follower, but the unity gain follower is the most sensitive configuration to capacitive loading. The combination of capacitive load placed directly on the output of an amplifier along with the output impedance of the amplifier creates a phase lag which in turn reduces the phase margin of the amplifier. If phase margin is significantly reduced, the response will cause overshoot and ringing in the step response.

The NJM8087 is unity gain stable for capacitive loads of 1000pF. To drive heavier capacitive loads, an isolation resistor, R_{ISO} as shown Figure2, should be used. R_{ISO} improves the feedback loop's phase margin by making the output load resistive at higher frequencies. The larger the value of R_{ISO}, the more stable the output voltage will be. However, larger values of R_{ISO} result in reduced output swing, reduced output current drive and reduced frequency bandwidth.

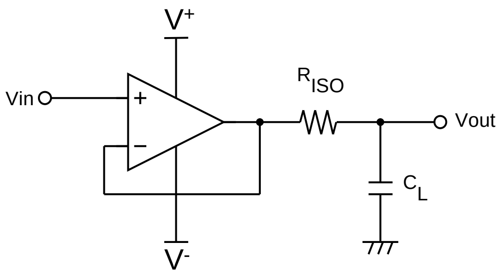


Figure2. Isolating capacitive load

■ APPLICATION NOTE

EMIRR (EMI Rejection Ratio) Definition

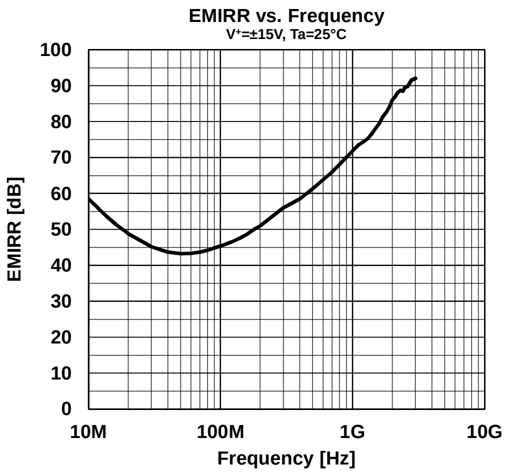
EMIRR is a parameter indicating the EMI robustness of an OpAmp. The definition of EMIRR is given by the following equation1.

$$EMIRR = 20 \cdot \log\left(\frac{V_{RF\_PEAK}}{|\Delta V_{IO}|}\right) \qquad \text{--- eq.1}$$

V_{RF_PEAK}: RF Signal Amplitude [V_P]

ΔV_{IO}: Input offset voltage shift quantity [V]

The tolerance of the RF signal can be grasped by measuring an RF signal and offset voltage shift quantity. Offset voltage shift is small so that a value of EMIRR is big. And it understands that the tolerance for the RF signal is high. In addition, about the input offset voltage shift with the RF signal, there is the thinking that influence applied to the input terminal is dominant. Therefore, generally the EMIRR becomes value that applied an RF signal to +INPUT terminal.

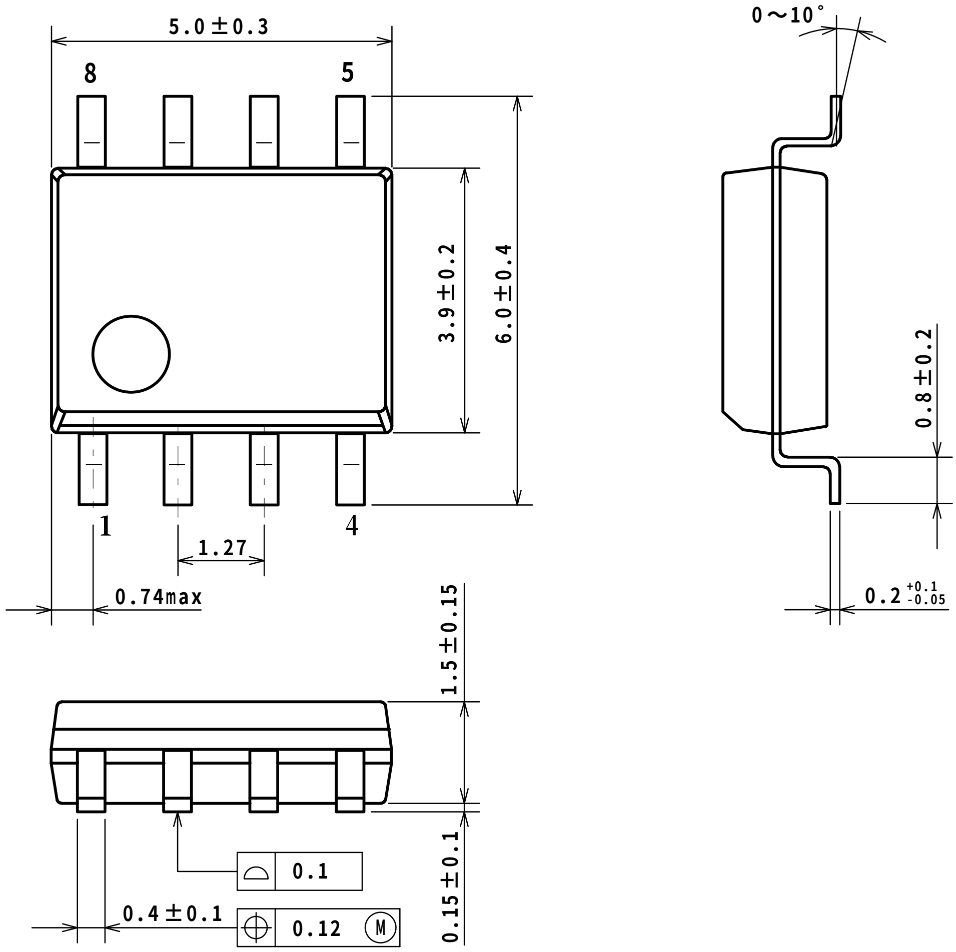


*For details, refer to “Application Note for EMI Immunity” in our HP: http://www.njr.com/

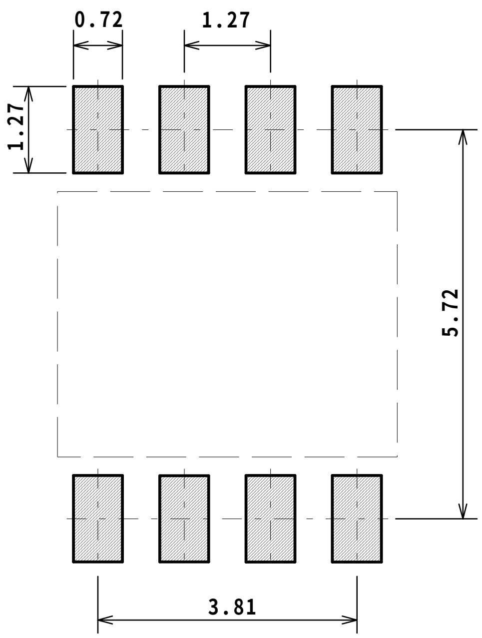
SOP (EMP8)

Unit: mm

■ PACKAGE DIMENSIONS



■ EXAMPLE OF SOLDER PADS DIMENSIONS

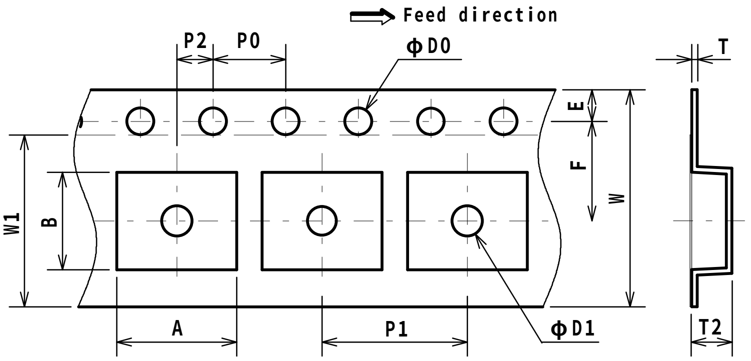


SOP8 (EMP8)

Unit: mm

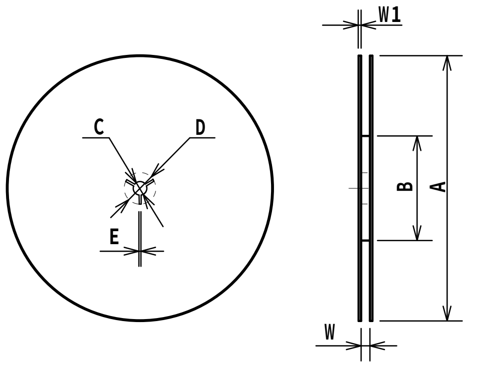
■ PACKING SPEC

TAPING DIMENSIONS



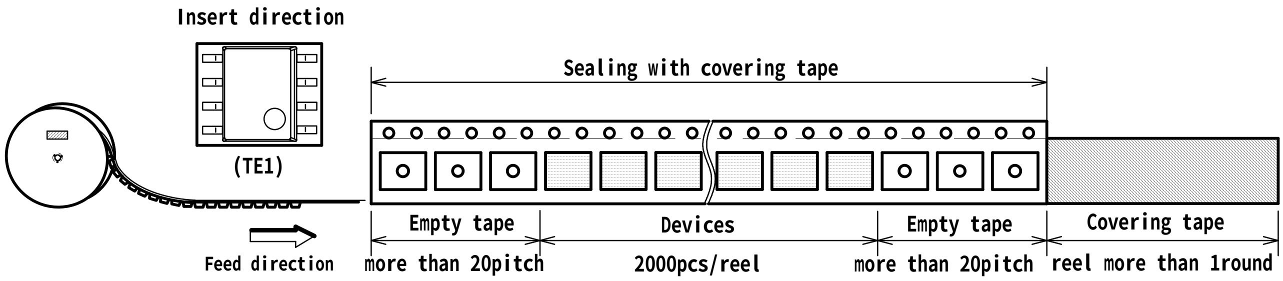
SYMBOL	DIMENSION	REMARKS
A	6.6	BOTTOM DIMENSION
B	5.4	BOTTOM DIMENSION
D0	$1.5^{+0.1}_{0}$	
D1	1.7±0.1	
E	1.75±0.1	
F	5.5±0.05	
P0	4.0±0.1	
P1	8.0±0.1	
P2	2.0±0.05	
T	0.30±0.05	
T2	2.2	
W	12.0±0.3	
W1	9.5	THICKNESS 0.1max

REEL DIMENSIONS

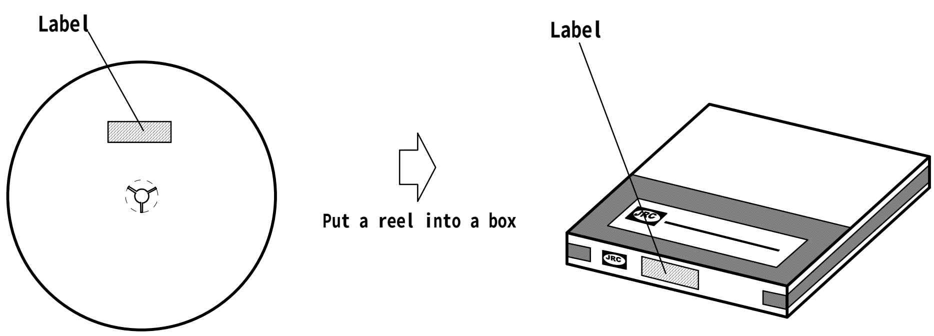


SYMBOL	DIMENSION
A	φ330±2
B	φ 80±1
C	φ 13±0.2
D	φ 21±0.8
E	2±0.5
W	13.5±0.5
W1	2.0±0.2

TAPING STATE

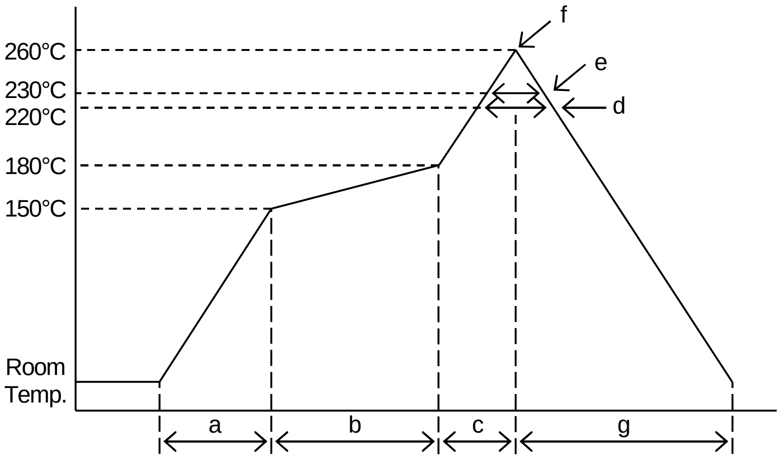


PACKING STATE



■ RECOMMENDED MOUNTING METHOD

INFRARED REFLOW SOLDERING PROFILE



a	Temperature ramping rate	1 to 4°C/s
b	Pre-heating temperature Pre-heating time	150 to 180°C 60 to 120s
c	Temperature ramp rate	1 to 4°C/s
d	220°C or higher time	shorter than 60s
e	230°C or higher time	shorter than 40s
f	Peak temperature	lower than 260°C
g	Temperature ramping rate	1 to 6°C/s

The temperature indicates at the surface of mold package.

■ REVISION HISTORY

DATE	REVISION	CHANGES
April 13, 2021	Ver.1.0	Initial release.

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   ・Equipment Used in the Deep Sea
   ・Power Generator Control Equipment (Nuclear, steam, hydraulic, etc.)
   ・Life Maintenance Medical Equipment
   ・Fire Alarms / Intruder Detectors
   ・Vehicle Control Equipment (Airplane, railroad, ship, etc.)
   ・Various Safety Devices

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9. The product specifications and descriptions listed in this datasheet are subject to change at any time, without notice.