

## High Isolation X-SP4T (DP8T) SWITCH

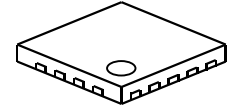
### ■ GENERAL DESCRIPTION

The NJG1695ME7 is a GaAs X (cross) - SP4T (DP8T) switch MMIC for switching of balanced (differential) mode filters. It features low insertion loss and very high isolation for balanced signal input.

The ESD protection circuits are integrated in the IC to achieve high ESD tolerance.

The ultra-small and ultra-thin EQFN18-E7 package is adopted.

### ■ PACKAGE OUTLINE



**NJG1695ME7**

\*) The X-SP4T is a paired SP4T switch that features two identical SP4T switches being integrated into one chip. The two SP4T switches are controlled synchronously, and their respective RF lines cross each other on the chip.

### ■ APPLICATIONS

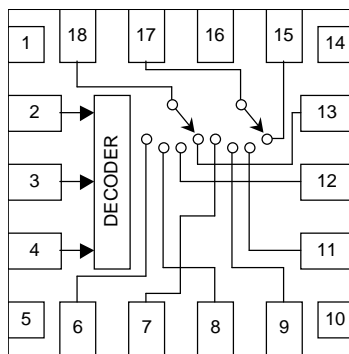
Switching of balanced type filters (Quad band) application  
Suitable for 3G and LTE application

### ■ FEATURES

- Low operation voltage       $V_{DD}=+1.5\sim+4.5V$
- Low control voltage       $V_{CTL(H)}=+1.35V$  min.
- High isolation  
(Balanced mode)      43dB typ.    @f=1.0GHz,  $P_{IN}=0dBm$   
   38dB typ.    @f=2.0GHz,  $P_{IN}=0dBm$   
   35dB typ.    @f=2.7GHz,  $P_{IN}=0dBm$
- Low insertion loss      0.45dB typ. @f=1.0GHz,  $P_{IN}=0dBm$   
   0.55dB typ. @f=2.0GHz,  $P_{IN}=0dBm$   
   0.80dB typ. @f=2.7GHz,  $P_{IN}=0dBm$
- Small package              EQFN18-E7 (Package size: 2.0mm x 2.0mm x 0.397mm typ.)
- RoHS compliant and Halogen Free
- MSL 1

### ■ PIN CONFIGURATION

(Top View)



- |          |             |
|----------|-------------|
| 1. GND   | 10. GND     |
| 2. VDD   | 11. P2B     |
| 3. VCTL2 | 12. P2A     |
| 4. VCTL1 | 13. P1A     |
| 5. GND   | 14. GND     |
| 6. P4A   | 15. P1B     |
| 7. P4B   | 16. GND(NC) |
| 8. P3A   | 17. PCB     |
| 9. P3B   | 18. PCA     |

### ■ TRUTH TABLE

“H”= $V_{CTL(H)}$ , “L”= $V_{CTL(L)}$

ON PATH	VCTL1	VCTL2
PCA-P1A, PCB-P1B	H	L
PCA-P2A, PCB-P2B	L	L
PCA-P3A, PCB-P3B	L	H
PCA-P4A, PCB-P4B	H	H

NOTE: The information on this datasheet is subject to change without notice.

## ■ ABSOLUTE MAXIMUM RATINGS

( $T_a=+25^{\circ}\text{C}$ ,  $Z_s=Z_l=50\Omega$ )

PARAMETERS	SYMBOL	CONDITIONS	RATINGS	UNITS
RF Input Power	$P_{IN}$	$V_{DD}=2.7\text{V}$ , $V_{CTL}=0\text{V}/1.8\text{V}$ ON state port	28	dBm
Supply Voltage	$V_{DD}$	VDD terminal	5.0	V
Control Voltage	$V_{CTL}$	VCTL terminal	5.0	V
Power Dissipation	$P_D$	Four-layer FR4 PCB with through-holes (74.2mmx74.2mm), $T_j=150^{\circ}\text{C}$	1400	mW
Operating Temperature	$T_{opr}$		-40~+90	$^{\circ}\text{C}$
Storage Temperature	$T_{stg}$		-55~+150	$^{\circ}\text{C}$

## ■ ELECTRICAL CHARACTERISTICS

(General conditions:  $T_a=+25^{\circ}\text{C}$ ,  $Z_s=Z_l=50\Omega$ ,  $V_{DD}=2.7\text{V}$ ,  $V_{CTL(L)}=0\text{V}$ ,  $V_{CTL(H)}=1.8\text{V}$ , with application circuit)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	$V_{DD}$		1.5	2.7	4.5	V
Operating Current	$I_{DD}$		-	30	60	$\mu\text{A}$
Control Voltage (LOW)	$V_{CTL(L)}$		0	0	0.45	V
Control Voltage (HIGH)	$V_{CTL(H)}$		1.35	1.8	4.5	V
Control Current	$I_{CTL}$		-	5	10	$\mu\text{A}$

## ■ ELECTRICAL CHARACTERISTICS

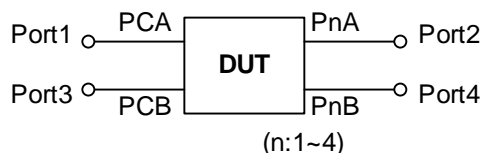
(General conditions:  $T_a=+25^{\circ}\text{C}$ ,  $Z_s=Z_l=50\Omega$ ,  $V_{DD}=2.7\text{V}$ ,  $V_{CTL(L)}=0\text{V}$ ,  $V_{CTL(H)}=1.8\text{V}$ , with application circuit)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion Loss 1	LOSS1	$f=1.0\text{GHz}$ , $P_{IN}=0\text{dBm}$	-	0.40	0.60	dB
Insertion Loss 2	LOSS2	$f=2.0\text{GHz}$ , $P_{IN}=0\text{dBm}$	-	0.45	0.65	dB
Insertion Loss 3	LOSS3	$f=2.7\text{GHz}$ , $P_{IN}=0\text{dBm}$	-	0.80	1.0	dB
Balanced mode isolation 1 (Note1)	B-ISL1	$f=1.0\text{GHz}$ , $P_{IN}=0\text{dBm}$ PC-P1, P2, P3, P4	40	43	-	dB
Balanced mode Isolation 2 (Note1)	B-ISL2	$f=2.0\text{GHz}$ , $P_{IN}=0\text{dBm}$ PC-P1, P2, P3, P4	35	38	-	dB
Balanced mode isolation 3 (Note1)	B-ISL3	$f=2.7\text{GHz}$ , $P_{IN}=0\text{dBm}$ PC-P1, P2, P3, P4	32	35	-	dB
Isolation 1	ISL1	PCA-P1A, P2A, P3A, P4A PCB-P1B, P2B, P3B, P4B $f=1.0\text{GHz}$ , $P_{IN}=0\text{dBm}$	26	28	-	dB
Isolation 2	ISL2	PCA-P1A, P2A, P3A, P4A PCB-P1B, P2B, P3B, P4B $f=2.0\text{GHz}$ , $P_{IN}=0\text{dBm}$	23	26	-	dB
Isolation 3	ISL3	PCA-P1A, P2A, P3A, P4A PCB-P1B, P2B, P3B, P4B $f=2.7\text{GHz}$ , $P_{IN}=0\text{dBm}$	18	20	-	dB
Isolation 4	ISL4	PCA-PCB port $f=2.0\text{GHz}$ , $P_{IN}=0\text{dBm}$	17	19	-	dB
Input power at 0.2dB Compression Point	$P_{-0.2\text{dB}}$	$f=2.0\text{GHz}$	20	23	-	dBm
VSWR	VSWR	$f=2.0\text{GHz}$ , On state port	-	1.2	1.4	-
Switching time	$T_{\text{SW}}$	50% $V_{\text{CTL}}$ to 10/90% RF	-	2	5	$\mu\text{s}$

Note1:

The calculation of "Balanced Mode Isolation" uses the following formula.

$$B - \text{ISL} = \frac{1}{2} (S_{21} - S_{23} - S_{41} + S_{43})$$

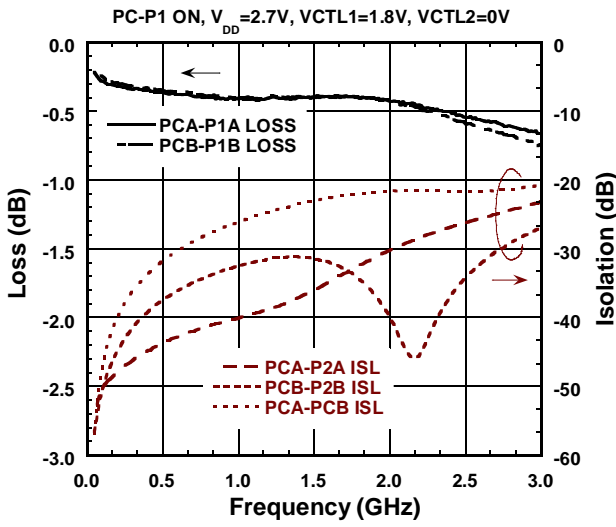


## ■ TERMINAL INFORMATION

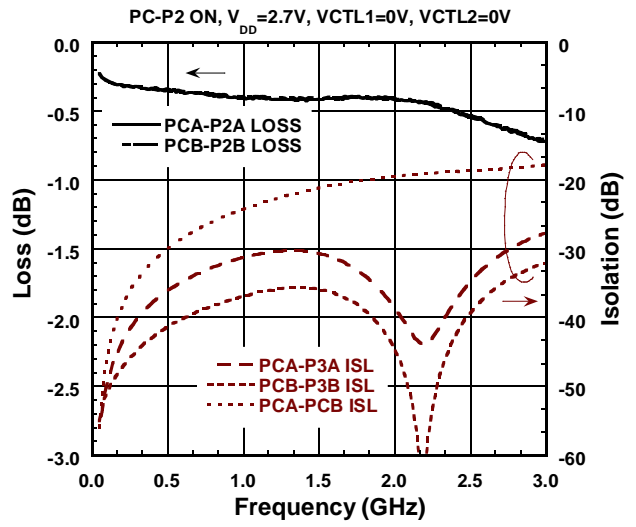
No.	SYMBOL	DESCRIPTION
1, 5, 10, 14	GND	Ground terminal. Please connect to the PCB ground plane.
2	VDD	Positive voltage supply terminal (+1.5~+4.5V). Please place a bypass capacitor between this terminal and GND for best RF performance.
3	VCTL2	Control signal input terminal. This terminal is to be set to High-Level (+1.35V~4.5V) or Low-Level (0~+0.45V).
4	VCTL1	Control signal input terminal. This terminal is to be set to High-Level (+1.35V~4.5V) or Low-Level (0~+0.45V).
6	P4A	The 4th RF port of the 1st switch. This port is connected with PCA port. PCB port is connected with P4B port at the same time. An external capacitor is required to block DC voltage.
7	P4B	The 4th RF port of the 2nd switch. This port is connected with PCB port. PCA port is connected with P4A port at the same time. An external capacitor is required to block DC voltage.
8	P3A	The 3rd RF port of the 1st switch. This port is connected with PCA port. PCB port is connected with P3B port at the same time. An external capacitor is required to block DC voltage.
9	P3B	The 3rd RF port of the 2nd switch. This port is connected with PCB port. PCA port is connected with P3A port at the same time. An external capacitor is required to block DC voltage.
11	P2B	The 2nd RF port of the 2nd switch. This port is connected with PCB port. PCA port is connected with P2A port at the same time. An external capacitor is required to block DC voltage.
12	P2A	The 2nd RF port of the 1st switch. This port is connected with PCA port. PCB port is connected with P2B port at the same time. An external capacitor is required to block DC voltage.
13	P1A	The 1st RF port of the 1st switch. This port is connected with PCA port. PCB port is connected with P1B port at the same time. An external capacitor is required to block DC voltage.
15	P1B	The 1st RF port of the 2nd switch. This port is connected with PCB port. PCA port is connected with P1A port at the same time. An external capacitor is required to block DC voltage.
16	GND(NC)	Not connected terminal. This terminal is not connected with internal circuit. Please connect it to the PCB ground plane.
17	PCB	Common RF port of the 2nd switch. This port is connected to one RF port of the 2nd switch (P1B~P4B). An external capacitor is required to block DC voltage.
18	PCA	Common RF port of the 1st switch. This port is connected to one RF port of the 1st switch (P1A~P4A). An external capacitor is required to block DC voltage.

## ■ ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)

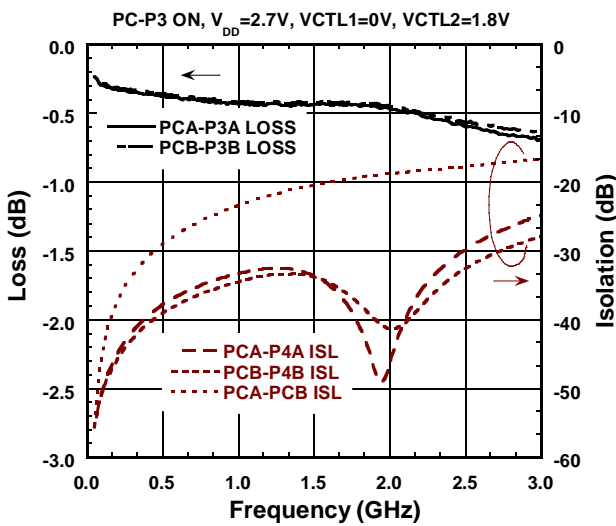
### Insertion Loss vs. Frequency



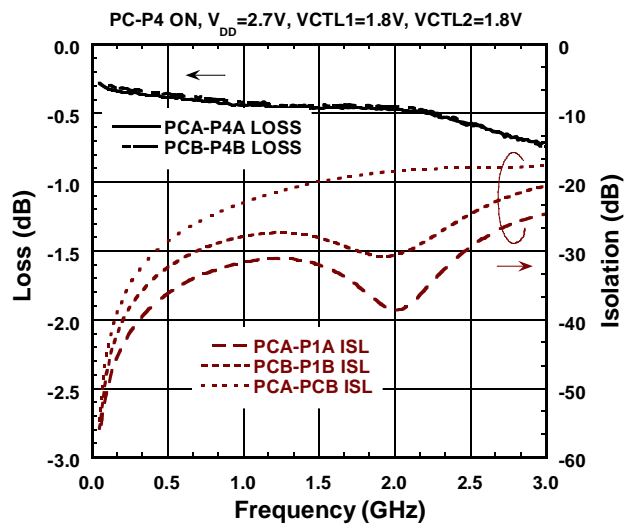
### Insertion Loss vs. Frequency



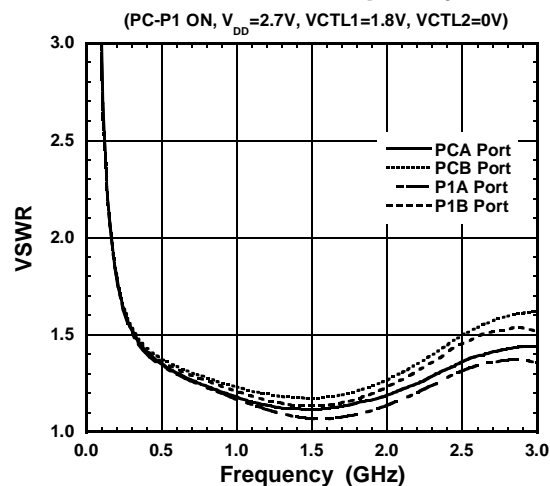
### Insertion Loss vs. Frequency



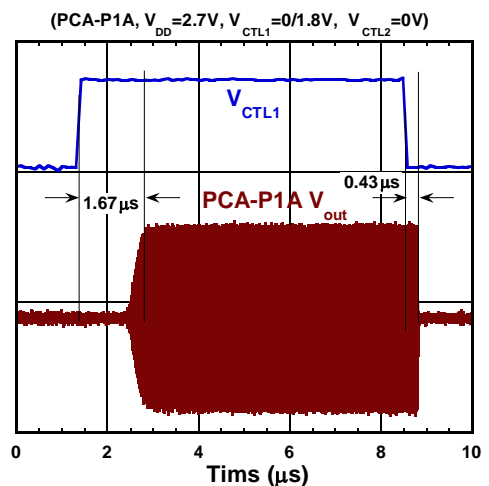
### Insertion Loss vs. Frequency



### VSWR vs. Frequency

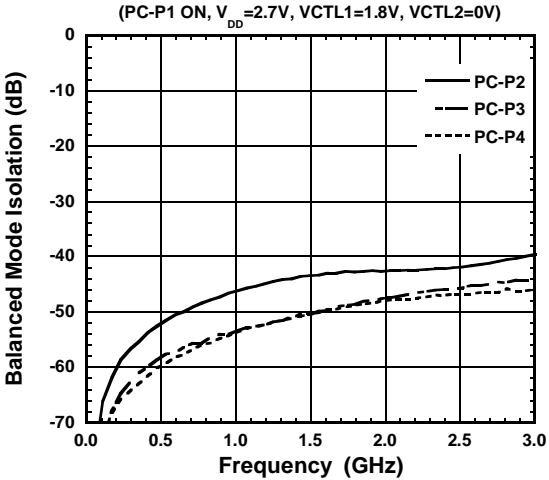


### Switching Time

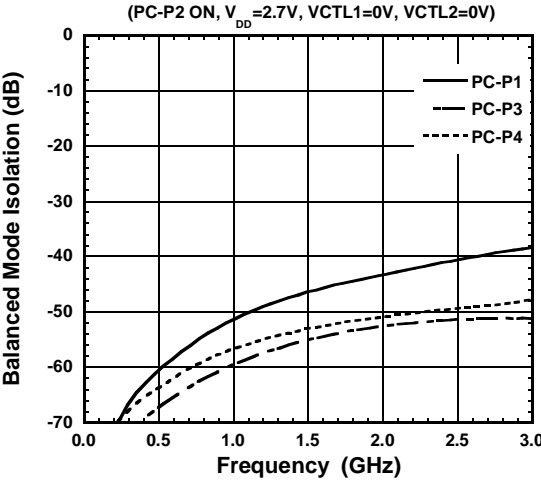


■ ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)

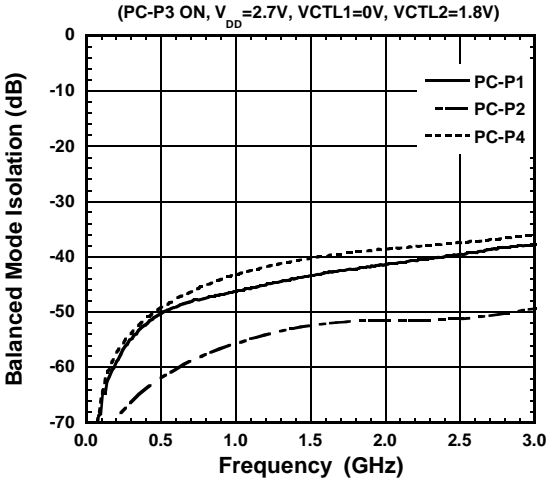
Balanced Mode Isolation vs. Frequency



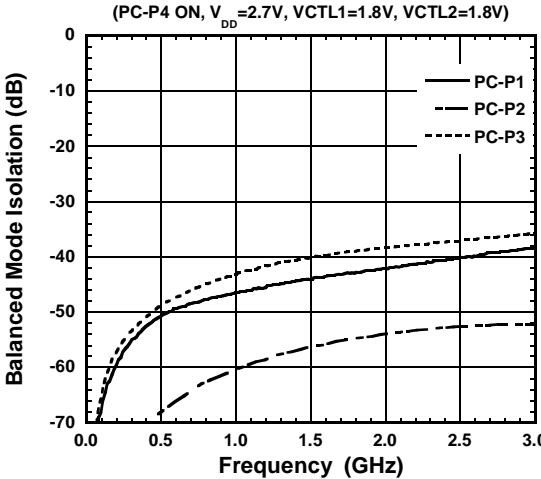
Balanced Mode Isolation vs. Frequency



Balanced Mode Isolation vs. Frequency



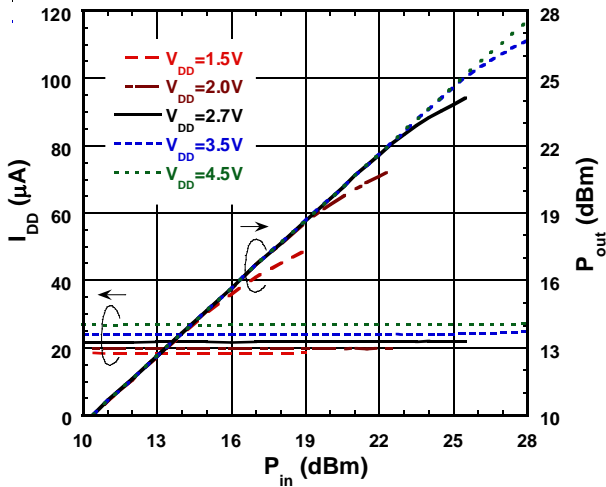
Balanced Mode Isolation vs. Frequency



## ■ ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)

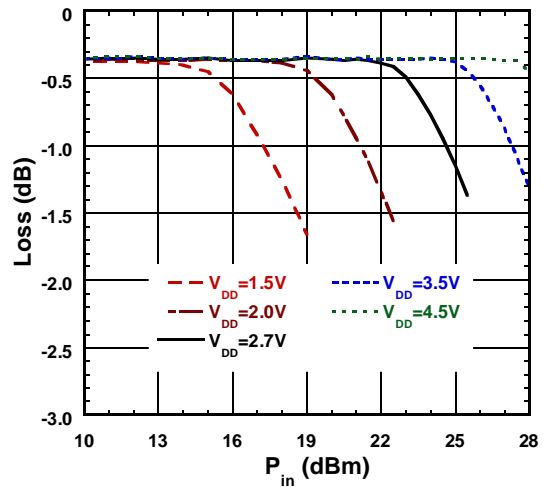
### $P_{out}$ & $I_{DD}$ vs. $P_{in}$ at 1.0GHz

(PCB-P1B ON, VCTL1=1.8V, VCTL2=0V)



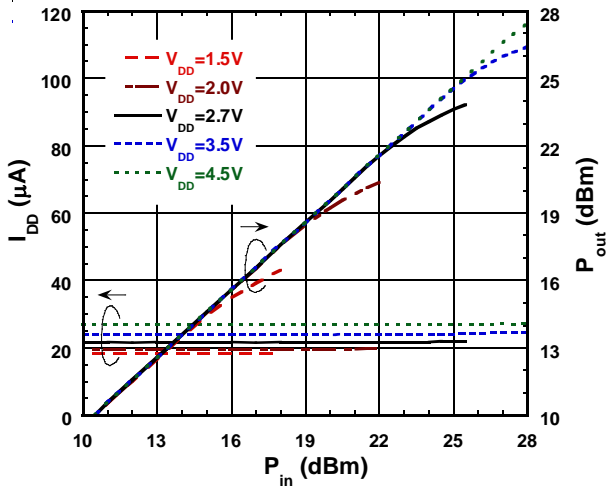
### Loss vs. $P_{in}$ at 1.0GHz

(PCB-P1B ON, VCTL1=1.8V, VCTL2=0V)



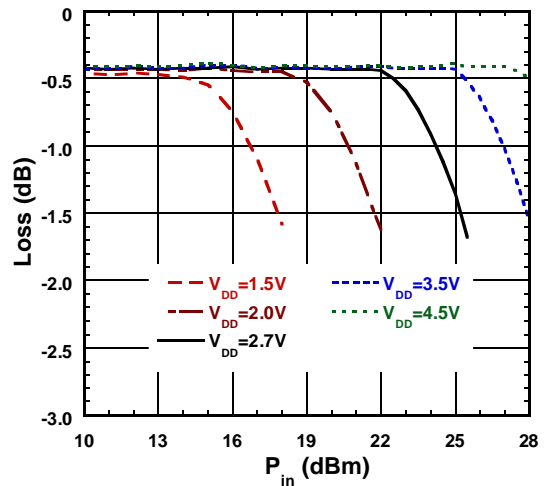
### $P_{out}$ & $I_{DD}$ vs. $P_{in}$ at 2.0GHz

(PCB-P1B ON, VCTL1=1.8V, VCTL2=0V)



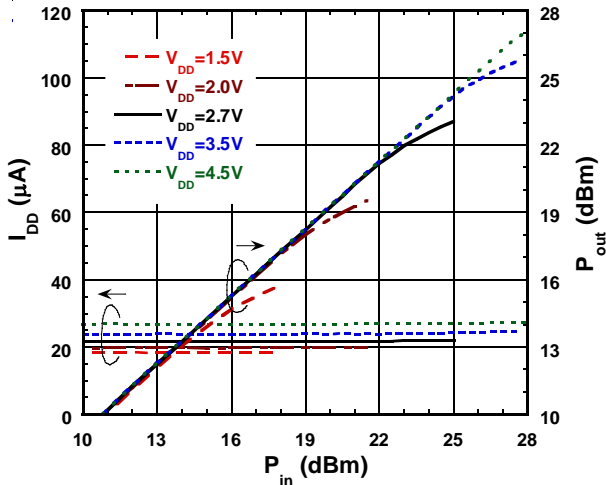
### Loss vs. $P_{in}$ at 2.0GHz

(PCB-P1B ON, VCTL1=1.8V, VCTL2=0V)



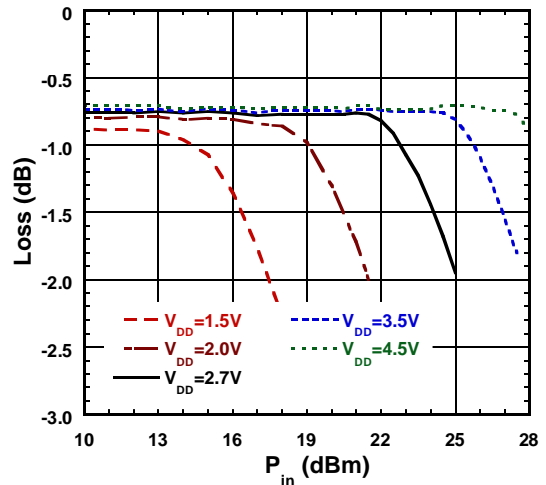
### $P_{out}$ & $I_{DD}$ vs. $P_{in}$ at 2.7GHz

(PCB-P1B ON, VCTL1=1.8V, VCTL2=0V)



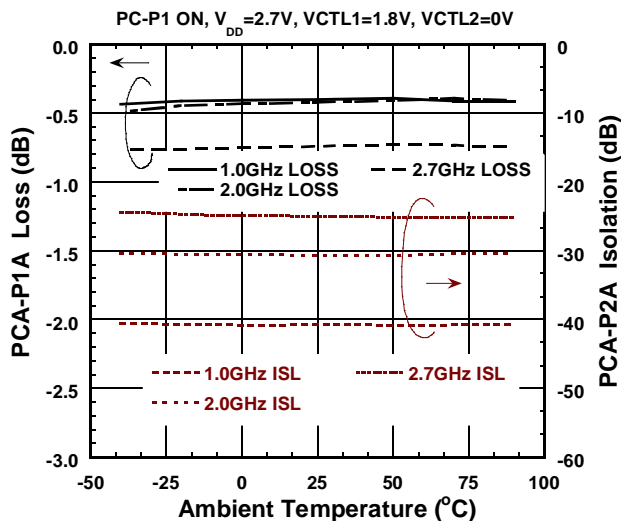
### Loss vs. $P_{in}$ at 2.7GHz

(PCB-P1B ON, VCTL1=1.8V, VCTL2=0V)

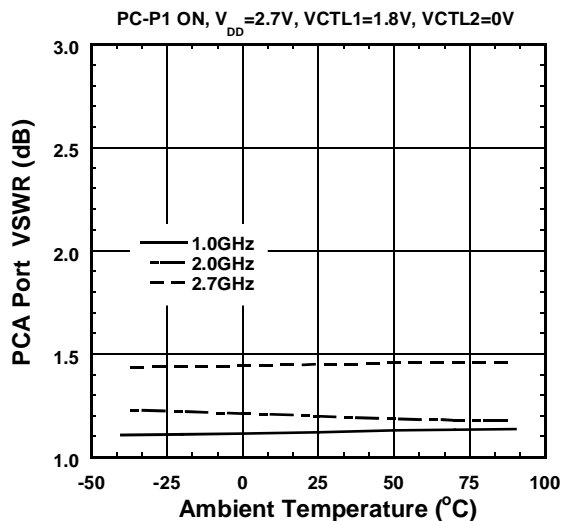


## ■ ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)

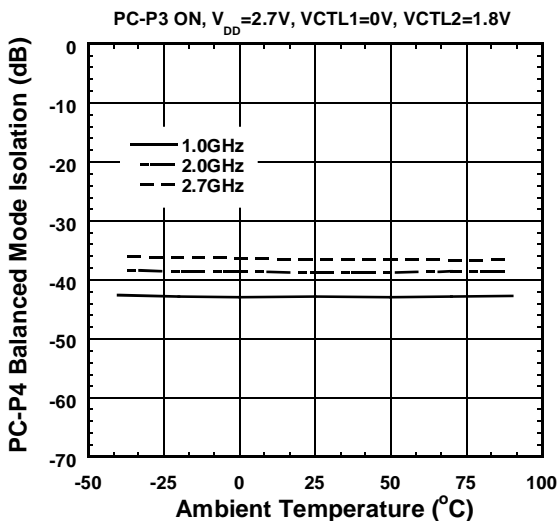
### Insertion Loss vs. Temperature



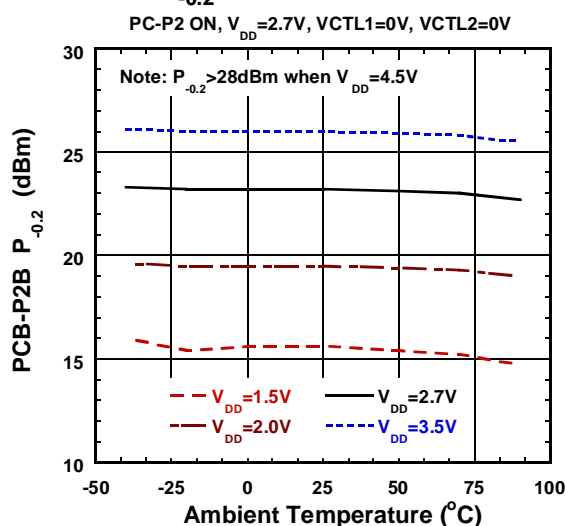
### VSWR vs. Temperature



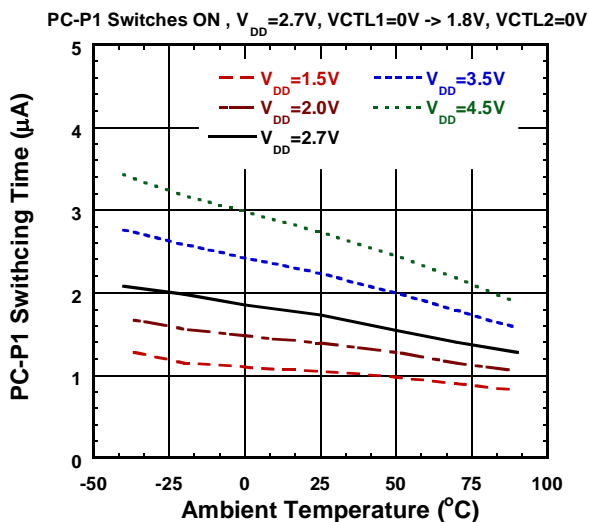
### Balanced Mode Isolation vs. Temperature



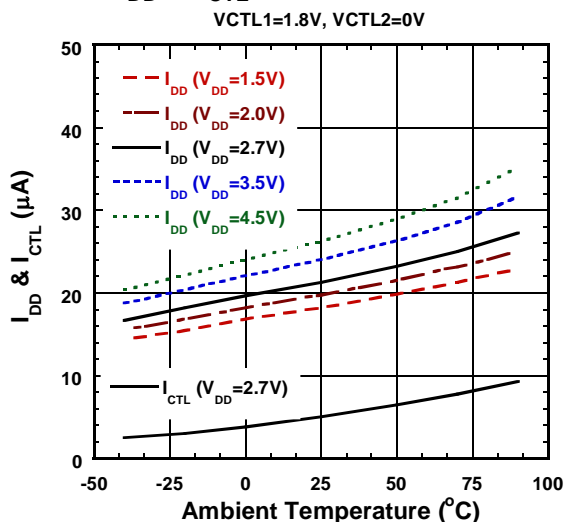
### $P_{-0.2}$ vs. Temperature



### Switching Time vs. Temperature



### $I_{DD}$ & $I_{CTL}$ vs. Temperature

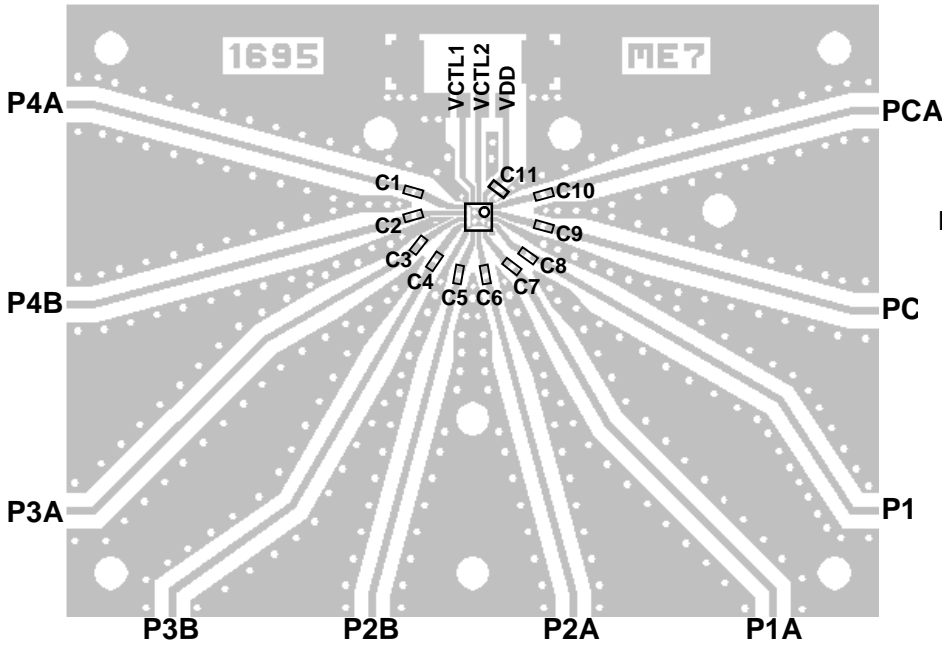






**■ TEST PCB LAYOUT**

(TOP VIEW)

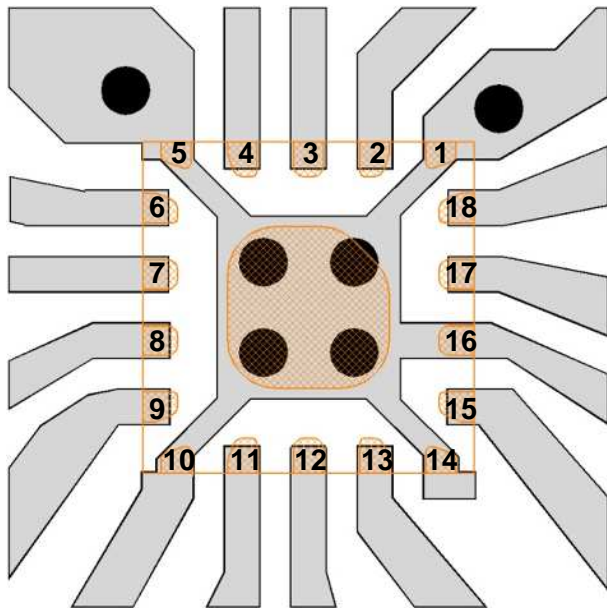


PCB: FR-4, t=0.2mm  
 Capacitor Size: 0603, 1005  
 Strip Line Width: 0.4mm  
 PCB Size: 53 x 40mm

Losses of PCB, capacitors and connectors

Paths	Frequency (GHz)	Loss (dB)
PCA-P1A, PCB-P1B, PCA-P3A, PCB-P3B	1.0	0.50
	2.0	0.84
	2.7	1.10
PCA-P2A, PCB-P2B, PCA-P4A, PCB-P4B	1.0	0.46
	2.0	0.77
	2.7	0.97

**<PCB LAYOUT GUIDELINE>**



- PCB Pattern
- Through-hole (radius: 0.15mm)
- Pin

**Note2:**

The ground plane and the through-holes under Tab, as shown in the picture, are not necessities. There is no problem in deleting them in the practical PCB design, though in such case beware that the GND terminals (pin 10 and 14 as for this particular design shown in the picture) still need through-holes being located in their vicinities.

**PRECAUTIONS**

- [1] The DC current at RF ports must be equal to zero, which can be achieved with DC blocking capacitors (C1~C10).  
 (However, in case there is no possibility that DC current flows, the DC blocking capacitors are unnecessary, i.e. the RF signals are fed by SAW filters that block DC current by nature, etc.)
- [2] To reduce stripline influence on RF characteristics, please locate the bypass capacitor (C11) close to VDD terminal.
- [3] For good isolation, the GND terminals must be connected to the PCB ground plane of substrate, and the through-holes connecting the backside ground plane should be placed near by the pin connection.





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  - 8-1. **Quality Warranty Period**

In the case of a product purchased through an authorized distributor or directly from us, the warranty period for this product shall be one (1) year after delivery to your company. For defective products that occurred during this period, we will take the quality warranty measures described in section 8-2. However, if there is an agreement on the warranty period in the basic transaction agreement, quality assurance agreement, delivery specifications, etc., it shall be followed.
  - 8-2. **Quality Warranty Remedies**

When it has been proved defective due to manufacturing factors as a result of defect analysis by us, we will either deliver a substitute for the defective product or refund the purchase price of the defective product.

Note that such delivery or refund is sole and exclusive remedies to your company for the defective product.
  - 8-3. **Remedies after Quality Warranty Period**

With respect to any defect of this product found after the quality warranty period, the defect will be analyzed by us. On the basis of the defect analysis results, the scope and amounts of damage shall be determined by mutual agreement of both parties. Then we will deal with upper limit in Section 8-2. This provision is not intended to limit any legal rights of your company.
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