

HIGH ISOLATION X-SPDT (DP4T) SWITCH GaAs MMIC

■ GENERAL DESCRIPTION

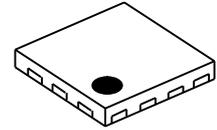
The NJG1690MD7 is a GaAs X (cross)-SPDT(DP4T) switch MMIC for switching of balanced (differential) dual band filters. It features low insertion loss and very high isolation for balanced signal input which makes it much suited for balanced filter switching.

The ESD protection circuit are integrated in the IC to achieve high ESD tolerance.

The ultra-small and ultra-thin EQFN14-D7 package is adopted.

*) X-SPDT is a paired SPDT switch controlled synchronously. The X-SPDT includes two SPDT switches whose RF lines have a crossing inside the chip.

■ PACKAGE OUTLINE



NJG1690MD7

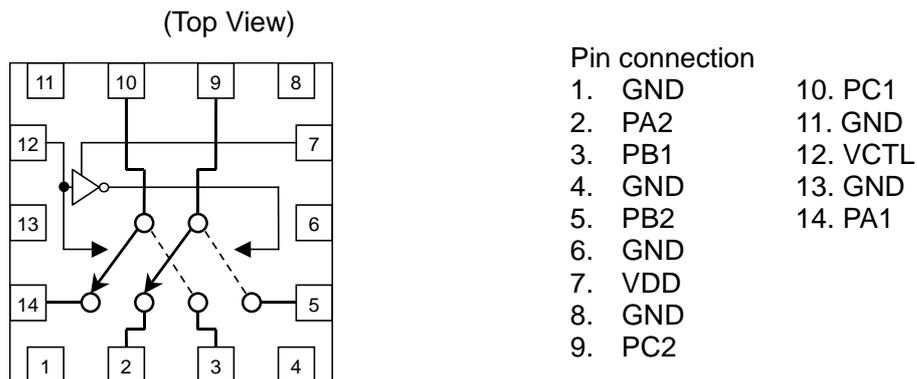
■ APPLICATIONS

Balanced filter switching application
 TDD/FDD LTE, UMTS, CDMA and GSM Multi-mode or Multi-band applications
 Mobile phone, Tablet PC, Data card, Router and others mobile device applications

■ FEATURES

- Low operation voltage $V_{DD} = 2.7V$
- Low control voltage $V_{CTL(H)} = 1.8V$ typ.
- High isolation
 - 37dB typ. @f=2.7GHz, $P_{IN}=0dBm$ (with balanced mode operation)
 - 29dB typ. @f=1.0GHz, $P_{IN}=0dBm$
 - 24dB typ. @f=2.0GHz, $P_{IN}=0dBm$
 - 21dB typ. @f=2.7GHz, $P_{IN}=0dBm$
- Low insertion loss
 - 0.3dB typ. @f=1.0GHz, $P_{IN}=0dBm$
 - 0.4dB typ. @f=2.0GHz, $P_{IN}=0dBm$
 - 0.45dB typ. @f=2.7GHz, $P_{IN}=0dBm$
- Small and thin package EQFN14-D7 (Package size: 1.6x1.6x0.397mm typ.)
- RoHS compliant and Halogen Free
- MSL: 1

■ PIN CONFIGURATION



■ TRUTH TABLE

“H”= $V_{CTL(H)}$, “L”= $V_{CTL(L)}$

ON PATH	VCTL
PC1-PA1, PC2-PA2	H
PC1-PB1, PC2-PB2	L

NOTE: Please note that any information on this catalog will be subject to change.

■ ABSOLUTE MAXIMUM RATINGS

($T_a=+25^{\circ}\text{C}$, $Z_s=Z_l=50\Omega$)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNITS
RF input power	P_{IN}	$V_{DD}=2.7\text{V}$, $V_{CTL}=0\text{V}/1.8\text{V}$	28	dBm
Supply voltage	V_{DD}		5.0	V
Control voltage	V_{CTL}		5.0	V
Power dissipation	P_D	Four-layer FR4 PCB with through-hole (74.2x74.2mm), $T_j=150^{\circ}\text{C}$	1300	mW
Operating temp.	T_{opr}		-40~+85	$^{\circ}\text{C}$
Storage temp.	T_{stg}		-55~+150	$^{\circ}\text{C}$

■ ELECTRICAL CHARACTERISTICS

(General conditions: $T_a=+25^{\circ}\text{C}$, $Z_s=Z_l=50\Omega$, $V_{DD}=2.7\text{V}$, $V_{CTL(L)}=0\text{V}$, $V_{CTL(H)}=1.8\text{V}$, with application circuit1)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply voltage	V_{DD}		1.5	2.7	4.5	V
Operating current	I_{DD}	$P_{IN}=0\text{dBm}$	-	16	30	μA
Control voltage (LOW)	$V_{CTL(L)}$		0	-	0.4	V
Control voltage (HIGH)	$V_{CTL(H)}$		1.3	1.8	4.5	V
Control current	I_{CTL}	$f=2\text{GHz}$, $P_{IN}=0\text{dBm}$	-	5	10	μA
Insertion loss 1	LOSS1	$f=1\text{GHz}$, $P_{IN}=0\text{dBm}$	-	0.30	0.45	dB
Insertion loss 2	LOSS2	$f=2\text{GHz}$, $P_{IN}=0\text{dBm}$	-	0.40	0.55	dB
Insertion loss 3	LOSS3	$f=2.7\text{GHz}$, $P_{IN}=0\text{dBm}$	-	0.45	0.65	dB
Balanced mode isolation *Note1	B-ISL	PC-PA (PC-PB ON) PC-PB (PC-PA ON) $f=2.7\text{GHz}$, $P_{IN}=0\text{dBm}$	33	37	-	dB
Isolation 1	ISL1	PC1-PA1, PC2-PA2 PC1-PB1, PC2-PB2 $f=1\text{GHz}$, $P_{IN}=0\text{dBm}$	27	29	-	dB
Isolation 2	ISL2	PC1-PA1, PC2-PA2 PC1-PB1, PC2-PB2 $f=2\text{GHz}$, $P_{IN}=0\text{dBm}$	21	24	-	dB
Isolation 3	ISL3	PC1-PA1, PC2-PA2 PC1-PB1, PC2-PB2 $f=2.7\text{GHz}$, $P_{IN}=0\text{dBm}$	18	21	-	dB
Isolation 4	ISL4	PC1-PC2 port $f=2\text{GHz}$, $P_{IN}=0\text{dBm}$	22	25	-	dB

Note1:

The balanced mode isolation is a unique specification for isolation defined under the condition where the X-SPDT switch is used in balanced mode operation as shown in application circuit2.

The NJG1690MD7 is designed so that the isolation in the balanced mode operation is much higher than the isolation in the single-ended mode operation.

■ ELECTRICAL CHARACTERISTICS

(General conditions: $T_a=+25^{\circ}\text{C}$, $Z_s=Z_l=50\Omega$, $V_{DD}=2.7\text{V}$, $V_{CTL(L)}=0\text{V}$, $V_{CTL(H)}=1.8\text{V}$, with application circuit1)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input power at 0.2dB compression point	$P_{-0.2\text{dB}}$	$f=2\text{GHz}$	20	24	-	dBm
VSWR	VSWR	$f=2\text{GHz}$, On port	-	1.2	1.4	
Switching time	T_{SW}	50% CTL to 10%/90% RF	-	1.5	5.0	μs

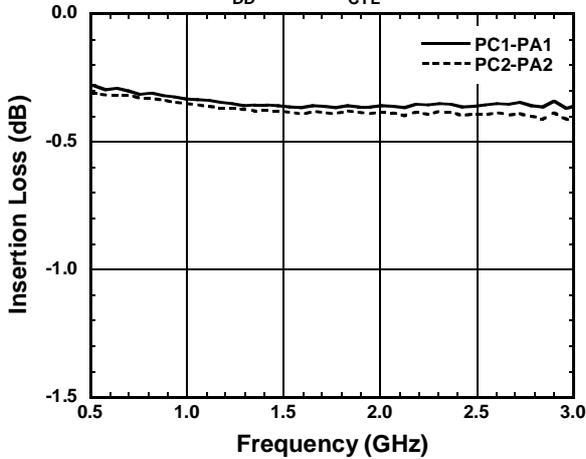
■ TERMINAL INFORMATION

No.	SYMBOL	DESCRIPTION
1	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for good RF performance.
2	PA2	This port is connected to PC2 terminal by applying High-level (1.3~4.5V) at VCTL terminal. An external capacitor is required to block DC voltage of internal circuit.
3	PB1	This port is connected to PC1 terminal by applying Low-level (0~0.4V) at VCTL terminal. An external capacitor is required to block DC voltage of internal circuit.
4	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for good RF performance.
5	PB2	This port is connected to PC2 terminal by applying Low-level (0~0.4V) at VCTL terminal. An external capacitor is required to block DC voltage of internal circuit.
6	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for good RF performance.
7	VDD	A supply voltage terminal (1.5~4.5V). Please place a bypass capacitor between this terminal and GND for avoiding RF noise from outside.
8	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for good RF performance.
9	PC2	Common RF port. This port is connected with either of PA2 or PB2. An external capacitor is required to block DC voltage of internal circuit.
10	PC1	Common RF port. This port is connected with either of PA1 or PB1. An external capacitor is required to block DC voltage of internal circuit.
11	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for good RF performance.
12	VCTL	Control signal input terminal. This terminal is set to high-level (1.3V~4.5V) or low-level (0~0.4V).
13	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for good RF performance.
14	PA1	This port is connected to PC1 terminal by applying High-level (1.3~4.5V) at VCTL terminal. An external capacitor is required to block DC voltage of internal circuit.

■ ELECTRICAL CHARACTERISTICS (With Application circuit1, Loss of external circuit are excluded)

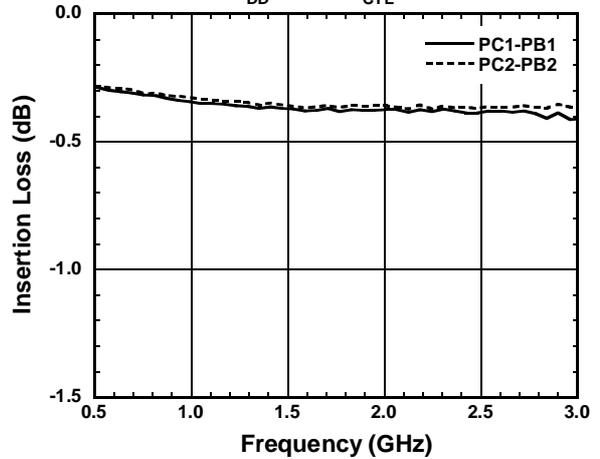
Insertion Loss vs. Frequency

($V_{DD}=2.7V, V_{CTL}=1.8V$)



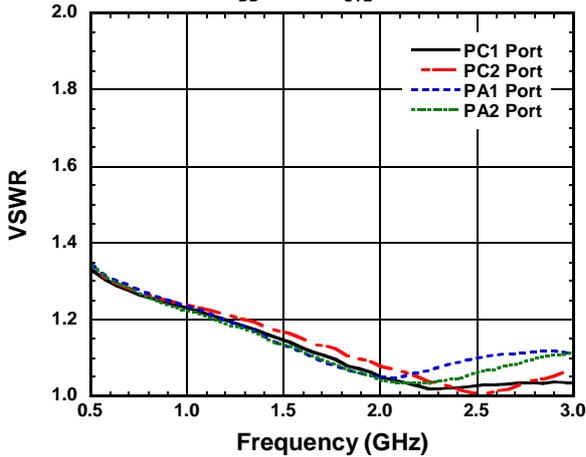
Insertion Loss vs. Frequency

($V_{DD}=2.7V, V_{CTL}=0V$)



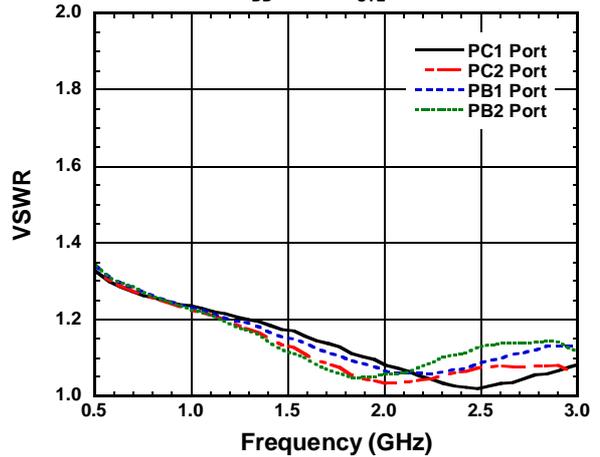
VSWR vs. Frequency

($V_{DD}=2.7V, V_{CTL}=1.8V$)



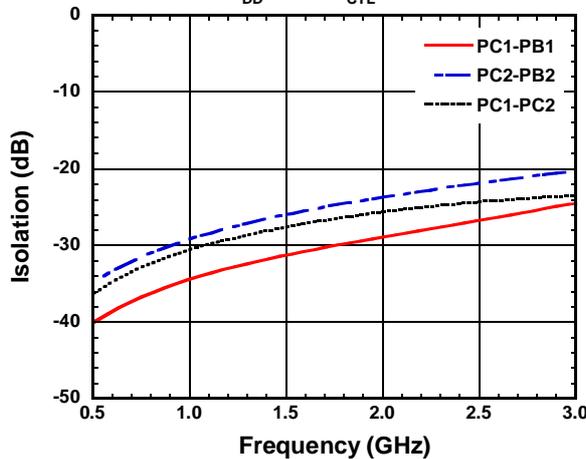
VSWR vs. Frequency

($V_{DD}=2.7V, V_{CTL}=0V$)



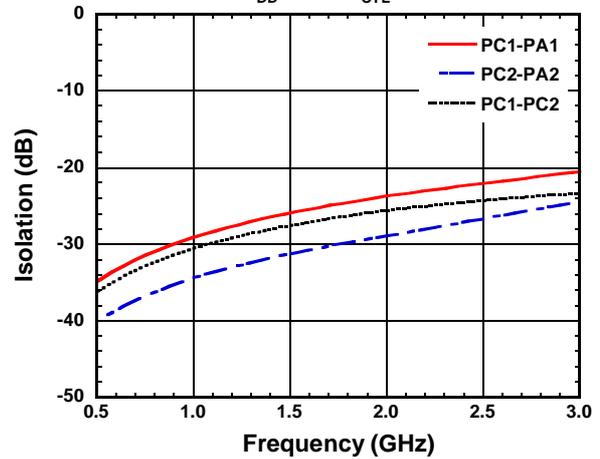
Isolation vs. Frequency

($V_{DD}=2.7V, V_{CTL}=1.8V$)



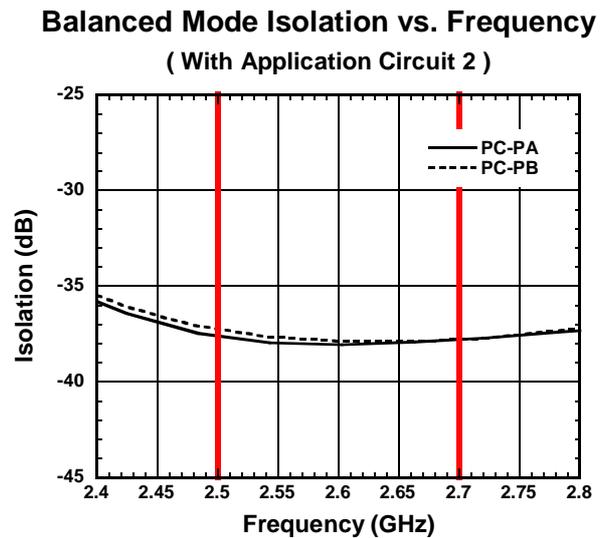
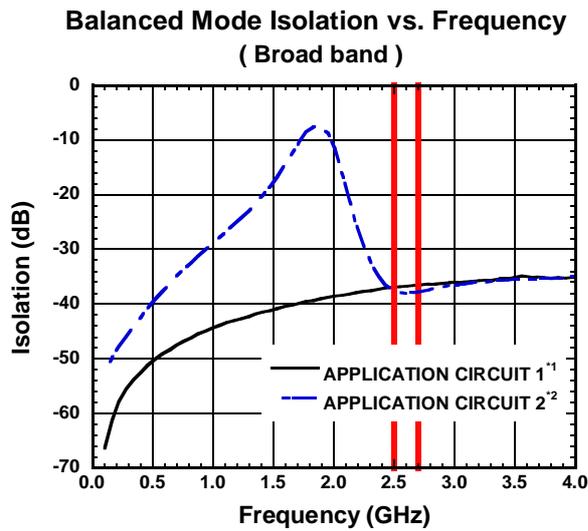
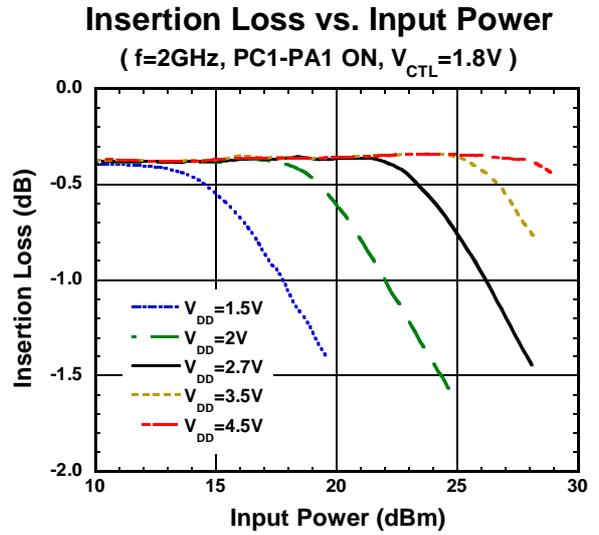
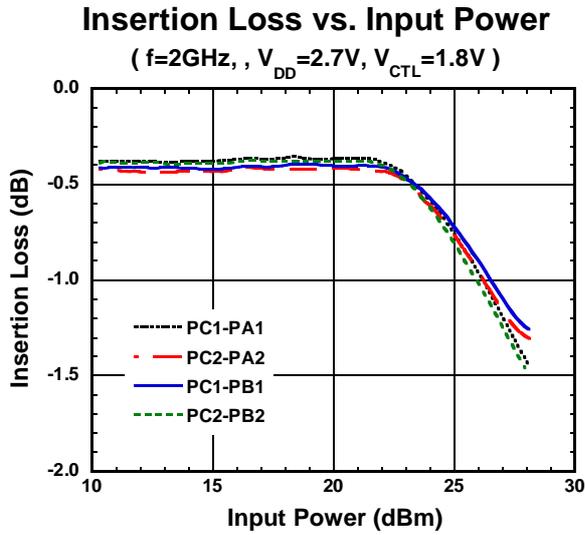
Isolation vs. Frequency

($V_{DD}=2.7V, V_{CTL}=0V$)



■ ELECTRICAL CHARACTERISTICS

(With Application circuit1 and 2, Loss of external circuit are excluded)

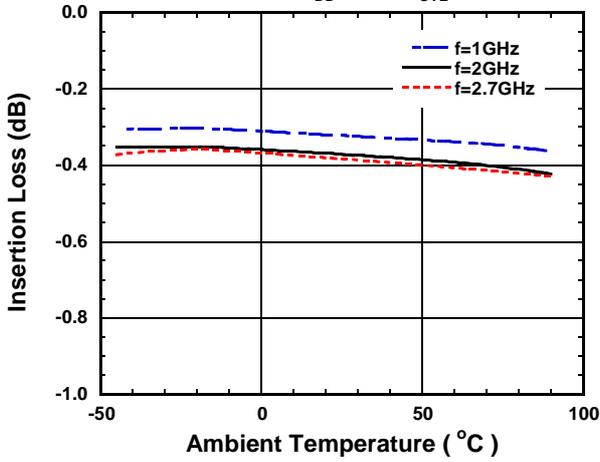


*1) The balanced mode isolation measured with the application circuit1.

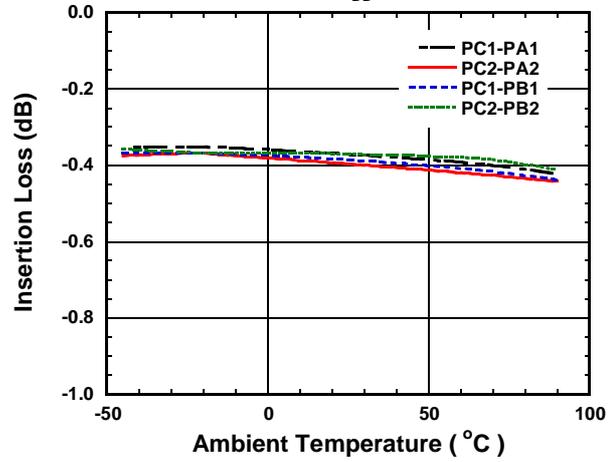
*2) The balanced mode isolation measured with the application circuit2 having single-ended interfaces and baluns.

■ ELECTRICAL CHARACTERISTICS (With Application circuit1, Loss of external circuit are excluded)

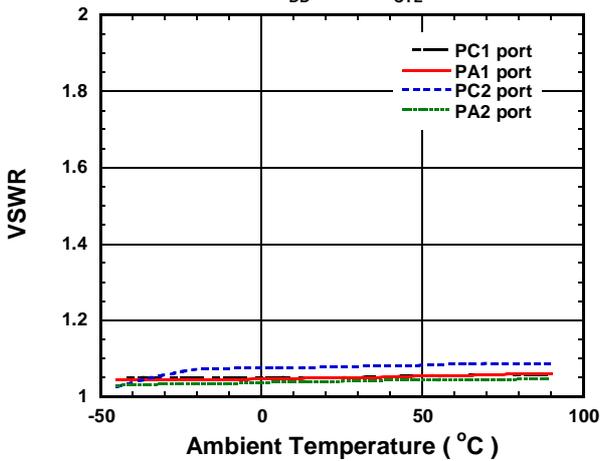
Insertion Loss vs. Ambient Temperature
(PC1-PA1 ON, $V_{DD}=2.7V$, $V_{CTL}=1.8V$)



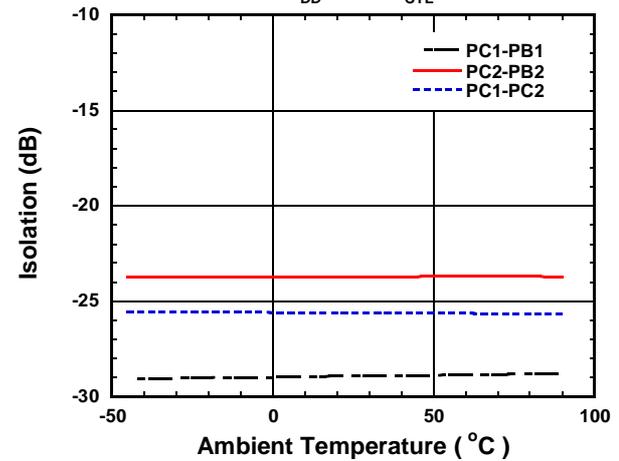
Insertion Loss vs. Ambient Temperature
(f=2GHz, $V_{DD}=2.7V$)



VSWR vs. Ambient Temperature
(f=2GHz, $V_{DD}=2.7V$, $V_{CTL}=1.8V$)



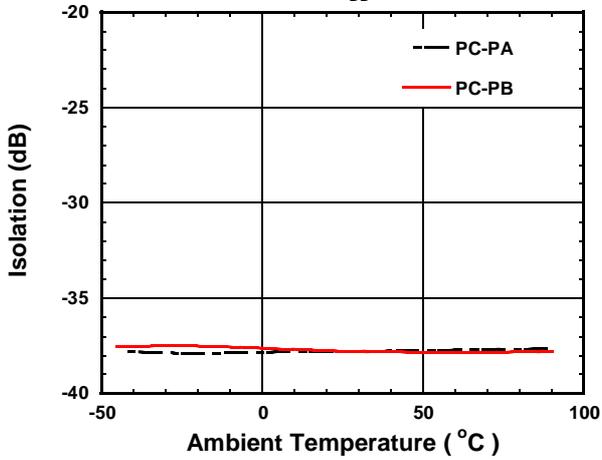
Isolation vs. Ambient Temperature
(f=2GHz, $V_{DD}=2.7V$, $V_{CTL}=1.8V$)



■ ELECTRICAL CHARACTERISTICS (With Application circuit1, Loss of external circuit are excluded)

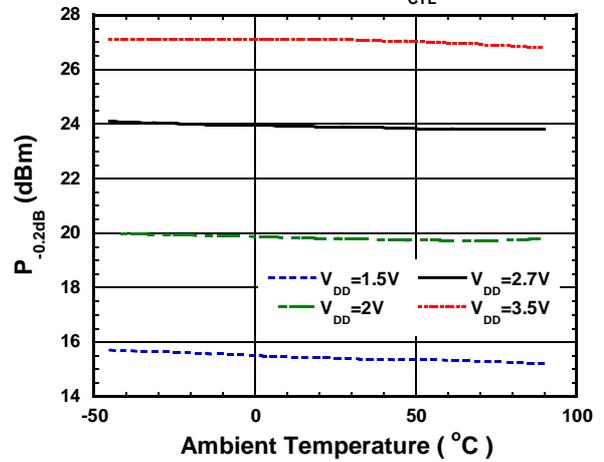
Balanced Mode Isolation vs. Temperature

($f=2.7\text{GHz}$, $V_{DD}=2.7\text{V}$)



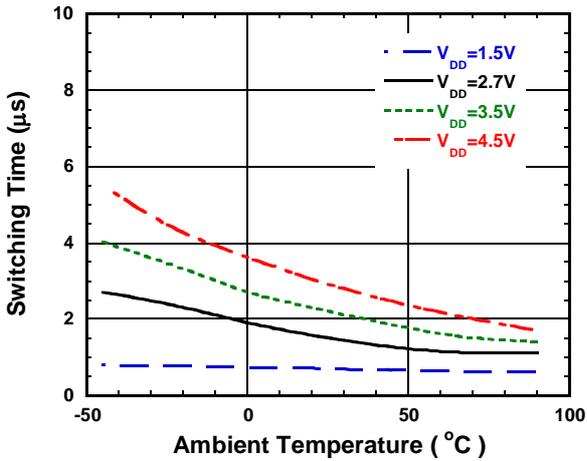
$P_{-0.2\text{dB}}$ vs. Ambient Temperature

($f=2\text{GHz}$, PC1-PA1 ON, $V_{CTL}=1.8\text{V}$)



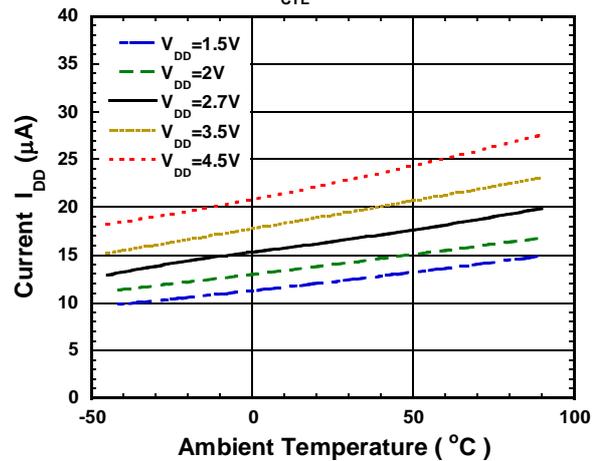
Switching Time vs. Ambient Temperature

($f=2\text{GHz}$, PC1-PA1 ON)

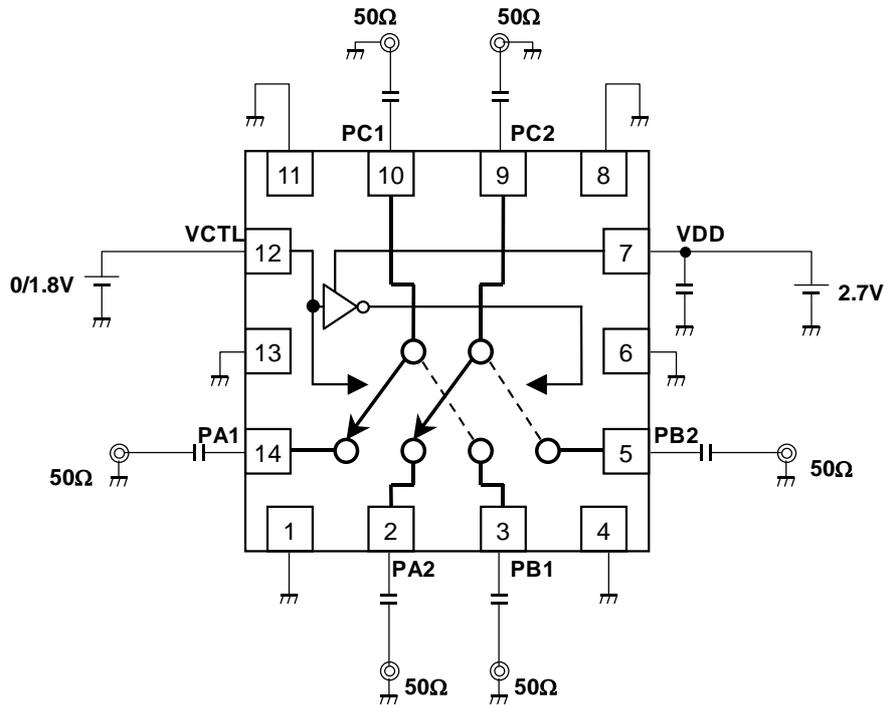


Current I_{DD} vs. Temperature

($V_{CTL}=1.8\text{V}$)

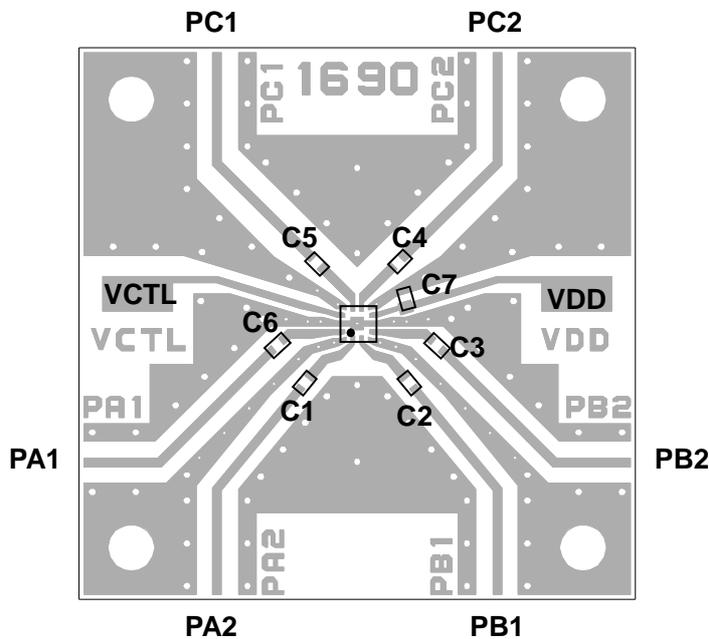


APPLICATION CIRCUIT 1 (Unbalanced mode)



PCB LAYOUT 1

(TOP VIEW)



PCB: FR-4, t=0.2mm
 Capacitor Size: 1005
 Strip Line Width: 0.4mm
 PCB Size: 26 x 26mm

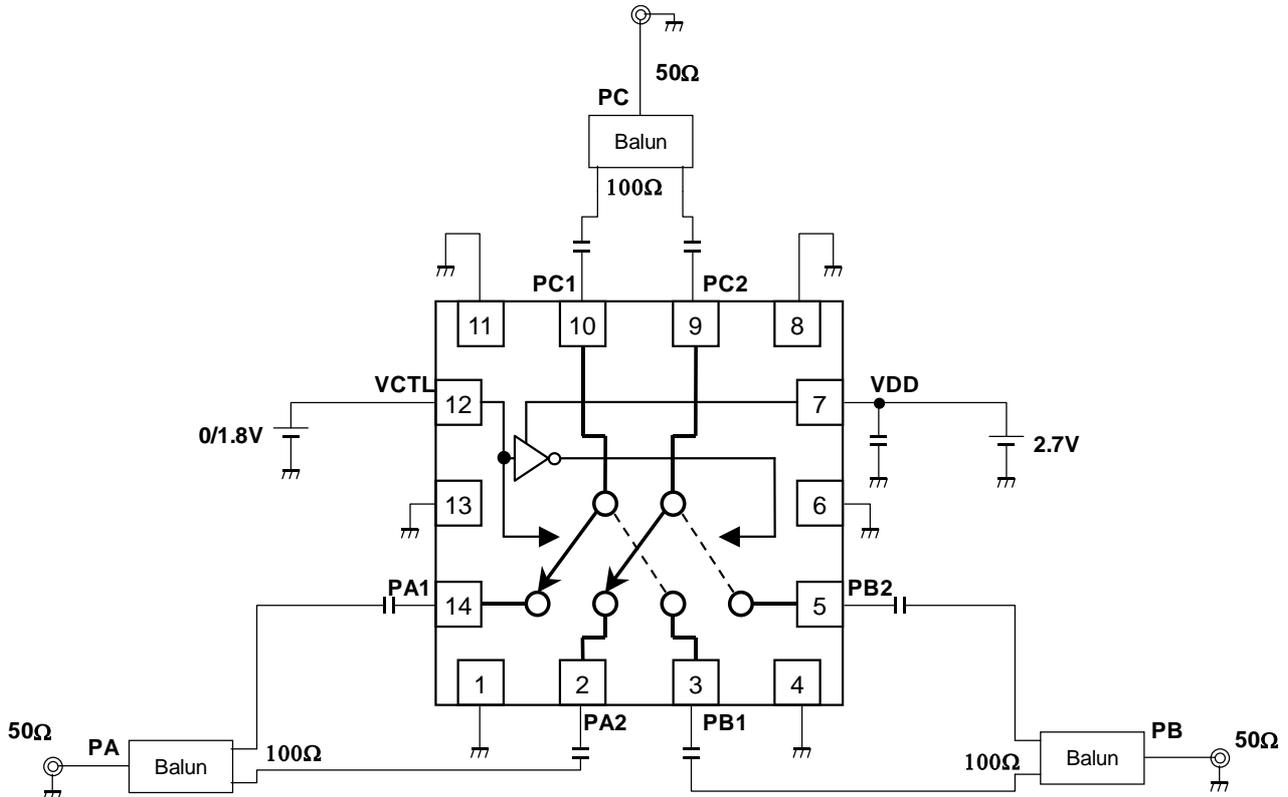
Losses of PCB, capacitors and connectors

Frequency (GHz)	Loss (dB)
1	0.35
2	0.54
2.7	0.68

PARTS LIST 1

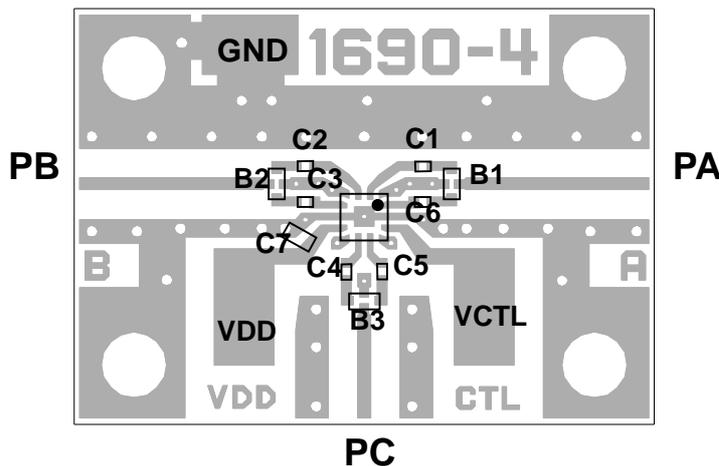
PART ID	Value	COMMENT
C1~C6	56pF	MURATA (GRM15)
C7	1000pF	MURATA (GRM15)

APPLICATION CIRCUIT 2 (BALANCED MODE)



PCB LAYOUT 2

(TOP VIEW)



PCB: FR-4, t=0.2mm
 Capacitor Size: 0603, 1005
 Strip Line Width: 0.4mm
 PCB Size: 19.4 x 14mm

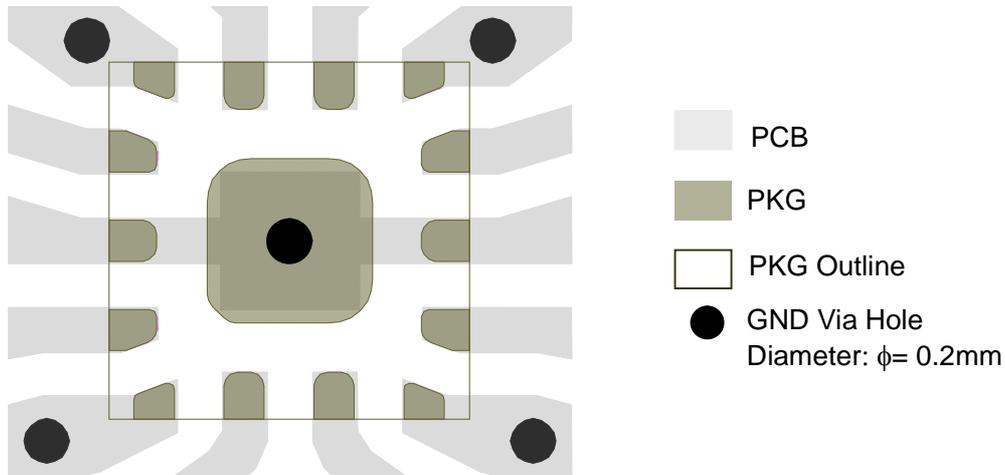
Losses of PCB, capacitors,
 connectors and baluns

Frequency (GHz)	Loss (dB)
2.7	0.93

PARTS LIST 2

PART ID	Value	COMMENT
C1~C6	56pF	MURATA (GRM03)
C7	1000pF	MURATA (GRM15)
B1~B3	2500MHz band	TDK-EPC (HHM1903A1)

PCB LAYOUT FOR EQFN14-D7



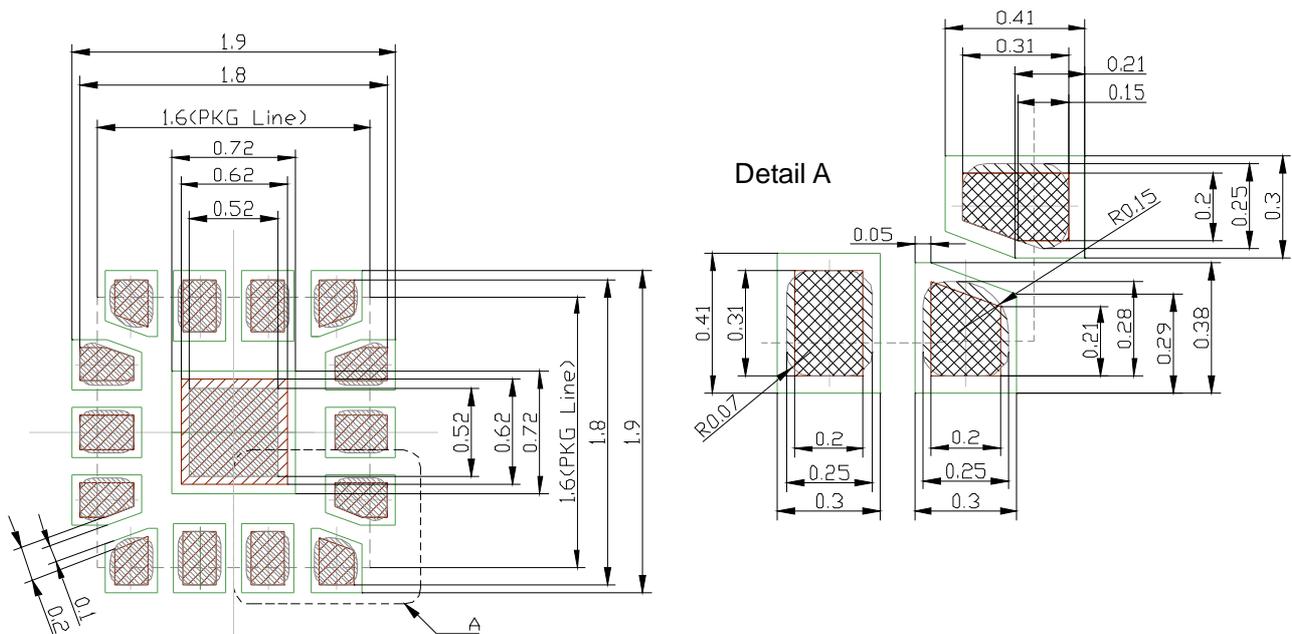
PRECAUTIONS

- [1] For good RF performance, all GND terminals must be connected to PCB ground plane of substrate, and via-holes for GND should be placed near the IC.
- [2] For good RF performance, through-holes for GND should be placed close to the GND pin 6 and pin 13. One of the ways to do this is to place a via-hole at the TAB pad under this IC.

RECOMMENDED FOOTPRINT PATTERN (EQFN14-D7 PACKAGE Reference)

- :Land
- :Mask (Open area) *Metal mask thickness : 100μm
- :Resist(Open area)

PKG: 1.6mm x 1.6mm
Pin pitch: 0.4mm



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 - 8-1. **Quality Warranty Period**

In the case of a product purchased through an authorized distributor or directly from us, the warranty period for this product shall be one (1) year after delivery to your company. For defective products that occurred during this period, we will take the quality warranty measures described in section 8-2. However, if there is an agreement on the warranty period in the basic transaction agreement, quality assurance agreement, delivery specifications, etc., it shall be followed.
 - 8-2. **Quality Warranty Remedies**

When it has been proved defective due to manufacturing factors as a result of defect analysis by us, we will either deliver a substitute for the defective product or refund the purchase price of the defective product.

Note that such delivery or refund is sole and exclusive remedies to your company for the defective product.
 - 8-3. **Remedies after Quality Warranty Period**

With respect to any defect of this product found after the quality warranty period, the defect will be analyzed by us. On the basis of the defect analysis results, the scope and amounts of damage shall be determined by mutual agreement of both parties. Then we will deal with upper limit in Section 8-2. This provision is not intended to limit any legal rights of your company.
9. Anti-radiation design is not implemented in the products described in this document.
10. The X-ray exposure can influence functions and characteristics of the products. Confirm the product functions and characteristics in the evaluation stage.
11. WLCSP products should be used in light shielded environments. The light exposure can influence functions and characteristics of the products under operation or storage.
12. Warning for handling Gallium and Arsenic (GaAs) products (Applying to GaAs MMIC, Photo Reflector). These products use Gallium (Ga) and Arsenic (As) which are specified as poisonous chemicals by law. For the prevention of a hazard, do not burn, destroy, or process chemically to make them as gas or power. When the product is disposed of, please follow the related regulation and do not mix this with general industrial waste or household waste.
13. Please contact our sales representatives should you have any questions or comments concerning the products or the technical information.



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