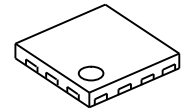


# HIGH ISOLATION SPDT SWITCH GaAs MMIC

## ■ GENERAL DESCRIPTION

The NJG1666MD7 is a GaAs SPDT switch designed for Set-top boxes, TV tuners, CATV tuners, and sub-microwave applications. The NJG1666MD7 features high isolation, low insertion loss and covering a broad frequency range up to 3GHz. The NJG1666MD7 operates single bit control switching by control voltage from 1.3V to 4.5V, and includes ESD protection circuits for good ESD tolerance. The NJG1666MD7 is available in a very small, lead-free, halogen-free, 1.6mm x 1.6mm x 0.397 mm, 14-pin EQFN14-D7 package.

## ■ PACKAGE OUTLINE



NJG1666MD7

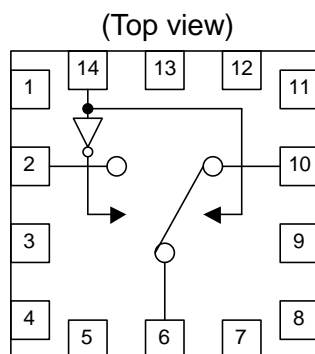
## ■ APPLICATIONS

Terrestrial and Satellite applications  
Set-top box, TV tuner, CATV tuner, Digital TV and Cable TV applications

## ■ FEATURES

- Low operating voltage  $V_{DD} = +2.0 \sim +4.5V$
  - Low control voltage  $V_{CTL(H)} = +1.3V \text{ min}$
  - Low current consumption 30 $\mu$ A typ.
  - High isolation
    - 70dB typ. @f=0.25GHz
    - 60dB typ. @f=1.0GHz
    - 60dB typ. @f=2.2GHz
  - Low insertion loss
    - 0.40dB typ. @f=0.25GHz
    - 0.45dB typ. @f=1.0GHz
    - 0.50dB typ. @f=2.2GHz
  - High ESD tolerance
  - Ultra- small and ultra-thin package
  - Lead and halogen-free
- On-chip ESD protection circuit  
EQFN14-D7 (package size: 1.6mm x 1.6mm x 0.397mm typ.)

## ■ PIN CONFIGURATION



### Pin Connection

- |            |             |
|------------|-------------|
| 1. NC(GND) | 8. NC(GND)  |
| 2. P2      | 9. GND      |
| 3. GND     | 10. P1      |
| 4. NC(GND) | 11. NC(GND) |
| 5. GND     | 12. VDD     |
| 6. PC      | 13. GND     |
| 7. GND     | 14. CTL     |

## ■ TRUTH TABLE

“H”= $V_{CTL(H)}$ , “L”= $V_{CTL(L)}$

CTL	PATH
H	PC-P1
L	PC-P2

**NOTE:** The information on this datasheet is subject to change without notice

## ■ ABSOLUTE MAXIMUM RATINGS

( $T_a=25^{\circ}\text{C}$ ,  $Z_s=Z_l=50\Omega$ )

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNITS
RF Input power	$P_{IN}$	$V_{DD}=3.0\text{V}$	28	dBm
Supply voltage	$V_{DD}$	VDD terminal	5.0	V
Control voltage	$V_{CTL}$	CTL terminal	5.0	V
Power dissipation	$P_D$	Four-layer FR4 PCB with through-hole (74.2mmx74.2mm), $T_j=150^{\circ}\text{C}$	1300	mW
Operating temp.	$T_{opr}$		-40~+85	$^{\circ}\text{C}$
Storage temp.	$T_{stg}$		-55~+150	$^{\circ}\text{C}$

## ■ ELECTRICAL CHARACTERISTICS 1 (DC)

(General conditions:  $V_{DD}=3.0\text{V}$ ,  $V_{CTL(L)}=0\text{V}$ ,  $V_{CTL(H)}=3.0\text{V}$ ,  $Z_s=Z_l=50\Omega$ ,  $T_a=+25^{\circ}\text{C}$ , with application circuit)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply voltage	$V_{DD}$		2.0	3.0	4.5	V
Operating current	$I_{DD}$		-	30	60	$\mu\text{A}$
Control voltage (L)	$V_{CTL(L)}$		0	-	0.4	V
Control voltage (H)	$V_{CTL(H)}$		1.3	3.0	4.5	V
Control current	$I_{CTL}$		-	15	30	$\mu\text{A}$

## ■ ELECTRICAL CHARACTERISTICS 2 (RF)

(General conditions:  $V_{DD}=3.0\text{V}$ ,  $V_{CTL(L)}=0\text{V}$ ,  $V_{CTL(H)}=3.0\text{V}$ ,  $Z_s=Z_l=50\Omega$ ,  $T_a=+25^{\circ}\text{C}$ , with application circuit)

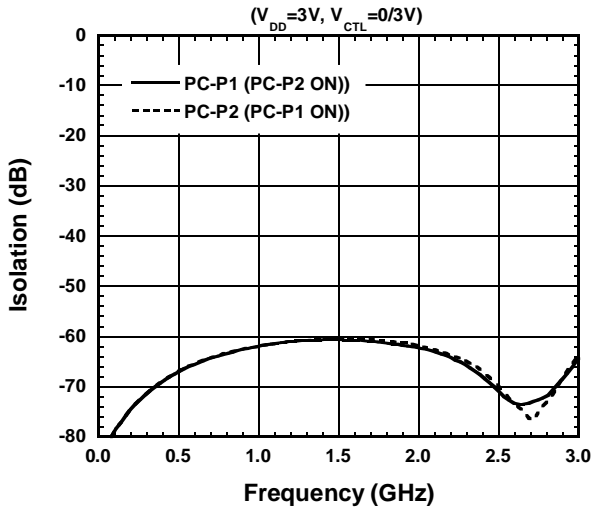
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion loss 1	LOSS1	$f=250\text{MHz}$ , $P_{IN}=0\text{dBm}$	-	0.40	0.60	dB
Insertion loss 2	LOSS2	$f=1000\text{MHz}$ , $P_{IN}=0\text{dBm}$	-	0.45	0.65	dB
Insertion loss 3	LOSS3	$f=2200\text{MHz}$ , $P_{IN}=0\text{dBm}$	-	0.50	0.70	dB
Isolation 1	ISL1	$f=250\text{MHz}$ , $P_{IN}=0\text{dBm}$	65	70	-	dB
Isolation 2	ISL2	$f=1000\text{MHz}$ , $P_{IN}=0\text{dBm}$	55	60	-	dB
Isolation 3	ISL3	$f=2200\text{MHz}$ , $P_{IN}=0\text{dBm}$	55	60	-	dB
Input power at 1dB compression point	$P_{-1\text{dB}}$	$f=2200\text{MHz}$	23	27	-	dBm
VSWR	VSWR	$f=2200\text{MHz}$ , ON state	-	1.3	1.5	
Switching time	$T_{sw}$	50% $V_{CTL}$ to 10%/90% RF	-	1	5	$\mu\text{s}$

## ■ TERMINAL INFORMATION

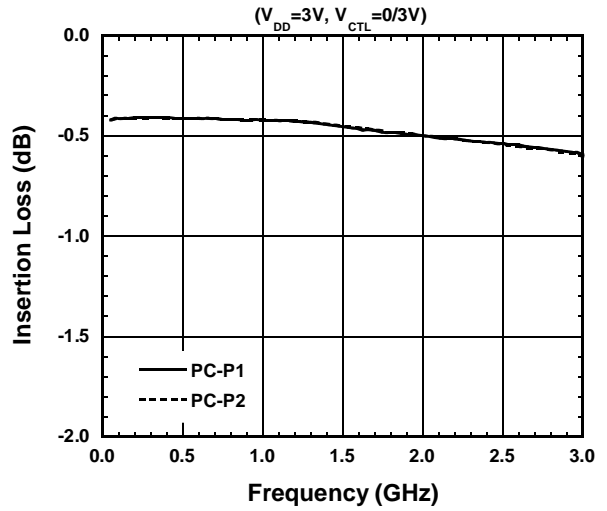
No.	SYMBOL	DESCRIPTION
2	P2	This port is connected to PC port by applying the control voltage 0~+0.4 V( $V_{CTL(L)}$ ) to 14th pin. An external capacitor is required to block the DC bias voltage of internal circuit.
6	PC	Common RF port. This PC port is connected to P1 or P2 by logical control voltage of 14th pin. In order to block DC bias voltage of internal circuit, an external capacitor is required.
10	P1	This port is connected to PC port by applying control voltage of +1.3~+4.5 V ( $V_{CTL(H)}$ ) to 14th pin. An external capacitor is required to block the DC bias voltage of internal circuit.
12	VDD	A supply voltage terminal (+2.0~+4.5 V). Place a bypass capacitor between this terminal and ground plane for avoiding RF noise from outside.
14	CTL	Control signal input terminal. This terminal is set to High-Level (+1.3~+4.5 V) or Low-Level (0~+0.4 V).
1,4,8,11	NC (GND)	No connected terminal. This terminal is not connected with internal circuit. Connect to the PCB ground plane.
3,5,7, 9,13	GND	Ground terminal. Connect this terminal with ground plane as close as possible for excellent RF performance.

## ■ ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)

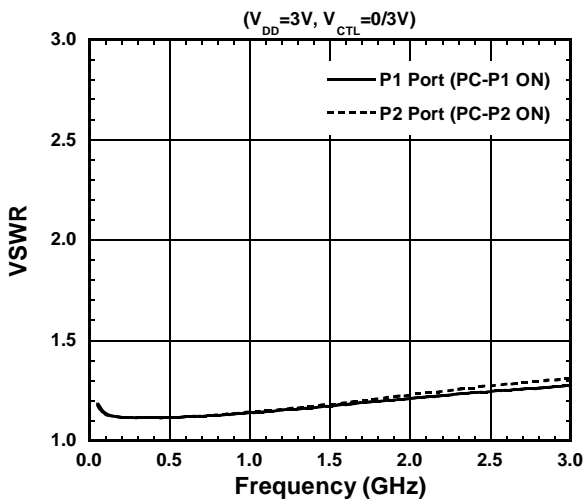
### Isolation vs. Frequency



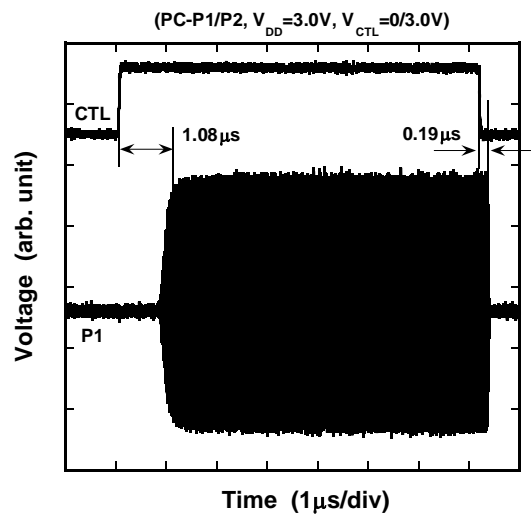
### Insertion Loss vs. Frequency



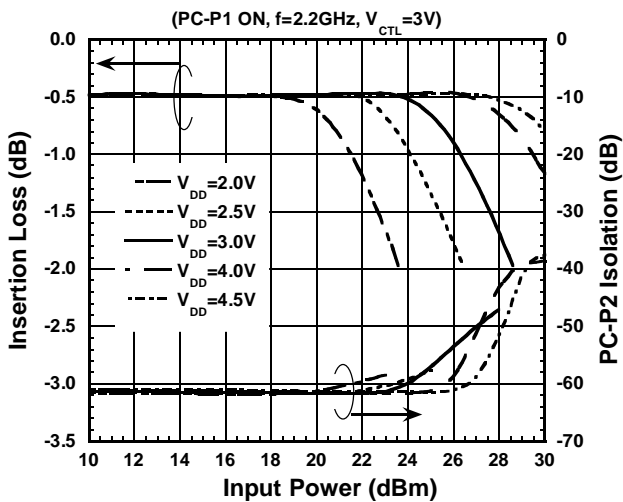
### VSWR vs. Frequency



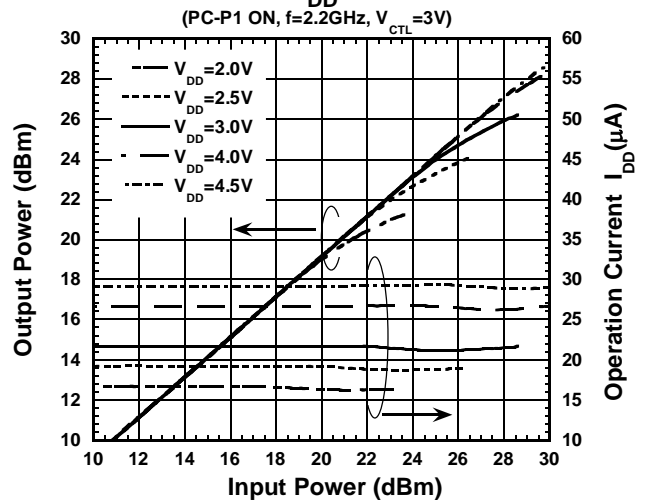
### Switching Time



### Loss, ISL vs. Input Power

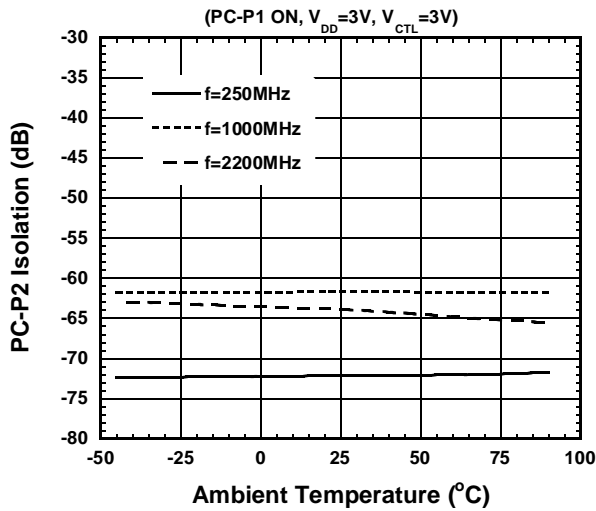


### Output Power, $I_{DD}$ vs. Input Power

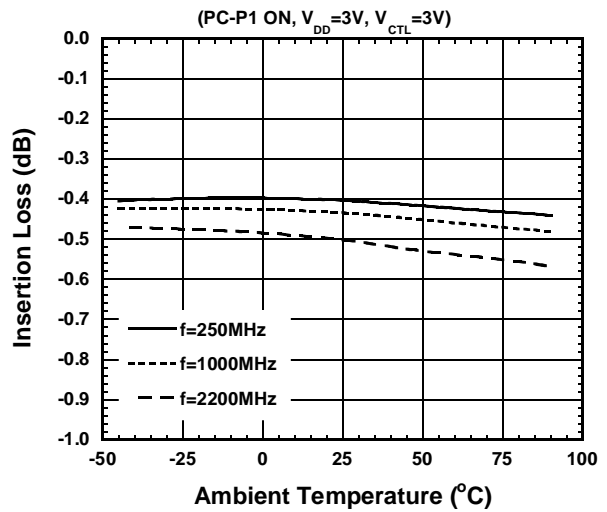


## ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)

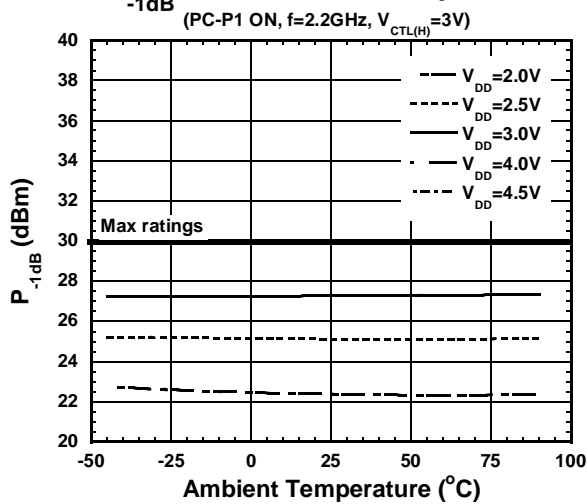
### ISL vs. Ambient Temperature



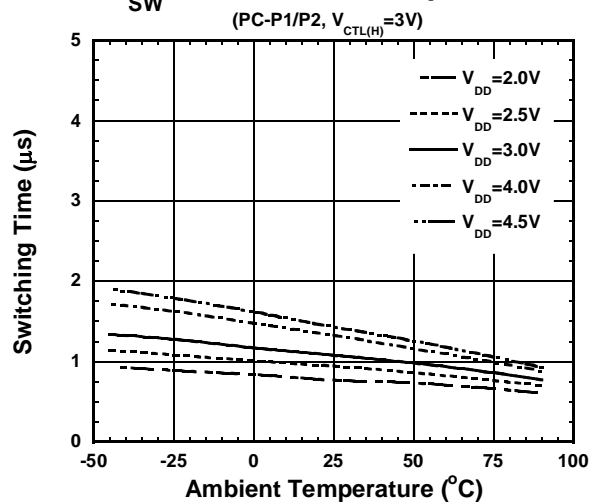
### Loss vs. Ambient Temperature



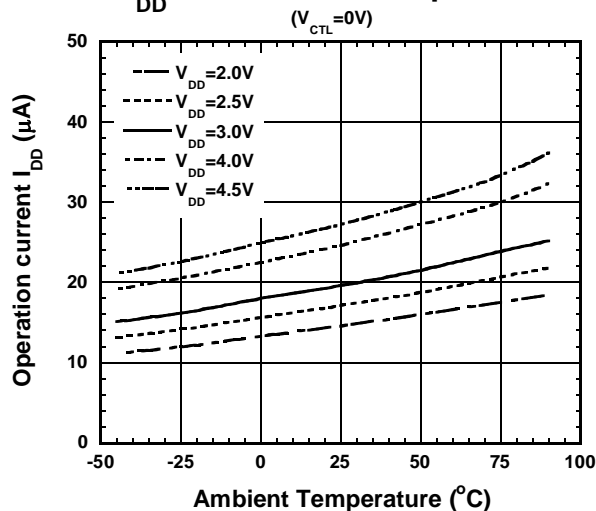
### P<sub>-1dB</sub> vs. Ambient Temperature



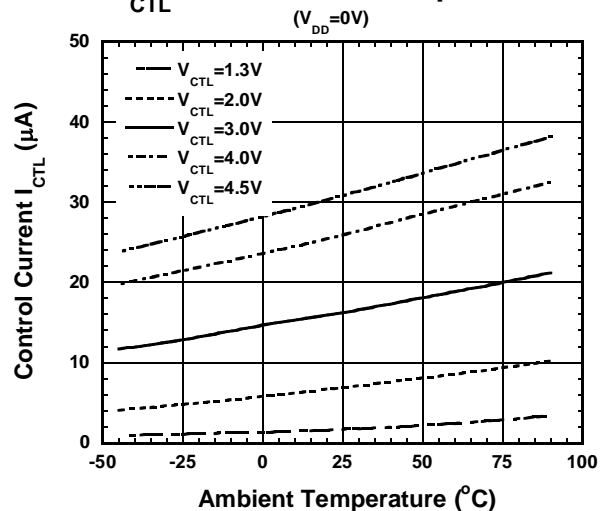
### T<sub>SW</sub> vs. Ambient Temperature



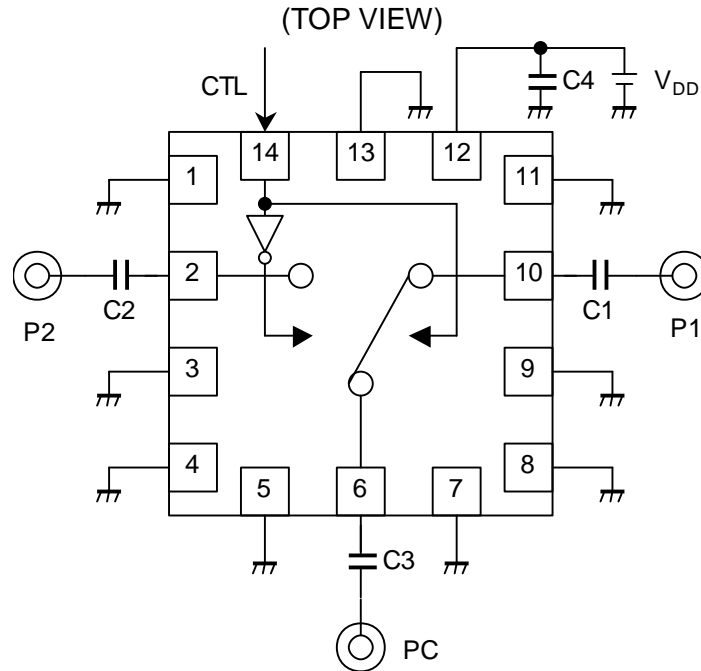
### I<sub>DD</sub> vs. Ambient Temperature



### I<sub>CTL</sub> vs. Ambient Temperature



## APPLICATION CIRCUIT

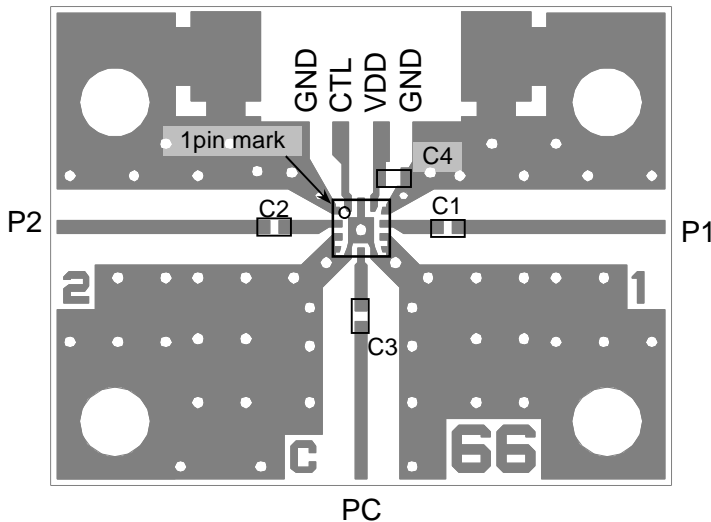


## PARTS LIST

Parts ID	Value	Notes
C1~C4	1000pF	Murata MFG (GRM15)

## TEST PCB LAYOUT

(TOP VIEW)



PCB SIZE = 19.4mm x 15.0mm  
 PCB: FR4, t = 0.2mm  
 CAPACITOR: SIZE 1005  
 STRIP LINE WIDTH = 0.4mm( $Z_0=50\Omega$ )

### PCB LOSS

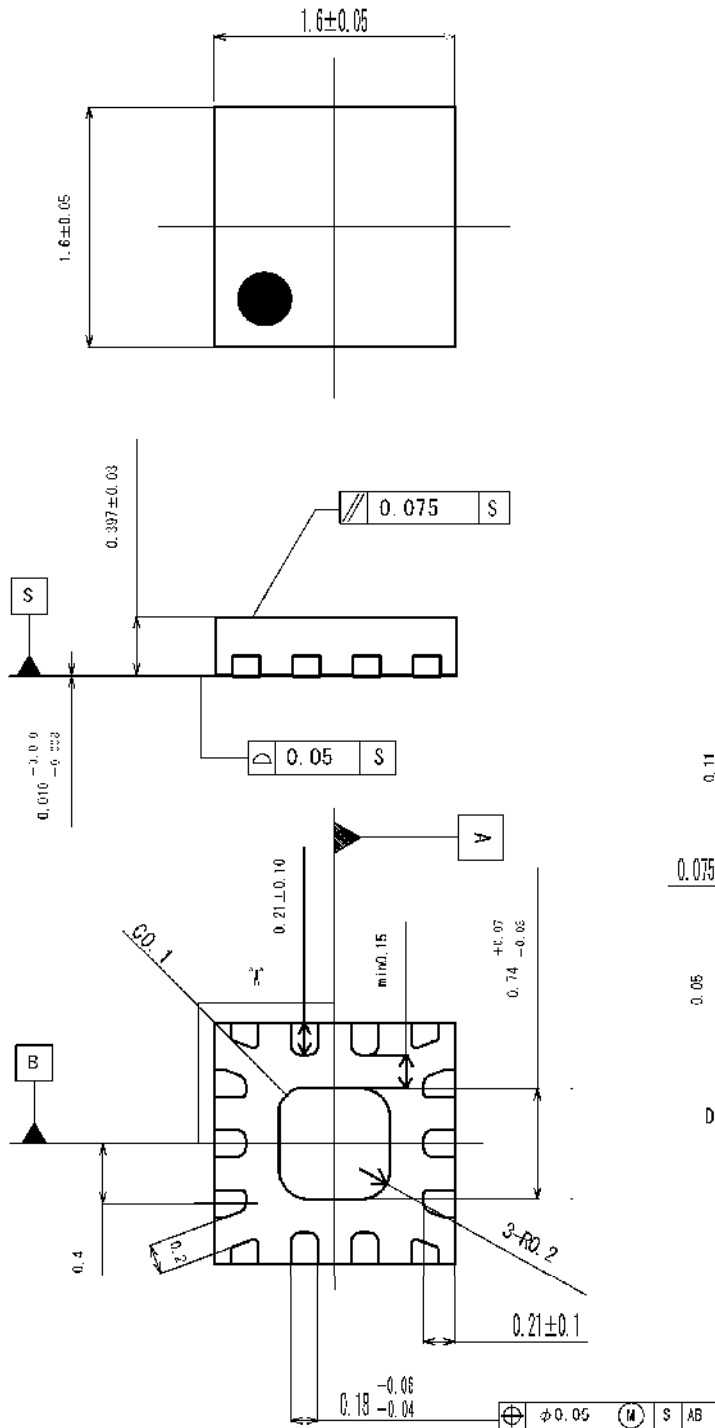
FREQ. (MHz)	PCB LOSS (dB)
250	0.11
1000	0.24
2200	0.40

\*) Including PCB, Connector and DC Blocking Capacitor Losses

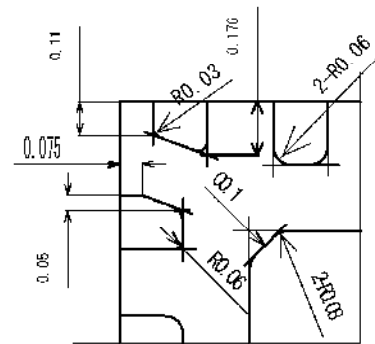
## PRECAUTIONS

- [1] The DC blocking capacitors have to be placed at RF terminal of PC, P1 and P2.
- [2] For good RF performance, the ground terminals must be placed possibly close to ground plane of substrate, and through holes for GND should be placed near by the pin connection.
- [3] Bypass capacitor (C4) should be placed close to terminal of VDD to reduce stripline influence of RF characteristics.

## PACKAGE OUTLINE (EQFN14-D7)



Units : mm  
 Board : Cu  
 Terminal treat : SnBi  
 Molding material : Epoxy resin  
 Weight : 3.4 mg



Details of "A" part (x 2)

### Cautions on using this product

- This product contains Gallium-Arsenide (GaAs) which is a harmful material.
- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

### [CAUTION]

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  - Life Maintenance Medical Equipment
  - Fire Alarms / Intruder Detectors
  - Vehicle Control Equipment (automotive, airplane, railroad, ship, etc.)
  - Various Safety Devices
  - Traffic control system
  - Combustion equipment

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8. **Quality Warranty**
  - 8-1. **Quality Warranty Period**

In the case of a product purchased through an authorized distributor or directly from us, the warranty period for this product shall be one (1) year after delivery to your company. For defective products that occurred during this period, we will take the quality warranty measures described in section 8-2. However, if there is an agreement on the warranty period in the basic transaction agreement, quality assurance agreement, delivery specifications, etc., it shall be followed.
  - 8-2. **Quality Warranty Remedies**

When it has been proved defective due to manufacturing factors as a result of defect analysis by us, we will either deliver a substitute for the defective product or refund the purchase price of the defective product.

Note that such delivery or refund is sole and exclusive remedies to your company for the defective product.
  - 8-3. **Remedies after Quality Warranty Period**

With respect to any defect of this product found after the quality warranty period, the defect will be analyzed by us. On the basis of the defect analysis results, the scope and amounts of damage shall be determined by mutual agreement of both parties. Then we will deal with upper limit in Section 8-2. This provision is not intended to limit any legal rights of your company.
9. Anti-radiation design is not implemented in the products described in this document.
10. The X-ray exposure can influence functions and characteristics of the products. Confirm the product functions and characteristics in the evaluation stage.
11. WLCSP products should be used in light shielded environments. The light exposure can influence functions and characteristics of the products under operation or storage.
12. Warning for handling Gallium and Arsenic (GaAs) products (Applying to GaAs MMIC, Photo Reflector). These products use Gallium (Ga) and Arsenic (As) which are specified as poisonous chemicals by law. For the prevention of a hazard, do not burn, destroy, or process chemically to make them as gas or power. When the product is disposed of, please follow the related regulation and do not mix this with general industrial waste or household waste.
13. Please contact our sales representatives should you have any questions or comments concerning the products or the technical information.



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