MPQ8633B-H

16V, 20A, Configurable-Frequency, Synchronous Step-Down Converter with Adjustable Current Limit and Voltage Tracking

DESCRIPTION

The MPQ8633B-H is a fully integrated, high-frequency, synchronous step-down converter. It offers a compact solution that can achieve up to 20A of output current (I_{OUT}) across a wide input voltage (V_{IN}) range, with excellent load and line regulation. The MPQ8633B-H operates at high efficiency across the entire I_{OUT} load range.

Internally compensated constant-on-time (COT) control provides fast transient response and eases loop stabilization.

The adjustable switching frequency (f_{SW}) can be set to 600kHz, 800kHz, or 1000kHz by configuring the MODE pin. This maintains a constant f_{SW}, regardless of the output voltage (V_{OUT}) or V_{IN}.

The V_{OUT} start-up ramp is controlled via an internal timer (1ms). For a longer internal timer, add a capacitor to the TRK/REF pin. An open-drain power good (PGOOD) signal indicates whether V_{OUT} is within its nominal voltage range. If the input supply fails to power the MPQ8633B-H, then PGOOD is clamped at about 0.7V via an external pull-up voltage.

Full protection features include over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and thermal shutdown.

The MPQ8633B-H requires a minimal number of readily available, standard external components, and is available in a QFN-21 (3mmx4mm) package.

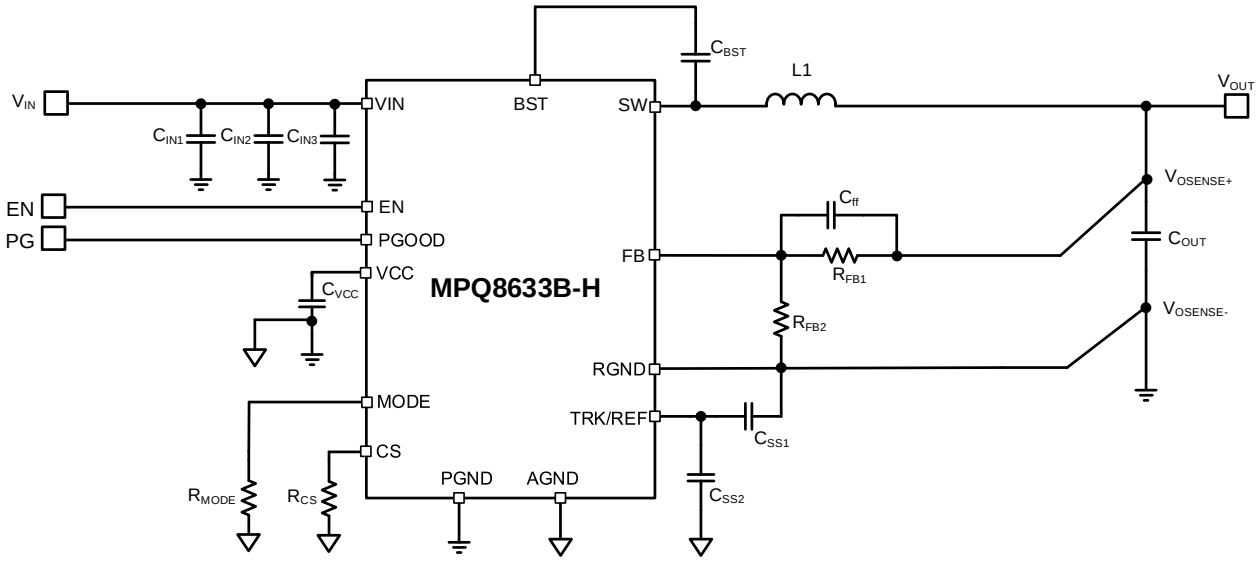
FEATURES

- Wide Input Voltage (V_{IN}) Range
  - 2.7V to 16V V_{IN} Range with External 3.3V VCC Bias
  - 4V to 16V V_{IN} Range with Internal Bias or External 3.3V VCC Bias
- Differential V_{OUT} Remote Sense
- Configurable Accurate Current Limit
- 20A Output Current (I_{OUT})
- Low $R_{DS(ON)}$ Integrated Power MOSFETs
- Proprietary Switching Loss Reduction Technique
- Adaptive Constant-On-Time (COT) Control for Fast Transient Response
- Stable with Zero ESR Output Capacitor
- 0.5% V_{REF} for 0°C to 70°C T_J Range
- 1% V_{REF} for -40°C to +125°C T_J Range
- Selectable Pulse Skip Mode (PSM)/Forced Continuous Conduction Mode (FCCM)
- Excellent Load Regulation
- V_{OUT} Tracking
- PGOOD Active Clamped Low during Power Failure
- Configurable Soft-Start Time (t_{SS}) from 1ms
- Pre-Bias Start-Up
- 600kHz, 800kHz, or 1000kHz Selectable f_{SW}
- Non-Latch OCP, OVP, UVP, UVLO, and Thermal Shutdown
- Adjustable Output between 0.6V and 90% of V_{IN}, with 5.5V Maximum
- Available in a QFN-21 (3mmx4mm) Package

APPLICATIONS

- Telecommunication/Networking Systems
- Servers, Cloud-Computing, and Storage
- Base Stations
- General-Purpose POL Systems
- 12V Distribution Power Systems
- High-End Televisions
- Game Consoles and Graphic Cards

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MPQ8633B-HGLE*	QFN-21 (3mmx4mm)	*See Below*	1

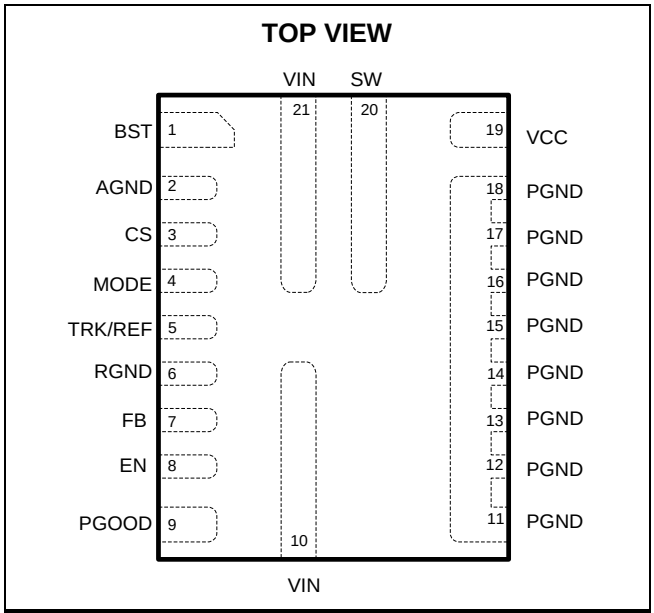
* For Tape & Reel, add suffix -Z (e.g. MPQ8633B-HGLE-Z).

TOP MARKING

MPYW
8633
BLLL
EH

MP: MPS prefix
Y: Year code
W: Week code
8633B: First five digits of the part number
LLL: Lot number
E: Package prefix
H: Non-latch OVP

PACKAGE REFERENCE



QFN-21 (3mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1	BST	**Bootstrap.** Connect a capacitor between the SW and BST pins to form a floating supply across the high-side MOSFET (HS-FET) driver.
2	AGND	**Analog ground.** Use the AGND pin as the control circuit reference point.
3	CS	**Current limit setting.** Connect a resistor to AGND to set the current limit. See the Current Sense (CS) and Over-Current Protection (OCP) section on page 15 for more details.
4	MODE	**Mode selection.** Configure the MODE pin to select forced continuous conduction mode (FCCM), pulse skip mode (PSM), or the operating switching frequency (f_{SW}). See Table 1 on page 14 for more details.
5	TRK/REF	**External tracking voltage input.** The output voltage (V_{OUT}) tracks the TRK/REF input signal. Use a ceramic decoupling capacitor placed as close to the TRK/REF pin as possible to decouple TRK/REF. Capacitors with X7R or X5R grade dielectrics are recommended due to their stable temperature characteristics. The soft-start time (t_{SS}) determines the capacitance of the TRK/REF capacitor ($C_{TRK/REF}$). The capacitance of this capacitor determines the soft-start time. See the Soft Start (SS) section on page 14 for more details.
6	RGND	**Differential remote sense negative input.** Connect the RGND pin to the negative side of the voltage sense point. Short RGND to GND if not used.
8	EN	**Enable.** The EN pin is an input signal that turns the converter on and off. Pull EN high to turn the converter on; pull EN low to turn it off. For automatic start-up, use a pull-up resistor or a resistive voltage divider to connect the EN and VIN pins. Do not float EN.
9	PGOOD	**Power good output.** The PGOOD pin is an open-drain signal. Use a pull-up resistor connected to a DC voltage for a logic high signal that indicates whether V_{OUT} is within its regulation range. There is a delay (about 1ms) between when $V_{FB} \geq 92.5\%$ of the reference voltage (V_{REF}) and when PGOOD is pulled high.
10, 21	VIN	**Input voltage.** The VIN pin supplies power for the internal MOSFET and the converter. Use decoupling input capacitors to decouple the input rail. Use wide PCB traces to make this connection.
11, 12, 13, 14, 15, 16, 17, 18	PGND	**System ground.** The PGND pin is the reference ground for the regulated V_{OUT}. Therefore, care must be taken during PCB layout. Use wide PCB traces to make the connection.
19	VCC	**Internal 3V LDO output.** The VCC pin supplies power for the driver and control circuits. Use a 1µF decoupling ceramic capacitor placed as close to the VCC pin as possible to decouple VCC. Capacitors with X7R or X5R grade dielectrics are recommended due to their stable temperature characteristics.
20	SW	**Switch output.** Connect the SW pin to the inductor and bootstrap capacitor (C_{BST}). SW is pulled up to VIN by the HS-FET during the pulse-width modulation (PWM) duty cycle on time (t_{ON}). (I_L) SW is pulled low by the inductor current during the PWM duty cycle off-time (t_{OFF}). Use wide PCB traces to make this connection.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 18V
$V_{SW(DC)}$ .....-0.3V to +18.3V
V_{SW} (25ns) (2) .....-3V to +25V
V_{SW} (25ns) .....-5V to +25V
V_{BST} .....-0.3V to +22.3V
V_{CC}, EN 4.5V
All other pins .....-0.3V to +4.3V
Junction temperature .....170°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +170°C

ESD Ratings

Human body model (HBM).....Class 2
Charged device model (CDM).....Class C2B

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....4V to 16V
V_{IN} (DC) - V_{SW} (DC) (4).....-0.3V to V_{IN} + 0.3V
V_{SW} (DC) (4).....-0.3V to V_{IN} + 0.3V
Output voltage (V_{OUT}).....0.6V to 5.5V
External VCC bias (V_{CC_EXT}).....3.12V to 3.6V
Maximum output current (I_{OUT_MAX})..... 20A
Maximum output current limit (I_{OC_MAX})..... 24A
Maximum peak inductor current (I_{L_PEAK}) 28A
EN voltage (V_{EN}) 3.6V
Operating junction temp (T_J)…. -40°C to +125°C

Thermal Resistance (5) (6) θ_{JB} θ_{JC_TOP}

QFN-21 (3mmx4mm)..... 8..... 18..... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Measured using a differential oscilloscope probe.
3) The device is not guaranteed to function outside of its operating conditions.
4) If the input voltage (V_{IN}) is 16V and the switching period is ≤25ns with a maximum repetition rate (1000kHz), then the voltage rating should be between -3V and +23V.
5) θ_{JB} is the thermal resistance from the junction to the board near the PGND soldering point.
6) θ_{JC_TOP} is the thermal resistance from the junction to the top of the package.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Shutdown current	I_{SD}	V_{EN} = 0V		11	30	μA
Quiescent current	I_Q	V_{EN} = 2V, V_{FB} = 0.65V		650	850	μA
MOSFET						
Switch leakage	I_{SWLKG_HS}	V_{EN} = 0V, V_{SW} = 0V		0	10	μA
	I_{SWLKG_LS}	V_{EN} = 0V, V_{SW} = 12V		0	30	
Current Limit						
Current limit threshold	V_{LIM}		1.15	1.2	1.25	V
I_{CS} to I_{OUT} ratio	I_{CS} / I_{OUT}	I_{OUT} ≥ 2A	9	10	11	μA/A
Low-side negative current limit	I_{LIMIT_NEG}			-18		A
Negative current limit timeout (7)	t_{NCL}			200		ns
Switching Frequency						
Switching frequency (8)	f_{SW}	MODE and GND are connected, I_{OUT} = 0A, V_{OUT} = 1V	480	600	720	kHz
		MODE = 30.1kΩ, I_{OUT} = 0A, V_{OUT} = 1V	680	800	920	kHz
		MODE = 60.4 kΩ, I_{OUT} = 0A, V_{OUT} = 1V	850	1000	1150	kHz
Minimum on time (7)	t_{ON_MIN}	V_{FB} = 500mV			50	ns
Minimum off time (7)	t_{OFF_MIN}	V_{FB} = 500mV			180	ns
Over-Voltage and Under-Voltage Protection						
OVP threshold	V_{OVP}		113	116	119	% of V_{REF}
UVP threshold	V_{UVP}		77	80	83	% of V_{REF}
Feedback Voltage and Soft Start						
Feedback voltage	V_{REF}	T_J = -40°C to +125°C	594	600	606	mV
		T_J = 0°C to 70°C	597	600	603	mV
TRK/REF source current	I_{TRK/REF_SOURCE}	$V_{TRK/REF}$ = 0V		42		μA
TRK/REF sink current	I_{TRACK_SINK}	$V_{TRK/REF}$ = 1V		12		μA
Soft-start time	t_{SS}	C_{TRACK} = 1nF, T_J = 25°C	0.75	1	1.25	ms
Error Amplifier (EA)						
EA offset	V_{OS}		-3	0	+3	mV
Feedback (FB) current	I_{FB}	V_{FB} = V_{REF}		50	100	nA
Enable (EN) and Under-Voltage Lockout (UVLO)						
EN input rising threshold	V_{EN_RISING}		1.17	1.22	1.27	V
EN hysteresis	V_{EN_HYS}			200		mV
EN input current	I_{EN}	V_{EN} = 2V		0		μA
V_{IN} UVLO						
V_{IN} UVLO rising threshold	$V_{IN\_UVLO\_RISING}$	V_{CC} = 3.3V		2.4	2.7	V
V_{IN} UVLO falling threshold	$V_{IN\_UVLO\_FALLING}$	V_{CC} = 3.3V		1.85	2.15	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VCC Regulator						
VCC UVLO rising threshold	$V_{CC\_UVLO\_RISING}$		2.65	2.8	2.95	V
VCC UVLO falling threshold	$V_{CC\_UVLO\_FALLING}$		2.35	2.5	2.65	V
VCC regulator	V_{CC}		2.88	3	3.12	V
VCC load regulation		I_{CC} = 25mA		0.5		%
Power Good (PGOOD)						
PGOOD high rising threshold	$V_{PGOOD\_HIGH\_RISING}$	FB from low to high	89.5	92.5	95.5	% of V_{REF}
PGOOD low rising threshold	$V_{PGOOD\_LOW\_RISING}$	FB from low to high	113	116	119	% of V_{REF}
PGOOD low falling threshold	$V_{PGOOD\_LOW\_FALLING}$	FB from high to low	77	80	83	% of V_{REF}
PGOOD low to high delay	t_{DELAY_PGOOD}	T_J = 25°C	0.63	0.9	1.17	ms
PGOOD sink current capability	V_{PGOOD_SINK}	I_{PG} = 10mA			0.5	V
PGOOD leakage current	I_{PGOOD_LEAK}	V_{PG} = 3.3V			3	µA
PGOOD low-level output voltage (V_{OUT})	$V_{PGOOD\_LOW\_100}$	V_{IN} = 0V, T_J = 25°C, pull PGOOD up to 3.3V via a 100kΩ pull-up resistor		650	800	mV
	$V_{PGOOD\_LOW\_10}$	V_{IN} = 0V, T_J = 25°C, pull PGOOD up to 3.3V via a 10kΩ pull-up resistor		750	900	mV
Thermal Protection						
Thermal shutdown (7)	T_{SD}			160		°C
Thermal shutdown hysteresis (7)				30		°C

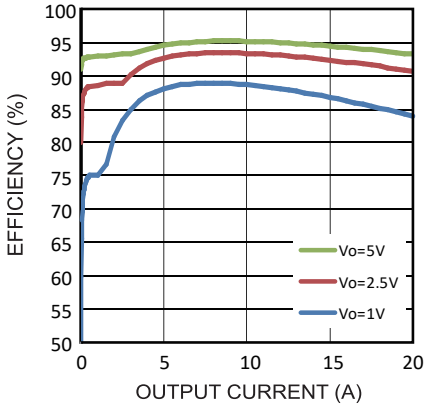
Notes:

7) Guaranteed by design.
8) Guaranteed by over-temperature correlation.

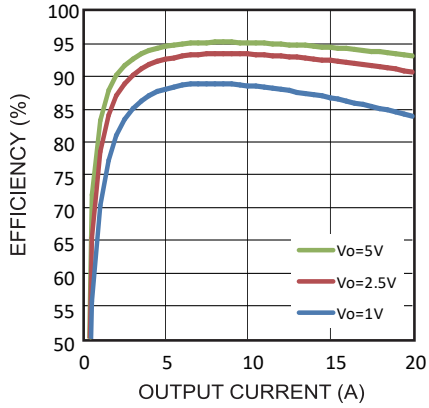
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, T_A = 25°C, V_{OUT} = 1.2V, f_{SW} = 800kHz, unless otherwise noted.

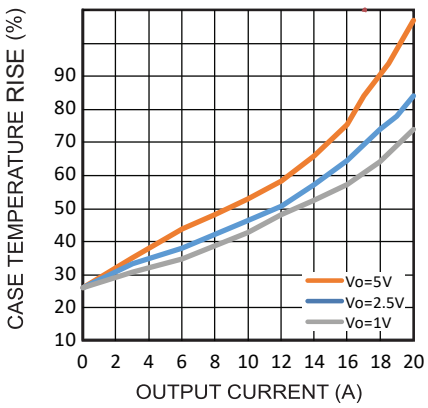
Efficiency vs. Output Current
PSM, 0.4µH, 800kHz



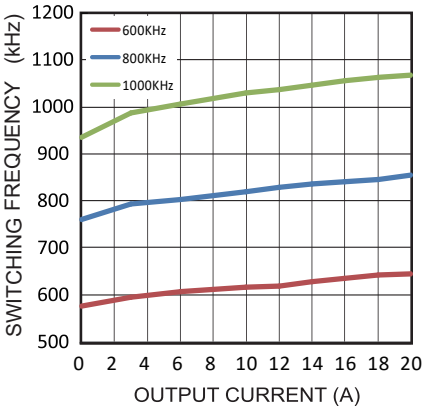
Efficiency vs. Output Current
FCCM, 0.4µH, 800kHz



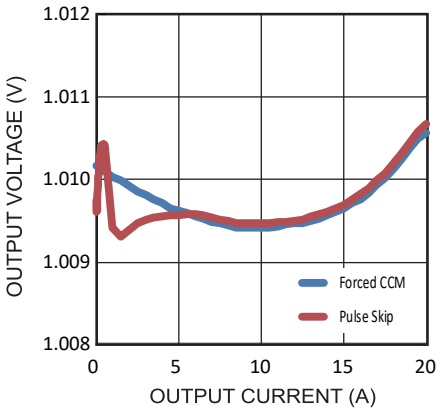
Case Temperature Rise
800kHz, no air flow



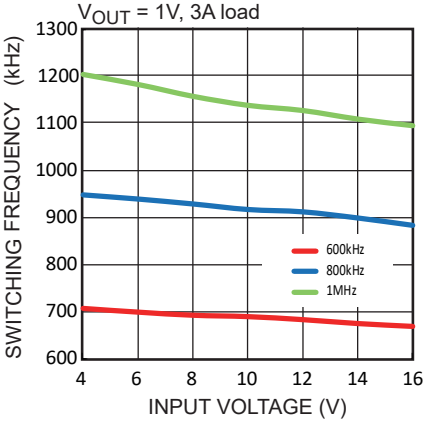
Switching Frequency vs. Output Current
FCCM



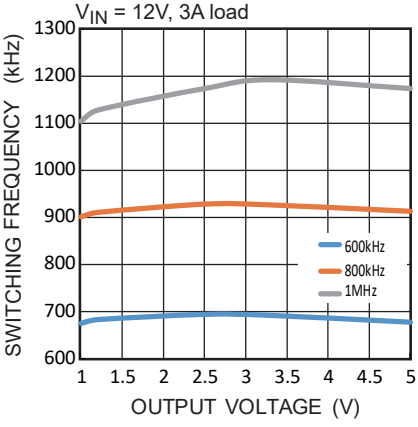
Load Regulation



Switching Frequency vs. Input Voltage
V_{OUT} = 1V, 3A load



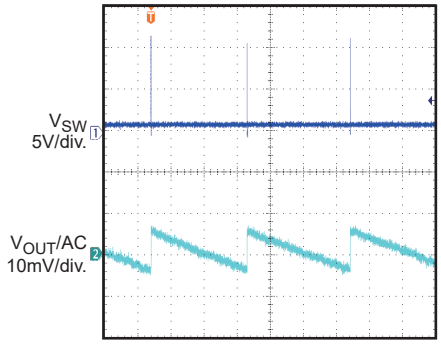
Switching Frequency vs. Output Voltage
V_{IN} = 12V, 3A load



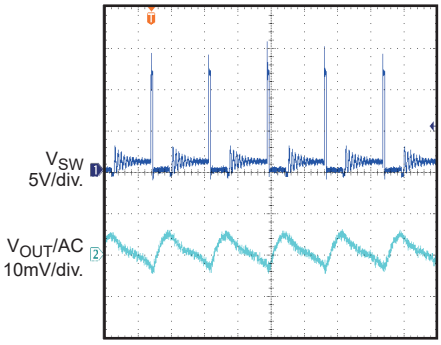
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = 25°C, V_{OUT} = 1.2V, f_{SW} = 800kHz, unless otherwise noted.

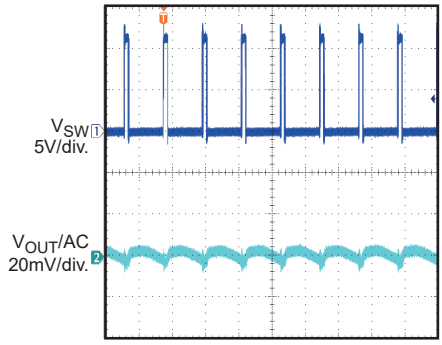
Steady State
I_{OUT} = 0A, PSM



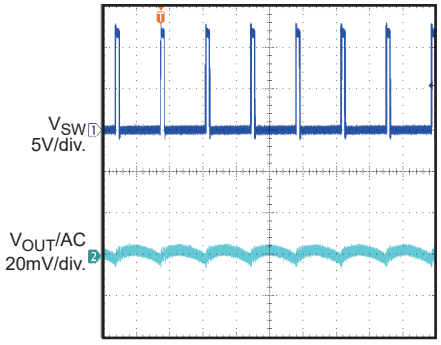
Steady State
I_{OUT} = 0.5A, PSM



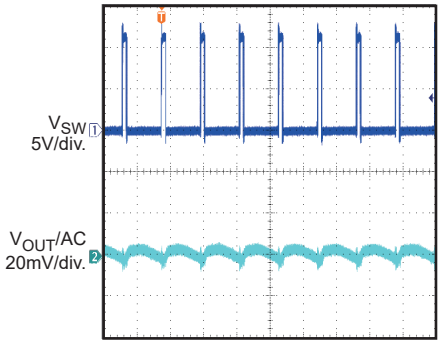
Steady State
I_{OUT} = 20A, PSM



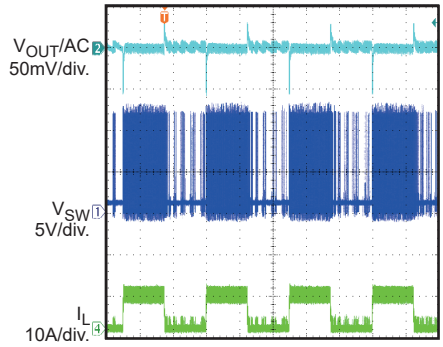
Steady State
I_{OUT} = 0A, FCCM



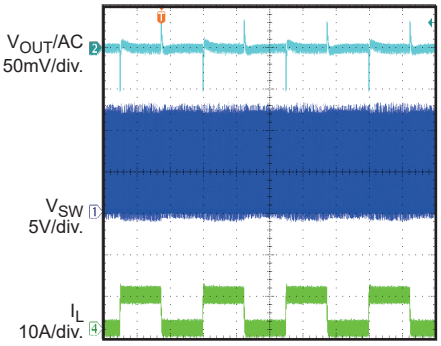
Steady State
I_{OUT} = 20A, FCCM



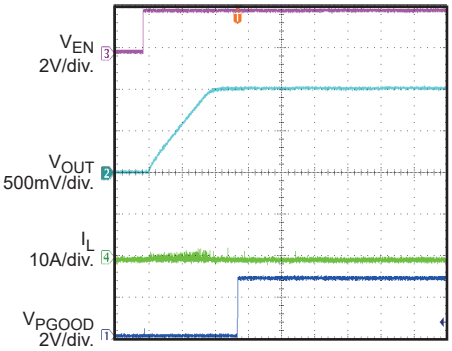
Load Transient
I_{OUT} = 0A to 8A, PSM



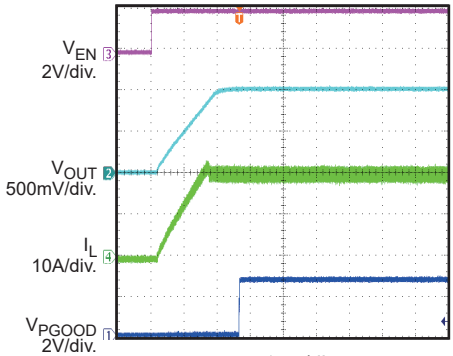
Load Transient
I_{OUT} = 0A to 8A, FCCM



Power Up through EN
I_{OUT} = 0A, PSM



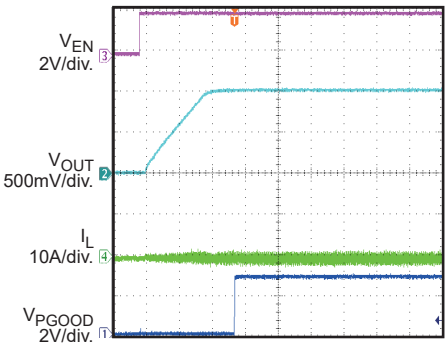
Power Up through EN
I_{OUT} = 20A, PSM



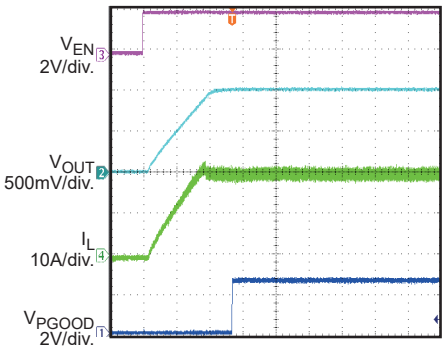
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = 25°C, V_{OUT} = 1.2V, f_{SW} = 800kHz, unless otherwise noted.

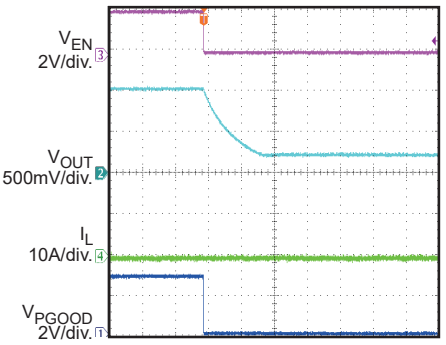
Start-Up through EN
I_{OUT} = 0A, FCCM



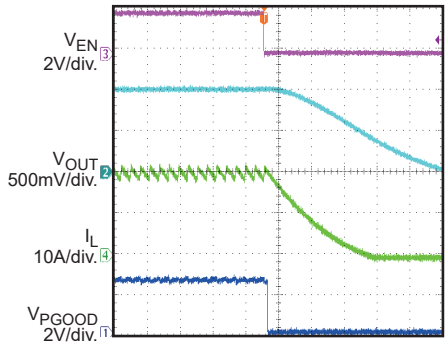
Start-Up through EN
I_{OUT} = 20A, FCCM



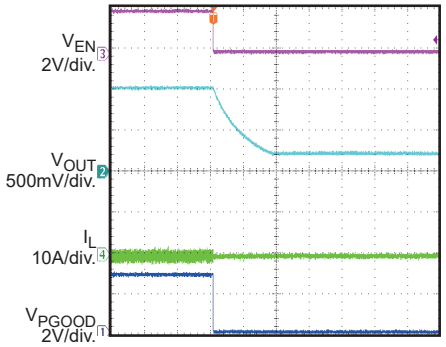
Shutdown through EN
I_{OUT} = 0A, PSM



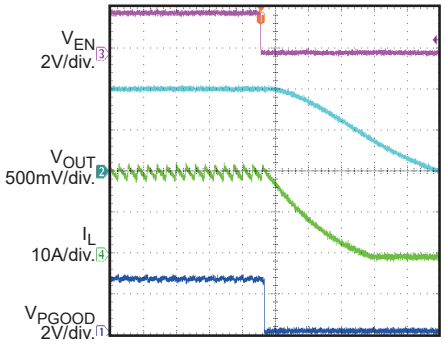
Shutdown through EN
I_{OUT} = 20A, PSM



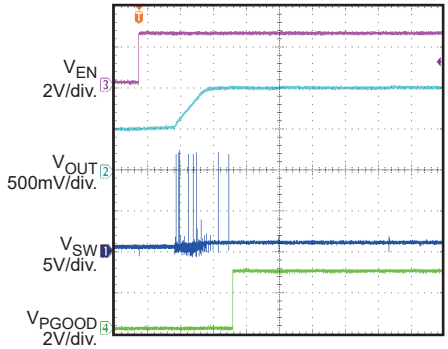
Shutdown through EN
I_{OUT} = 0A, FCCM



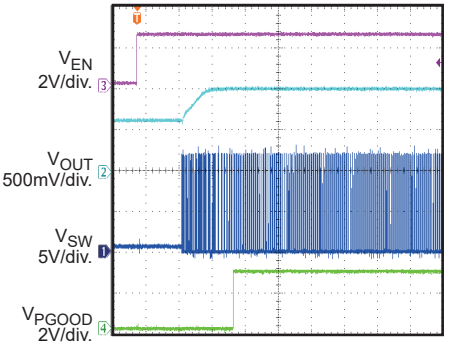
Shutdown through EN
I_{OUT} = 20A, FCCM



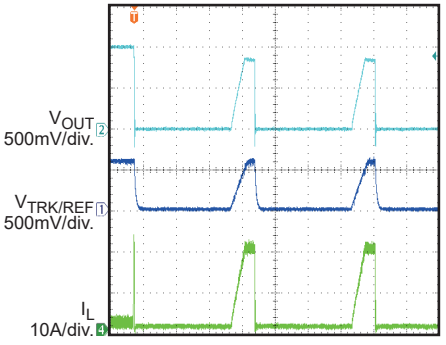
Pre-Bias Start-Up
PSM



Pre-Bias Start-Up
FCCM



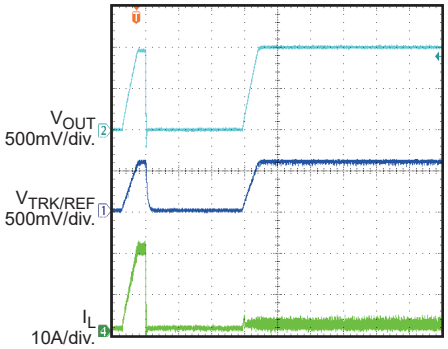
OVP Entry



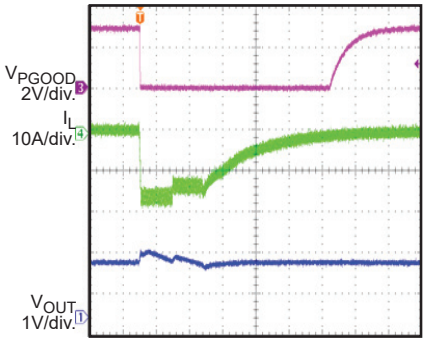
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = 25°C, V_{OUT} = 1.2V, f_{SW} = 800kHz, unless otherwise noted.

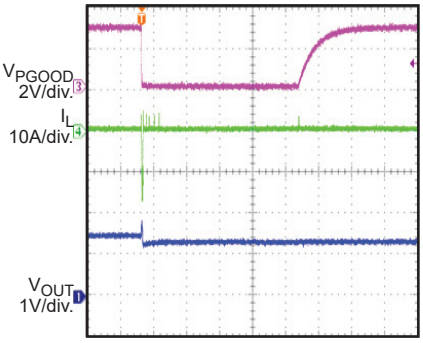
OCP Entry



Over-Voltage Protection
FCCM



Over-Voltage Protection
PSM



FUNCTIONAL BLOCK DIAGRAM

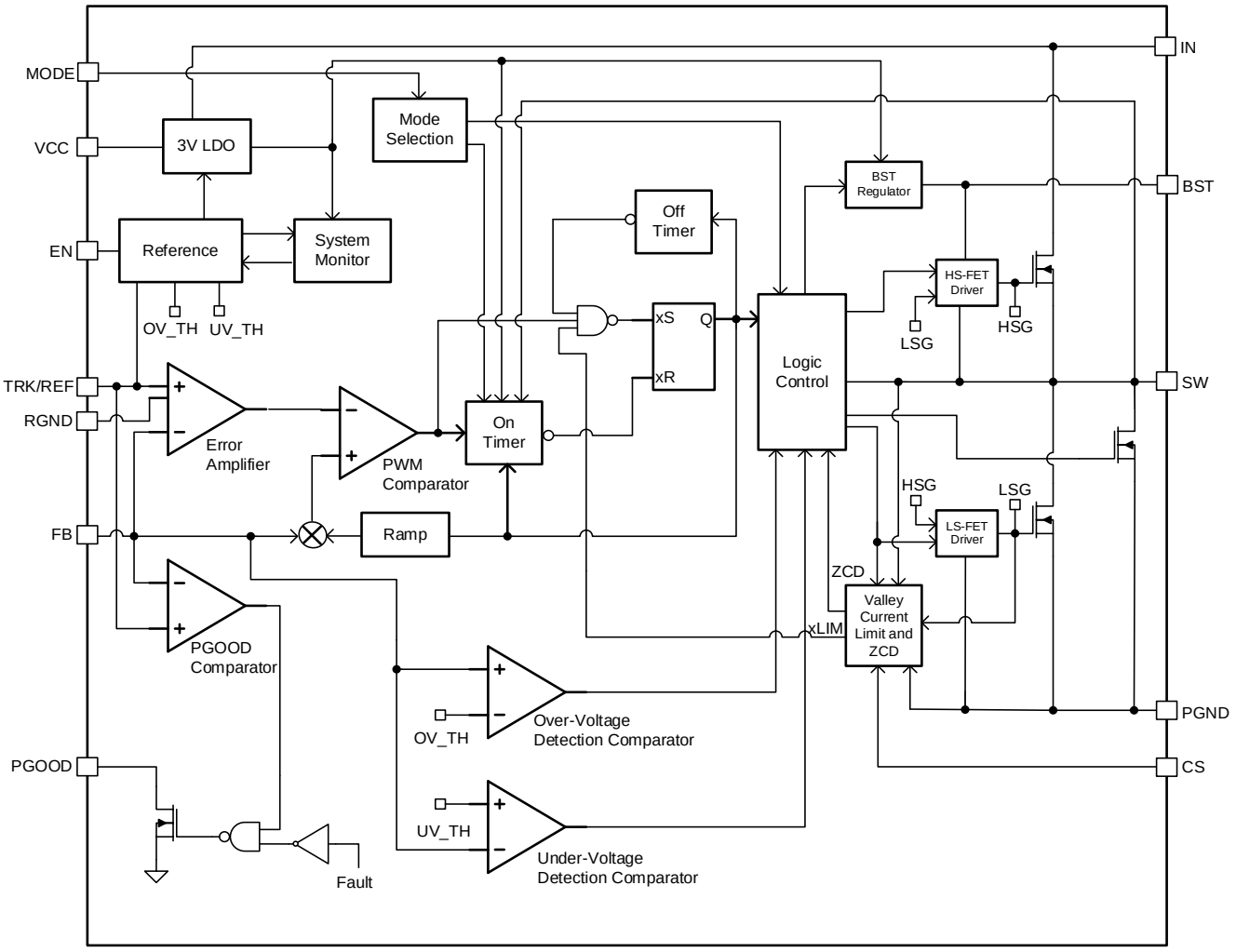


Figure 1: Functional Block Diagram

OPERATION

Constant-On-Time (COT) Control

The MPQ8633B-H employs constant-on-time (COT) control to achieve fast load transient response. Figure 2 shows the COT control stage.

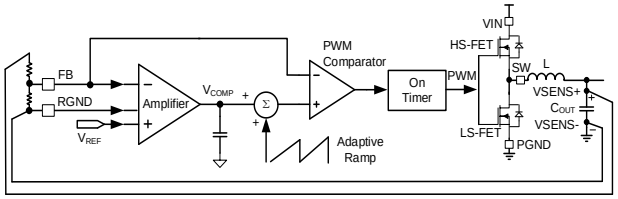


Figure 2: COT Control

The operational amplifier corrects error voltages between V_{FB} and V_{REF}. The MPQ8633B-H also uses the amplifier to provide excellent load regulation across the entire load range in both forced continuous conduction mode (FCCM) and pulse skip mode (PSM).

The RGND pin provides the differential output voltage (V_{OUT}) remote sense function. For best performance, the pair of the remote sense traces should be kept in low impedance state.

The MPQ8633B-H has internal ramp compensation to support a low ESR, MLCC output capacitor (C_{OUT}) solution. The adaptive internal ramp provides stable operation across the entire operating input voltage (V_{IN}) range and V_{OUT} range, with a proper design of the output L/C filter.

Pulse-Width Modulation (PWM) Mode

The operation amplifier corrects any error between V_{FB} and V_{REF}, and generates a fairly smooth DC voltage comp voltage (V_{COMP}). The internal ramp is superimposed onto V_{COMP}, which is compared to the V_{FB}. If V_{FB} drops below V_{COMP}, then the high-side MOSFET (HS-FET) turns on. The HS-FET remains on for a fixed on time (t_{ON}). t_{ON} is determined by V_{IN}, V_{OUT}, and the selected switching frequency (f_{SW}). After t_{ON} has elapsed, the HS-FET turns off. It turns on again once V_{FB} drops below V_{COMP}. The MPQ8633B-H regulates V_{OUT} by repeating this operation. The low-side MOSFET (LS-FET) turns on once the HS-FET is off to minimize conduction loss. If both the HS-FET and the LS-FET turn on at the same time, then a dead short occurs between the VIN and PGND pins. This is called shoot-through. To avoid shoot-through, a dead time (DT) is generated internally between the HS-FET off time (t_{OFF}) and the LS-FET t_{ON}, and vice versa. Figure 3 shows PWM mode under heavy-load conditions.

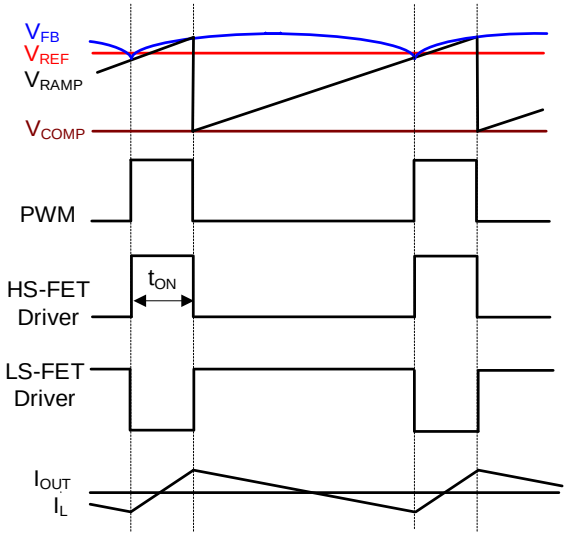


Figure 3: CCM during Heavy-Load Operation

Continuous Conduction Mode (CCM)

If the output current (I_{OUT}) is high and the inductor current (I_L) is above 0A, then the part operates in continuous conduction mode (CCM) (see Figure 3). The MPQ8633B-H can also be configured to operate in forced continuous conduction mode (FCCM) when the I_{OUT} is low. See the Mode Selection section on page 14 for more details.

f_{SW} remains fairly constant in CCM (PWM mode), which maintains a constant output voltage ripple (ΔV_{OUT}) throughout the entire load range.

Pulse-Skip Mode (PSM)

The MPQ8633B-H can be configured to operate in pulse-skip mode (PSM) at light loads to improve efficiency. I_L decreases as the load decreases. Once I_L reaches 0A, the device enters PSM. See the Mode Selection section on page 14 for more details.

If V_{FB} drops below V_{COMP}, then the HS-FET turns on for a fixed interval. Once the HS-FET turns off, the LS-FET turns on until I_L reaches 0A. In PSM, V_{FB} should not reach V_{COMP} while I_L

approaches 0A. The LS-FET driver turns on and enters a high impedance (Hi-Z) state once I_L reaches 0A. A current modulator takes control of the LS-FET and limits I_L to below -1mA. The output capacitors discharge slowly to PGND via the LS-FET. In PSM at light loads, the HS-FET does not turn on as frequently as in FCCM. As a result, PSM has higher efficiency compared to that in FCCM. Figure 4 shows PSM under light-load conditions.

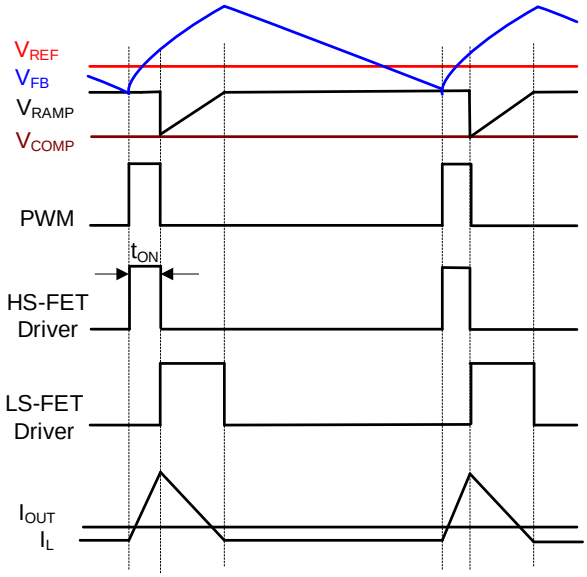


Figure 4: PSM during Light-Load Operation

As I_{OUT} increases from light load, the time period regulated by the current modulator decreases. The HS-FET turns on more frequently, and f_{SW} increases accordingly. I_{OUT} reaches its critical level once the current modulator time is 0s. The critical level of the I_{OUT} can be calculated with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (1)$$

The device enters CCM once I_{OUT} exceeds its critical level. After I_{OUT} has exceeded its critical level, f_{SW} remains fairly constant across the entire I_{OUT} range.

The MPQ8633B-H can be configured to operate in FCCM, even under light-load conditions (see Table 1).

Mode Selection

The MPQ8633B-H provides both FCCM and PSM for light-load operation. It also has three selectable f_{SW} options. The operation mode and f_{SW} is set by the resistor connected between MODE and AGND or MODE and VCC. Choose a resistance to select the desired mode and f_{SW}. (see Table 1).

Table 1: Mode Selection

MODE Resistor Value	Mode at Light Loads	Switching Frequency
VCC	PSM	600kHz
243kΩ (±20%) to AGND	PSM	800kHz
121kΩ (±20%) to AGND	PSM	1000kHz
AGND	FCCM	600kHz
30.1kΩ (±20%) to AGND	FCCM	800kHz
60.4kΩ (±20%) to AGND	FCCM	1000kHz

Soft Start (SS)

The MPQ8633B-H has a 1ms minimum soft-start time (t_{SS}). Connect a soft-start capacitor (C_{SS}) between the TRK/REF and RGND pins to increase t_{SS}.

The total soft-start capacitance (C_{SS}) can be calculated with Equation (2):

$$C_{SS}(nF) = \frac{t_{ss}(ms) \times 36\mu A}{0.6(V)} \quad (2)$$

C_{SS} can also be calculated with Equation (3):

$$C_{SS} = C_{SS1} + C_{SS2} \quad (3)$$

Where C_{SS2} is ≥22nF.

Output Voltage Tracking and Reference

The MPQ8633B-H provides an analog input pin (TRK/REF) to track a second power supply or accept an external reference. If an external voltage is connected to TRK/REF, then it acts as the reference voltage (V_{REF}) for V_{OUT}. V_{FB} also follows this external voltage signal, and the soft-start settings are ignored. The TRK/REF input signal can be between 0.3V and 1.4V. During start-up, the TRK/REF should exceed 600mV to ensure proper operation. After that, TRK/REF can be set to any value between 0.3V and 1.4V.

Pre-Biased Start-Up

The MPQ8633B-H is designed for monotonic start-up into a pre-biased load. If V_{OUT} is pre-biased to a certain voltage during start-up, then the HS-FET and LS-FET turn off until the on the TRK/REF voltage ($V_{TRK/REF}$) exceeds the V_{FB}. Before the TRK/REF voltage reaches the pre-biased FB level, If the BST capacitor (C_{BST}) between the BST to SW pins is below 2.3V, and $V_{TRK/REF}$ has not reached the pre-biased FB level, then the LS-FET turns on to allow VCC to charge C_{BST}. The LS-FET turns on for short pulses, so the drop in the pre-biased voltage is negligible.

Current Sense (CS) and Over-Current Protection (OCP)

The MPQ8633B-H features an on-die current sense and a configurable positive current limit (I_{LIMIT}) threshold.

I_{LIMIT} is active while the IC is on. During the LS-FET on state, I_L (the SW current) is sensed and mirrored to the CS pin with the current-sense gain (G_{CS}) ratio. Connect a resistor (R_{CS}) between the CS and AGND pins to make the CS voltage (V_{CS}) proportional to I_L cycle-by-cycle. The HS-FET can only turn on once V_{CS} is below the internal over-current protection (OCP) threshold (V_{OCP}) while the LS-FET is on to limit the SW valley current cycle-by-cycle.

The current limit threshold (R_{CS}) can be calculated with Equation (4):

$$R_{CS}(\Omega) = \frac{V_{OCP}}{G_{CS} \times (I_{LIMIT} - \frac{(V_{IN} - V_{OUT}) \times V_{OOUT}}{V_{IN}} \times \frac{1}{2 \times L \times f_{SW}})} \quad (4)$$

Where V_{OCP} is 1.2V, G_{CS} is 10μA/A, and I_{LIMIT} is the desired current limit in amps.

After the MPQ8633B-H starts up, there is a delay time (t_{DELAY}) (3ms) before OCP and hiccup mode are active. If the IC detects an over-current (OC) condition for 31 consecutive cycles, or if V_{FB} drops below the under-voltage protection (UVP) threshold, the part enters hiccup mode. In hiccup mode, the HS-FET turns off, and the LS-FET turns on after zero current detection (ZCD). The TRK/REF capacitor ($V_{TRK/REF}$) is also discharged during hiccup mode. After about 11ms, the MPQ8633B-H initiates a soft start to resume normal operation. If the OC condition remains after 3ms, then the device repeats this operation until the OC condition is removed and V_{OUT} reaches its regulation voltage level.

Negative Inductor Current Limit

If the LS-FET detects a -18A current, then the LS-FET turns off for 200ns to limit the negative current.

Over-Voltage Protection (OVP)

The MPQ8633B-H monitors V_{OUT} continuously. The FB pin is connected to the tap of the feedback resistor divider to detect whether an over-voltage (OV) condition has occurred. This provides over-voltage protection (OVP) with hiccup mode for the device.

If V_{FB} exceeds 116% of V_{REF}, then OVP is triggered. The power good (PGOOD) pin is pulled down until it reaches the low-side negative current limit (I_{LIMIT_NEG}). Once the PGOOD current (I_{PGOOD}) reaches I_{LIMIT_NEG}, the LS-FET turns off for 200ns and the HS-FET turns on for 200ns. After 200ns, the LS-FET turns on again. The MPQ8633AH repeats this operation to discharge the OV condition on the output. Once V_{FB} drops below 105% of V_{REF}, the IC exits OVP discharge mode.

Thermal Shutdown

Thermal shutdown protects the IC from operating at exceedingly high temperatures by internally monitoring the junction temperature (T_J). If T_J exceeds the thermal shutdown threshold (typically 160°C), then the converter shuts down and discharges the TRK/REF capacitors. Once T_J drops below 130°C, then the converter initiates a SS to resume normal operation. There is a hysteresis of about 30°C. Thermal shutdown is a non-latch protection.

Output Voltage Setting and Remote Output Voltage Sensing

Choose a value for R_{FB1}. Then R_{FB2} can be calculated with Equation (5):

$$R_{FB2}(k\Omega) = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R_{FB1}(k\Omega) \quad (5)$$

For the best load transient response, place a feed-forward capacitor (C_{FF}) in parallel to R_{FB1}. R_{FB1} and C_{FF} add an extra zero to the system,

which improves loop response. R_{FB1} and C_{FF} are selected so that the zero is between 20kHz and 60kHz. This zero can be calculated with Equation (6):

$$f_Z = \frac{1}{2\pi \times R_{FB1} \times C_{FF}} \quad (6)$$

Power Good (PGOOD)

The MPQ8633B-H has a power good (PGOOD) output pin. PGOOD is the open-drain of a MOSFET. Connect PGOOD to V_{CC} or another external voltage source below 3.6V via a pull-up resistor (10kΩ). Once V_{IN} is applied, the MOSFET turns on and PGOOD is pulled down low before TRK/REF is ready. Once V_{FB} reaches 92.5% of V_{REF}, PGOOD is pulled high after a 0.8ms delay.

If V_{FB} drops to 80% of V_{REF} or exceeds 116% of the nominal V_{REF}, then PGOOD is pulled low. PGOOD can only be pulled high again after a SS is initiated.

If the input supply fails to power the IC, then PGOOD is pulled low, even when it is tied to an external DC source via a pull-up resistor. The relationship between the PGOOD voltage (V_{PGOOD}) and the pull-up current is shown in Figure 5.

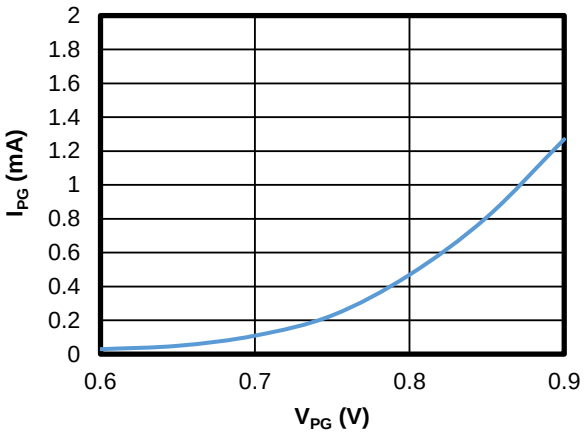


Figure 5: Pull-Up Current vs. PGOOD Voltage

Enable (EN) Configuration

The enable (EN) pin turns the converter on and off. Pull EN high to turn the converter on; pull EN low to turn it off. Do not float EN. EN can be driven by an analog or a digital control logic signal to enable and disable the part. The MPQ8633B-H provides accurate EN thresholds, which allows a resistor divider connected between the VIN and AGND pins can be used to configured V_{IN} to enable the part. This is highly recommended for applications with no dedicated EN control logic signals to avoid V_{EN} dropping below or exceeding the under-voltage lockout (UVLO) threshold during start-up and shutdown. The resistor divider values (R_{UP} + R_{DOWN}) can be calculated with Equation (7):

$$V_{IN\_START}(V) = V_{EN\_RISING} \times \frac{R_{UP} + R_{DOWN}}{R_{DOWN}} \quad (7)$$

Where V_{EN_RISING} is 1.22V.

Choose R_{UP} and R_{DOWN} so that that V_{EN} does not exceed 3.6V as V_{IN} reaches its maximum value.

EN can also be connected to VIN via a pull-up resistor (R_{UP}). Choose R_{UP} so that the maximum EN current is 50μA. R_{UP} can be calculated with Equation (8):

$$R_{UP}(k\Omega) = \frac{V_{IN\_MAX}(V)}{0.05(mA)} \quad (8)$$

APPLICATION INFORMATION

Selecting the Input Capacitor (C_{IN})

The step-down converter has a discontinuous input current (I_{IN}) and requires a capacitor to supply AC current to the step-down converter while maintaining the DC V_{IN}. Use ceramic capacitors for the best performance. Place the input capacitors as close to the VIN pin as possible.

The capacitance can vary significantly with the temperature. Capacitors with X5R and X7R dielectrics are recommended due to their stable temperature characteristics and low ESR.

The input capacitors should have a ripple current rating that exceeds the converter's maximum input ripple current. The input ripple current (I_{CIN}) can be estimated with Equation (9):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (9)$$

The worst case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (10):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (10)$$

For simplification, choose an input capacitor (C_{IN}) with an RMS current rating that exceeds half the maximum load current (I_{LOAD_MAX}). C_{IN} determines the converter's input voltage ripple (ΔV_{IN}). If there is a ΔV_{IN} requirement in the system, then select C_{IN} to meet the system's specification.

ΔV_{IN} can be calculated with Equation (11):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (11)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (12):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (12)$$

Selecting the Output Capacitor (C_{OUT})

The output capacitor (C_{OUT}) maintains the DC V_{OUT}. Use POSCAP or ceramic capacitors for the best performance. The output voltage ripple (ΔV_{OUT}) can be estimated with Equation (13):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \quad (13)$$

When using ceramic capacitors, the capacitance dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be calculated with Equation (14):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{\ 2} \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (14)$$

The capacitance also dominates the ΔV_{OUT}. For simplification, ΔV_{OUT} can be estimated with Equation (15):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (15)$$

Selecting the Inductor

The inductor supplies a constant current to the output load while being driven by the switching V_{IN}. A larger inductor results in less ripple current and lower ΔV_{OUT}; however, a larger inductor has a larger size, a higher series resistance, and a lower saturation current. Choose an inductor so that the peak-to-peak inductor ripple current (ΔI_L) is between 30% and 40% of the maximum switch I_{LIMIT}. The peak inductor current (I_{L_PEAK}) should be below the maximum switch I_{LIMIT}. The inductance (L) can be calculated with Equation (16):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (16)$$

Choose an inductor that will not saturate under the maximum I_{L_PEAK}. I_{L_PEAK} can be calculated with Equation (17):

$$I_{L\_PEAK} = I_{OUT} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (17)$$

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best performance, refer to Figure 6 and follow the guidelines below:

1. Place the input MLCC capacitors as close to VIN and PGND as possible.
2. Place the major MLCC capacitors on the same layer as the IC.
3. Ensure that both the VIN and PGND copper planes are large enough to minimize parasitic impedance.
4. Place as multiple PGND vias as close to PGND as possible to minimize both parasitic impedance and thermal resistance.
5. Place the VCC decoupling capacitor close to the device.
6. Connect AGND and PGND at the VCC capacitor's ground connection.
7. Place the BST capacitor (C_{SBT}) as close to the BST and SW pins as possible using ≥20 mil traces. It is recommended to have C_{SBT} be between 0.1µF and 1µF.
8. Place the REF capacitor (C_{REF}) close to TRK/REF and RGND.
9. Place a via on the PGOOD pad as close to the IC as possible, and at least 10mm away from the positive side of the first input decoupling capacitor.
10. Place the VOSENSE capacitor between the output sensing traces, and close to the FB components.

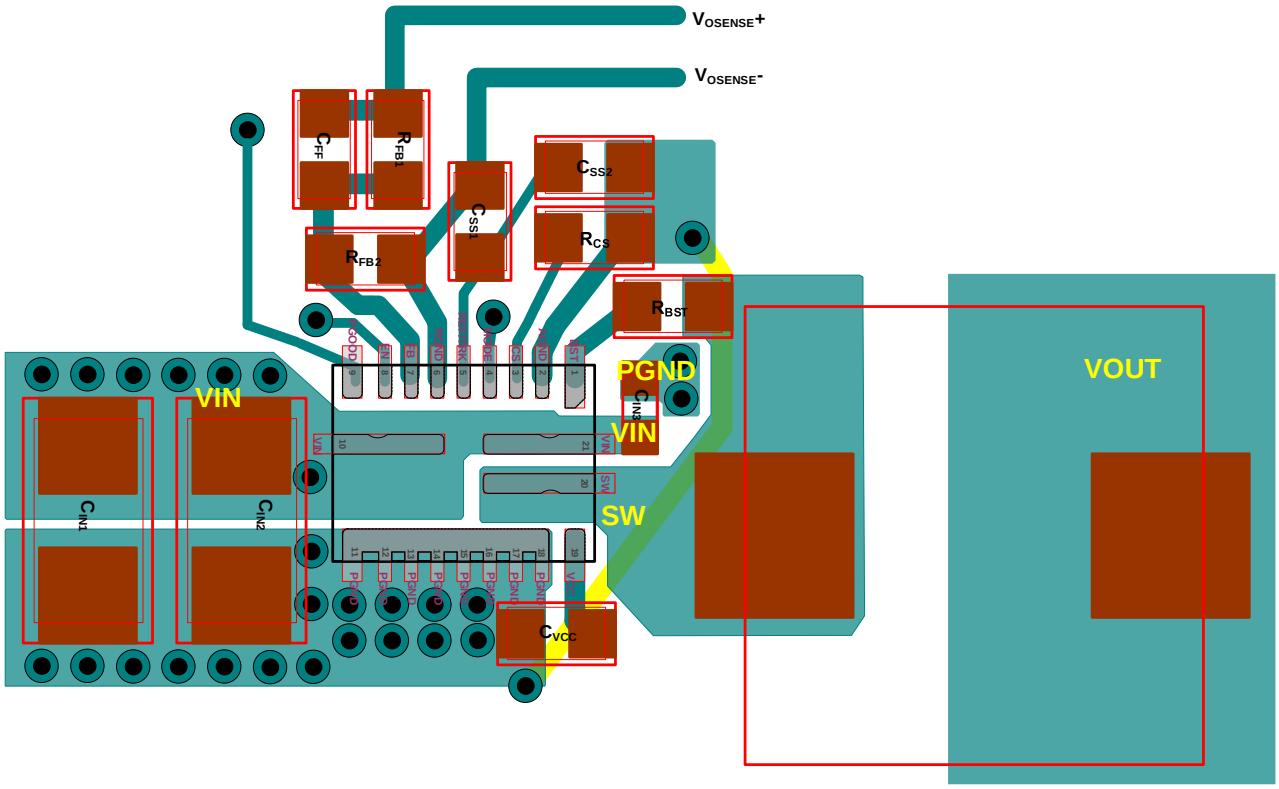
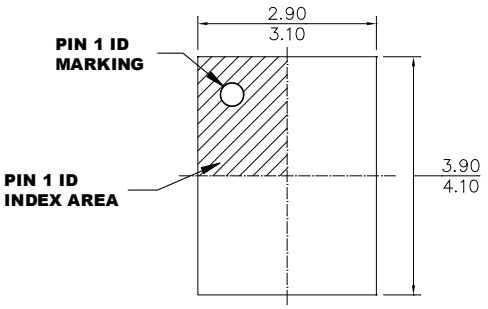


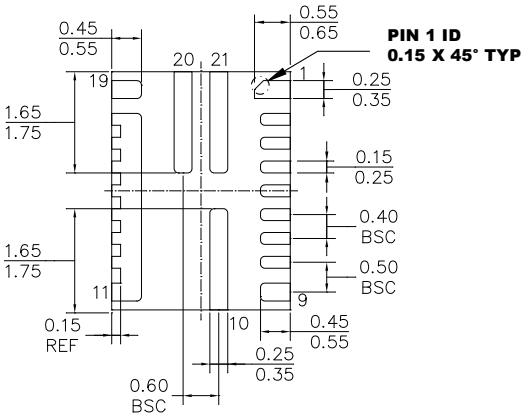
Figure 6: Recommended PCB Layout

PACKAGE INFORMATION

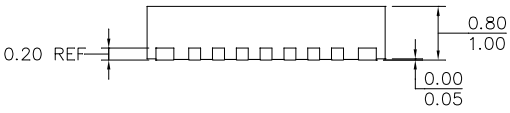
QFN-21 (3mmx4mm)



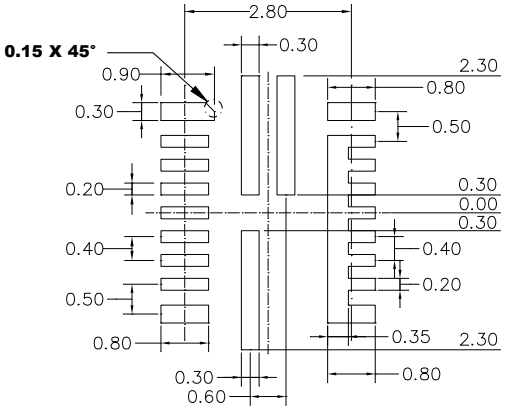
TOP VIEW



BOTTOM VIEW



SIDE VIEW

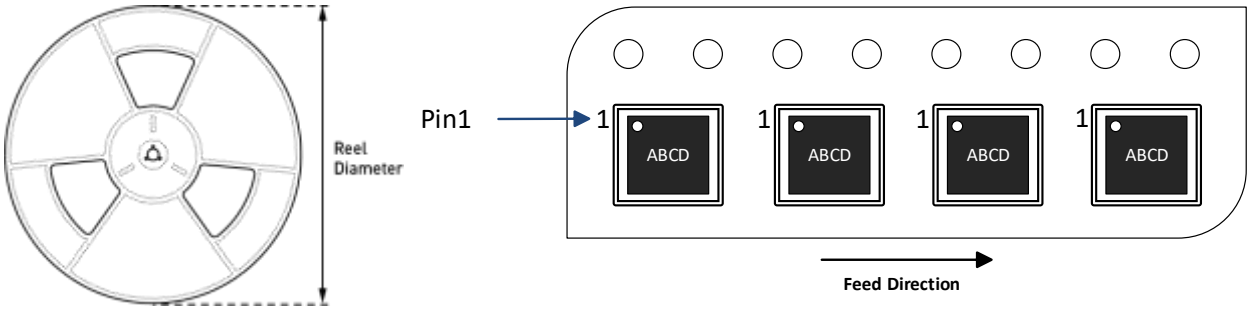


RECOMMENDED LAND PATTERN

NOTE:

1) THE LAND PATTERNS OF PINS 1, 9, 10, 11, 19, 20, AND 21 ARE THE SAME WIDTH.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
4) LEAD COPLANARITIES SHALL BE 0.1 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ8633B-HGLE-Z	QFN-21 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	2/25/2022	Initial Release	-