GigaDevice Semiconductor Inc.

GD32W515xx
Arm® Cortex®-M33 32-bit MCU

Datasheet

Revision 1.2

(Dec. 2022)

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1. General description

The GD32W515xx is a highly integrated 2.4GHz Wi-Fi System-on-Chip (SoC) that includes an ARM Cortex®-M33 processor with Trustzone, a single stream IEEE 802.11b/g/n MAC/baseband/radio, a power amplifier (PA), and a receive low-noise amplifier (LNA). It is an optimized SoC designed for a broad array of smart devices for Internet of Things (IoT) applications. The Cortex®-M33 processor is a 32-bit processor that possesses low interrupt latency and low-cost debug. The Cortex®-M33 processor is a 32-bit processor that possesses low interrupt latency and low-cost debug. The characteristics of integrated and advanced make the Cortex®-M33 processor suitable for market products that require microcontrollers with high performance and low power consumption. The Cortex®-M33 processor is based on the ARMv8 architecture and supports a powerful and scalable instruction set including general data processing I/O control tasks, advanced data processing bit field manipulations and DSP.

The GD32W515xx device incorporates the Arm® Cortex®-M33 32-bit processor core operating at up to 180 MHz frequency to obtain maximum efficiency. It provides up to 2048 KB on-chip Flash memory or support up to 32MB of EXT Flash memory and up to 448 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer a 12-bit ADC, up to four general 16-bit timers, two general 32-bit timers, one basic timer, one PWM advanced timer, as well as standard and advanced communication interfaces: up to two SPIs, a SQPI, a SDIO, two I2Cs, three USARTs, one I2S, an USBFS and a Wi-Fi. Additional peripherals as TrustZone protection controller union (TZPCU), digital camera interface (DCI), touch sensing interface (TSI), high-performance digital filter (HPDF), quad-SPI interface (QSPI) are included.

The device operates from a 1.62 to 3.63 V power supply and available in –40 to +85 °C temperature range. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make the GD32W515xx devices suitable for a wide range of applications, especially in areas such as industrial control, motor drives, user interface, power monitor and alarm systems, consumer and handheld equipment, gaming and GPS, E-bike, optical module and so on.

2. Device overview

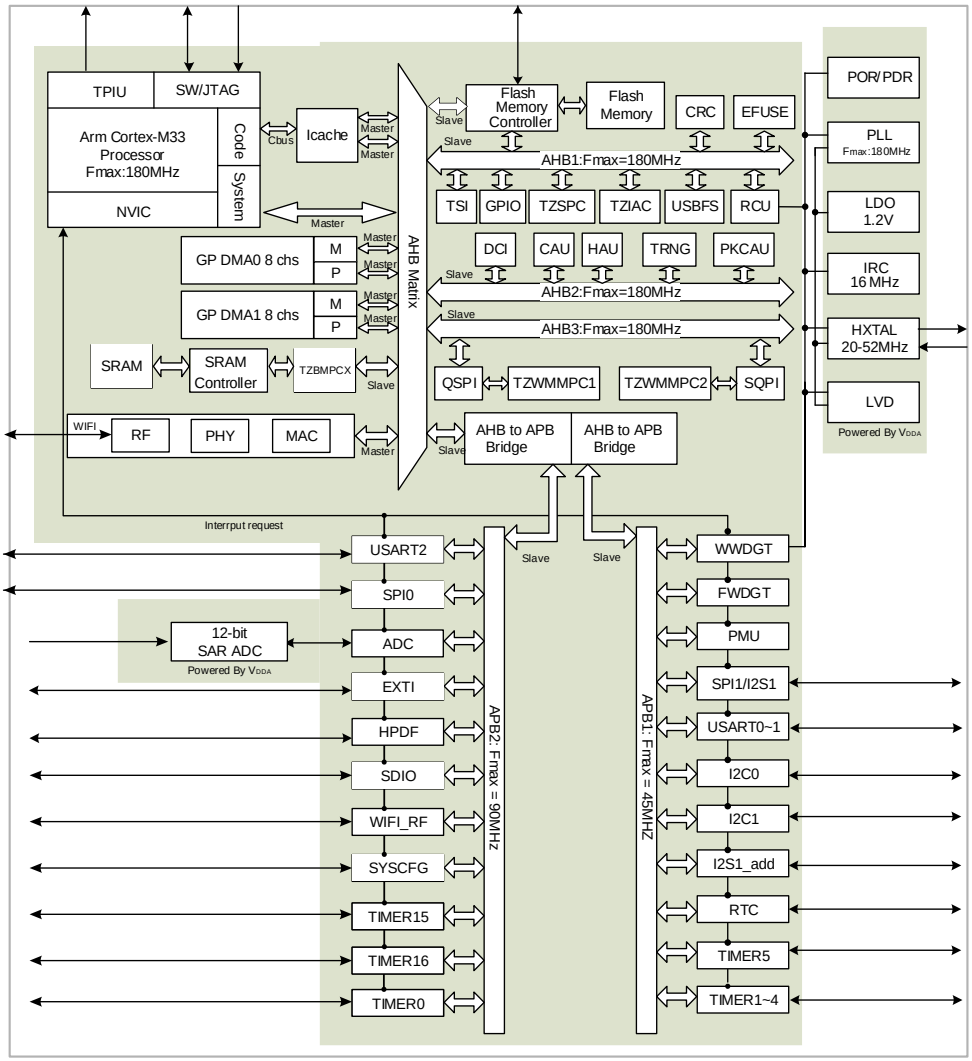
2.1. Device information

Table 2-1. GD32W515xx devices features and peripheral list

Part Number		GD32W515xx			
		PI	P0	TI	TG
FLASH (KB)		2048	0	2048	1024
SRAM (KB)		448	448	448	384
Timers	General timer(16-bit)	4 (3-4,15-16)	4 (3-4,15-16)	3 (4,15-16)	3 (4,15-16)
	General timer(32-bit)	2 (1-2)	2 (1-2)	2 (1-2)	2 (1-2)
	Advanced timer(16-bit)	1 (0)	1 (0)	1 (0)	1 (0)
	SysTick	1	1	1	1
	Basic timer(16-bit)	1 (5)	1 (5)	1 (5)	1 (5)
	Watchdog	2	2	2	2
	RTC	1	1	1	1
Connectivity	USART	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)
	I2C	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)
	SPI/I2S	2/1 (0-1)/(1)	2/1 (0-1)/(1)	2/1 (0-1)/(1)	2/1 (0-1)/(1)
	SDIO	1	1	1	1
	QSPI	1	1	1	1
	SQPI	1	1	1	1
	USBFS	1	1	1	1
	Wi-Fi	1	1	1	1
GPIO		43	43	25	25
HPDF		1	1	0	0
DCI		1	1	0	0
TSI (Channels)		12	12	7	7
TZGPC		1	1	1	1
ADC	Units	1	1	1	1
	Channels	9	9	5	5
Package		QFN56		QFN36	

2.2. Block diagram

Figure 2-1. GD32W515xx block diagram



2.3. Pinouts and pin assignment

Figure 2-2. GD32W515Px QFN56 pinouts

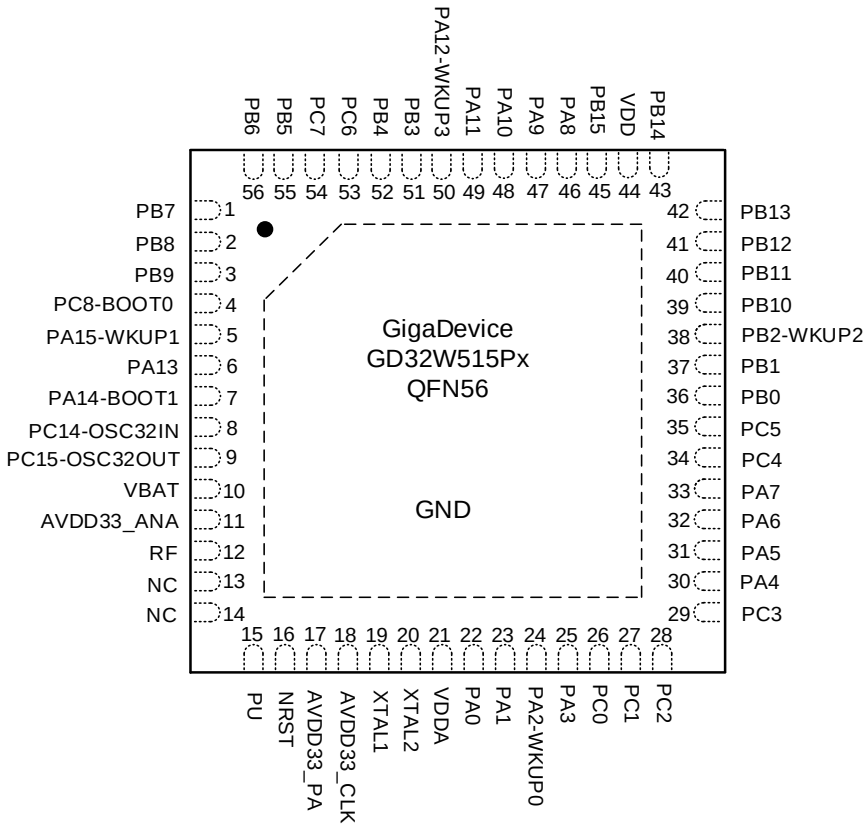
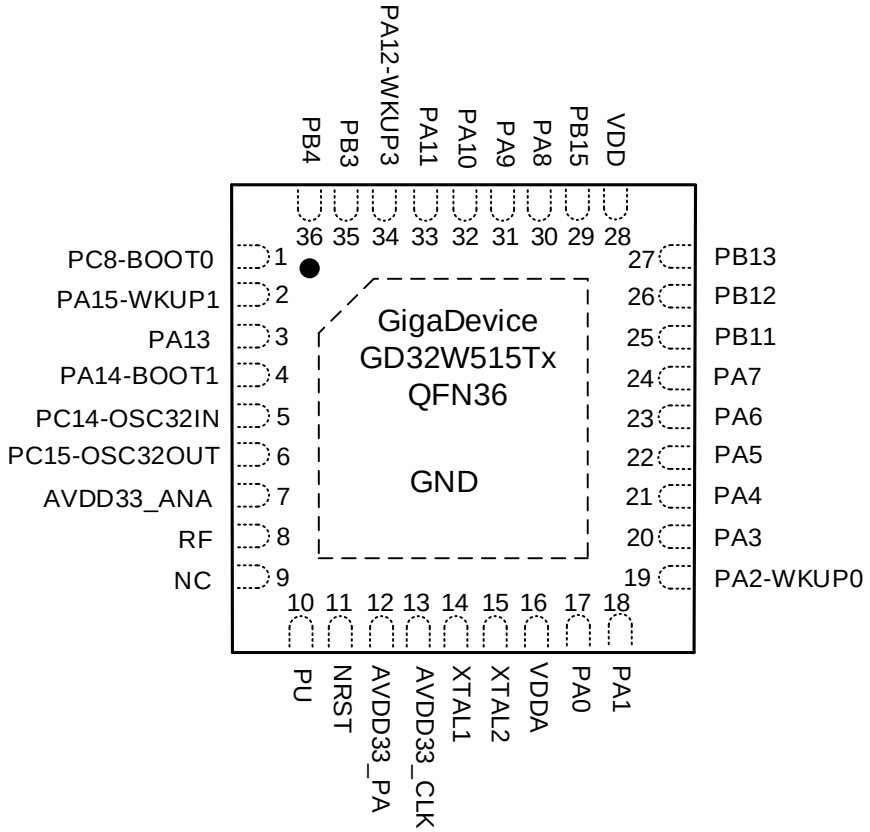


Figure 2-3. GD32W515Tx QFN36 pinouts



2.4. Memory map

Table 2-2. GD32W515xx memory map

Pre-defined Regions	Bus	Secure boundary address	Non-Secure boundary address	Peripherals
	-	-	0xE000 1000 - 0xE00F FFFF	Cortex M33 internal peripherals
External device	AHB3	-	0x9800 0000 - 0xDFFF FFFF	Reserved
		-	0x9000 0000 - 0x97FF FFFF	QSPI_FLASH(MEM)
		-	0x6800 0000 - 0x8FFF FFFF	Reserved
		-	0x6000 0000 - 0x67FF FFFF	SQPI_PSRAM(MEM)
Peripheral	AHB2	0x5C06 3000 - 0x5FFF FFFF	0x4C06 3000 - 0x4FFF FFFF	Reserved
		0x5C06 1000 - 0x5C06 2FFF	0x4C06 1000 - 0x4C06 2FFF	PKCAU
		0x5C06 0C00 - 0x5C06 0FFF	0x4C06 0C00 - 0x4C06 0FFF	Reserved
		0x5C06 0800 - 0x5C06 0BFF	0x4C06 0800 - 0x4C06 0BFF	TRNG
		0x5C06 0400 - 0x5C06 07FF	0x4C06 0400 - 0x4C06 07FF	HAU
		0x5C06 0000 - 0x5C06 03FF	0x4C06 0000 - 0x4C06 03FF	CAU
		0x5C05 0400 - 0x5C05 FFFF	0x4C05 0400 - 0x4C05 FFFF	Reserved
		0x5C05 0000 - 0x5C05 03FF	0x4C05 0000 - 0x4C05 03FF	DCI
		0x5C04 0000 - 0x5C04 FFFF	0x4C04 0000 - 0x4C04 FFFF	Reserved
		0x5C00 0000 - 0x5C03 FFFF	0x4C00 0000 - 0x4C03 FFFF	Reserved
	AHB1	0x5904 0000 - 0x5BFF FFFF	0x4904 0000 - 0x4BFF FFFF	Reserved
		0x5900 0000 - 0x5903 FFFF	0x4900 0000 - 0x4903 FFFF	USBFS
		0x500B 1000 - 0x58FF FFFF	0x400B 1000 - 0x48FF FFFF	Reserved
		0x500B 0800 - 0x500B 0FFF	0x400B 0800 - 0x400B 0FFF	Reserved
		0x500B 0400 - 0x500B 07FF	0x400B 0400 - 0x400B 07FF	TZBMPC3
		0x500B 0000 - 0x500B 03FF	0x400B 0000 - 0x400B 03FF	TZBMPC2
		0x500A 1000 - 0x500A FFFF	0x400A 1000 - 0x400A FFFF	Reserved
		0x500A 0C00 - 0x500A 0FFF	0x400A 0C00 - 0x400A 0FFF	TZBMPC1
		0x500A 0800 - 0x500A 0BFF	0x400A 0800 - 0x400A 0BFF	TZBMPC0
		0x500A 0400 - 0x500A 07FF	0x400A 0400 - 0x400A 07FF	TZIAC
		0x500A 0000 - 0x500A 03FF	0x400A 0000 - 0x400A 03FF	TZSPC
		0x5008 0400 - 0x5009 FFFF	0x4008 0400 - 0x4009 FFFF	Reserved
		0x5008 0000 - 0x5008 03FF	0x4008 0000 - 0x4008 03FF	ICACHE
		0x5003 3000 - 0x5007 FFFF	0x4003 3000 - 0x4007 FFFF	Reserved
		0x5003 0000 - 0x5003 2FFF	0x4003 0000 - 0x4003 2FFF	Wi-Fi
		0x5002 BC00 - 0x5002 FFFF	0x4002 BC00 - 0x4002 FFFF	Reserved
		0x5002 B000 - 0x5002 BBFF	0x4002 B000 - 0x4002 BBFF	Reserved
		0x5002 A000 - 0x5002 AFFF	0x4002 A000 - 0x4002 AFFF	Reserved
		0x5002 8000 - 0x5002 9FFF	0x4002 8000 - 0x4002 9FFF	Reserved
		0x5002 6800 - 0x5002 7FFF	0x4002 6800 - 0x4002 7FFF	Reserved
		0x5002 6400 - 0x5002 67FF	0x4002 6400 - 0x4002 67FF	DMA1
		0x5002 6000 - 0x5002 63FF	0x4002 6000 - 0x4002 63FF	DMA0

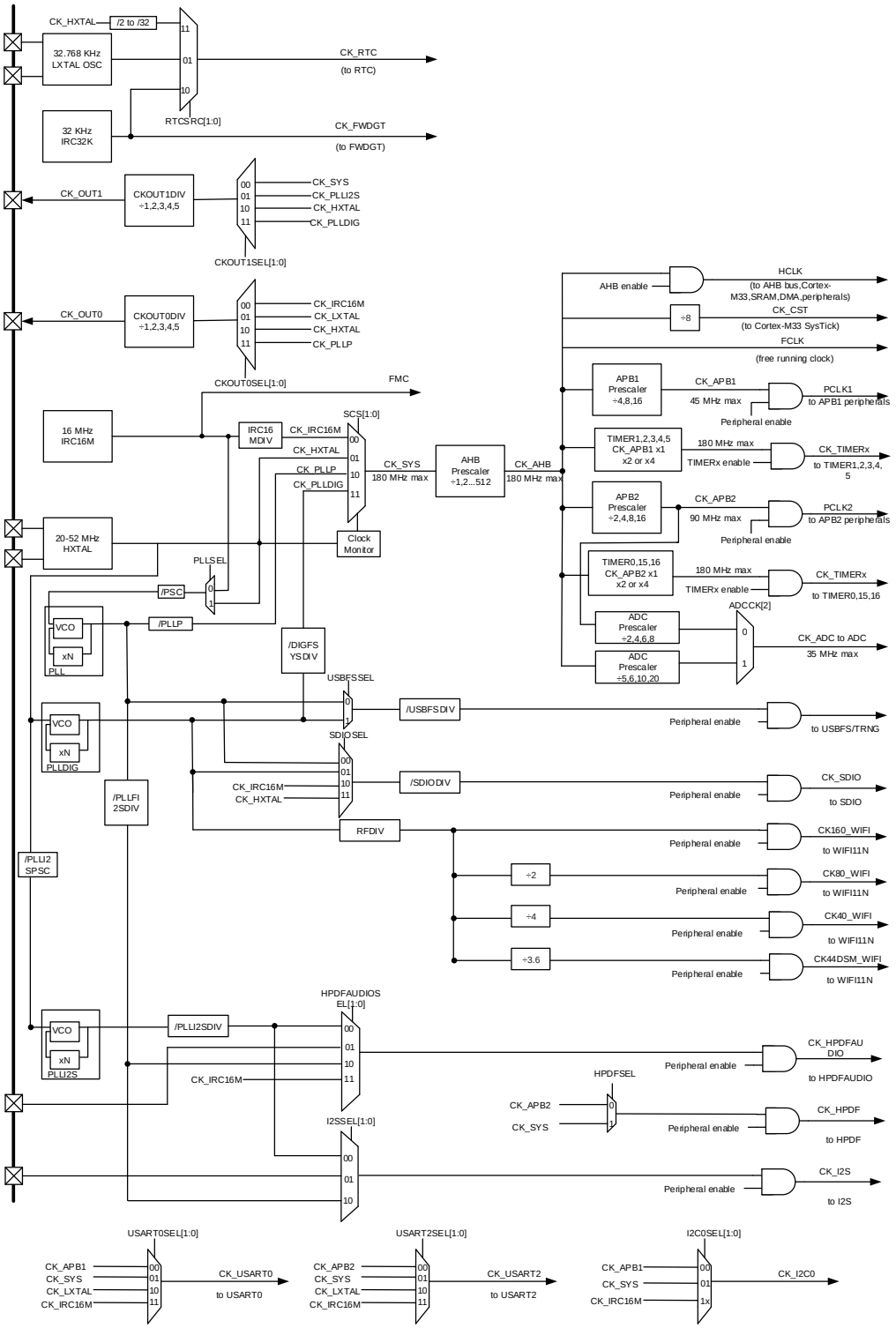
Pre-defined Regions	Bus	Secure boundary address	Non-Secure boundary address	Peripherals
		0x5002 5C00 - 0x5002 5FFF	0x4002 5C00 - 0x4002 5FFF	Reserved
		0x5002 5800 - 0x5002 5BFF	0x4002 5800 - 0x4002 5BFF	QSPI_FLASH(REG)
		0x5002 5400 - 0x5002 57FF	0x4002 5400 - 0x4002 57FF	SQPI_PSRAM(REG)
		0x5002 5000 - 0x5002 53FF	0x4002 5000 - 0x4002 53FF	Reserved
		0x5002 4000 - 0x5002 4FFF	0x4002 4000 - 0x4002 4FFF	TSI
		0x5002 3C00 - 0x5002 3FFF	0x4002 3C00 - 0x4002 3FFF	Reserved
		0x5002 3800 - 0x5002 3BFF	0x4002 3800 - 0x4002 3BFF	RCU
		0x5002 3400 - 0x5002 37FF	0x4002 3400 - 0x4002 37FF	Reserved
		0x5002 3000 - 0x5002 33FF	0x4002 3000 - 0x4002 33FF	CRC
		0x5002 2C00 - 0x5002 2FFF	0x4002 2C00 - 0x4002 2FFF	Reserved
		0x5002 2800 - 0x5002 2BFF	0x4002 2800 - 0x4002 2BFF	EFUSE
		0x5002 2400 - 0x5002 27FF	0x4002 2400 - 0x4002 27FF	Reserved
		0x5002 2000 - 0x5002 23FF	0x4002 2000 - 0x4002 23FF	FMC
		0x5002 1C00 - 0x5002 1FFF	0x4002 1C00 - 0x4002 1FFF	Reserved
		0x5002 1800 - 0x5002 1BFF	0x4002 1800 - 0x4002 1BFF	Reserved
		0x5002 1400 - 0x5002 17FF	0x4002 1400 - 0x4002 17FF	Reserved
		0x5002 1000 - 0x5002 13FF	0x4002 1000 - 0x4002 13FF	Reserved
		0x5002 0C00 - 0x5002 0FFF	0x4002 0C00 - 0x4002 0FFF	Reserved
		0x5002 0800 - 0x5002 0BFF	0x4002 0800 - 0x4002 0BFF	GPIOC
		0x5002 0400 - 0x5002 07FF	0x4002 0400 - 0x4002 07FF	GPIOB
		0x5002 0000 - 0x5002 03FF	0x4002 0000 - 0x4002 03FF	GPIOA
	APB2	0x5001 8800 - 0x5001 FFFF	0x4001 8800 - 0x4001 FFFF	Reserved
		0x5001 8400 - 0x5001 87FF	0x4001 8400 - 0x4001 87FF	TIMER16
		0x5001 8000 - 0x5001 83FF	0x4001 8000 - 0x4001 83FF	TIMER15
		0x5001 7C00 - 0x5001 7FFF	0x4001 7C00 - 0x4001 7FFF	Reserved
		0x5001 7800 - 0x5001 7BFF	0x4001 7800 - 0x4001 7BFF	Wi-Fi_RF
		0x5001 6800 - 0x5001 77FF	0x4001 6800 - 0x4001 77FF	Reserved
		0x5001 6000 - 0x5001 67FF	0x4001 6000 - 0x4001 67FF	HPDF
		0x5001 5800 - 0x5001 5FFF	0x4001 5800 - 0x4001 5FFF	Reserved
		0x5001 5400 - 0x5001 57FF	0x4001 5400 - 0x4001 57FF	Reserved
		0x5001 4C00 - 0x5001 53FF	0x4001 4C00 - 0x4001 53FF	Reserved
		0x5001 4800 - 0x5001 4BFF	0x4001 4800 - 0x4001 4BFF	Reserved
		0x5001 4400 - 0x5001 47FF	0x4001 4400 - 0x4001 47FF	Reserved
		0x5001 4000 - 0x5001 43FF	0x4001 4000 - 0x4001 43FF	Reserved
		0x5001 3C00 - 0x5001 3FFF	0x4001 3C00 - 0x4001 3FFF	EXTI
		0x5001 3800 - 0x5001 3BFF	0x4001 3800 - 0x4001 3BFF	SYSCFG
		0x5001 3400 - 0x5001 37FF	0x4001 3400 - 0x4001 37FF	Reserved
		0x5001 3000 - 0x5001 33FF	0x4001 3000 - 0x4001 33FF	SPI0
		0x5001 2C00 - 0x5001 2FFF	0x4001 2C00 - 0x4001 2FFF	SDIO
		0x5001 2400 - 0x5001 2BFF	0x4001 2400 - 0x4001 2BFF	Reserved

Pre-defined Regions	Bus	Secure boundary address	Non-Secure boundary address	Peripherals
		0x5001 2000 - 0x5001 23FF	0x4001 2000 - 0x4001 23FF	ADC
		0x5001 1400 - 0x5001 1FFF	0x4001 1400 - 0x4001 1FFF	Reserved
		0x5001 1000 - 0x5001 13FF	0x4001 1000 - 0x4001 13FF	USART2
		0x5001 0800 - 0x5001 0FFF	0x4001 0800 - 0x4001 0FFF	Reserved
		0x5001 0400 - 0x5001 07FF	0x4001 0400 - 0x4001 07FF	Reserved
		0x5001 0000 - 0x5001 03FF	0x4001 0000 - 0x4001 03FF	TIMER0
	APB1	0x5000 7400 - 0x5000 FFFF	0x4000 D000 - 0x4000 FFFF	Reserved
		0x5000 CC00 - 0x5000 CFFF	0x4000 CC00 - 0x4000 CFFF	Reserved
		0x5000 7400 - 0x5000 CBFF	0x4000 7400 - 0x4000 CBFF	Reserved
		0x5000 7000 - 0x5000 73FF	0x4000 7000 - 0x4000 73FF	PMU
		0x5000 6C00 - 0x5000 6FFF	0x4000 6C00 - 0x4000 6FFF	Reserved
		0x5000 5C00 - 0x5000 6BFF	0x4000 5C00 - 0x4000 6BFF	Reserved
		0x5000 5800 - 0x5000 5BFF	0x4000 5800 - 0x4000 5BFF	I2C1
		0x5000 5400 - 0x5000 57FF	0x4000 5400 - 0x4000 57FF	I2C0
		0x5000 4C00 - 0x5000 53FF	0x4000 4C00 - 0x4000 53FF	Reserved
		0x5000 4800 - 0x5000 4BFF	0x4000 4800 - 0x4000 4BFF	USART0
		0x5000 4400 - 0x5000 47FF	0x4000 4400 - 0x4000 47FF	USART1
		0x5000 4000 - 0x5000 43FF	0x4000 4000 - 0x4000 43FF	Reserved
		0x5000 3C00 - 0x5000 3FFF	0x4000 3C00 - 0x4000 3FFF	Reserved
		0x5000 3800 - 0x5000 3BFF	0x4000 3800 - 0x4000 3BFF	SPI1/I2S1
		0x5000 3400 - 0x5000 37FF	0x4000 3400 - 0x4000 37FF	I2S1_add
		0x5000 3000 - 0x5000 33FF	0x4000 3000 - 0x4000 33FF	FWDGT
		0x5000 2C00 - 0x5000 2FFF	0x4000 2C00 - 0x4000 2FFF	WWDGT
		0x5000 2800 - 0x5000 2BFF	0x4000 2800 - 0x4000 2BFF	RTC
		0x5000 2400 - 0x5000 27FF	0x4000 2400 - 0x4000 27FF	Reserved
		0x5000 2000 - 0x5000 23FF	0x4000 2000 - 0x4000 23FF	Reserved
		0x5000 1C00 - 0x5000 1FFF	0x4000 1C00 - 0x4000 1FFF	Reserved
		0x5000 1800 - 0x5000 1BFF	0x4000 1800 - 0x4000 1BFF	Reserved
		0x5000 1400 - 0x5000 17FF	0x4000 1400 - 0x4000 17FF	Reserved
		0x5000 1000 - 0x5000 13FF	0x4000 1000 - 0x4000 13FF	TIMER5
		0x5000 0C00 - 0x5000 0FFF	0x4000 0C00 - 0x4000 0FFF	TIMER4
		0x5000 0800 - 0x5000 0BFF	0x4000 0800 - 0x4000 0BFF	TIMER3
		0x5000 0400 - 0x5000 07FF	0x4000 0400 - 0x4000 07FF	TIMER2
		0x5000 0000 - 0x5000 03FF	0x4000 0000 - 0x4000 03FF	TIMER1
SRAM	AHB	0x3007 0000 - 0x3FFF FFFF	0x2007 0000 - 0x2FFF FFFF	Reserved
		0x3004 0000 - 0x2006 FFFF	0x2004 0000 - 0x2006 FFFF	SRAM3 (192KB)
		0x3002 0000 - 0x3003 FFFF	0x2002 0000 - 0x2003 FFFF	SRAM2 (128KB)
		0x3001 0000 - 0x3001 FFFF	0x2001 0000 - 0x2001 FFFF	SRAM1 (64KB)
		0x3000 0000 - 0x3000 FFFF	0x2000 0000 - 0x2000 FFFF	SRAM0 (64KB)
Code	AHB	-	0x1000 0000 - 0x1FFF FFFF	External memories remap

Pre-defined Regions	Bus	Secure boundary address	Non-Secure boundary address	Peripherals
		-	0x0BFF 8000 - 0x0BFF FFFF	Reserved
		0x0FF8 8000 - 0x0FFF FFFF	0x0BF8 0000 – 0x0BFF 7FFF	Reserved
		0x0FF8 4000 – 0x0FF8 7FFF	-	ROM(16KB)
		0x0FF8 0000 – 0x0FF8 3FFF	-	GSSA(16KB)
		0x0FF4 E000 – 0x0FF7 FFFF	0x0BF4 E000 – 0x0BF7 FFFF	ROM(200KB)
		-	0x0BF4 6000 – 0x0BF4 CFFF	Reserved
		-	0x0BF4 0000 - 0x0BF4 5FFF	ROM(24KB)
		0x0E07 0000 - 0x0FF4 DFFF	0x0A07 0000 - 0x0BF3 FFFF	Reserved
		0x0E04 0000 - 0x0E06 FFFF	0x0A04 0000 - 0x0A06 FFFF	SRAM3 (192KB)
		0x0E02 0000 - 0x0E03 FFFF	0x0A02 0000 - 0x0A03 FFFF	SRAM2 (128KB)
		0x0E01 0000 - 0x0E01 FFFF	0x0A01 0000 - 0x0A01 FFFF	SRAM1 (64KB)
		0x0E00 0000 - 0x0E00 FFFF	0x0A00 0000 - 0x0A00 FFFF	SRAM0 (64KB)
		0x0C20 0000 - 0x0DFF FFFF	0x0820 0000 - 0x09FF FFFF	Reserved
		0x0C00 0000 - 0x0C1F FFFF	0x0800 0000 - 0x081F FFFF	Flash memory
		-	0x0000 0000 - 0x07FF FFFF	External memories remap

2.5. Clock tree

Figure 2-4. GD32W515xx clock tree



Legend:

HXTAL: High speed crystal oscillator

LXTAL: Low speed crystal oscillator

IRC16M: Internal 16M RC oscillator

IRC32K: Internal 32K RC oscillator

2.6. Pin definitions

2.6.1. GD32W515Px QFN56 pin definitions

Table 2-3. GD32W515Px QFN56 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PB7	1	I/O	5VT	Default: PB7 Alternate: I2S1_WS, SPI1_NSS, EVENTOUT, TIMER3_CH1, I2C0_SDA, USART0_RX, DCI_VSYNC
PB8	2	I/O	5VT	Default: PB8 Alternate: SPI1_SCK, I2S1_CK, EVENTOUT, TIMER3_CH2, SDIO_D4, DCI_D6
PB9	3	I/O	5VT	Default: PB9 Alternate: I2S1_SD, SPI1_MOSI, EVENTOUT, TIMER1_CH1, TIMER3_CH3, SDIO_D5, DCI_D7
PC8-BOOT0	4	I/O	5VT	Default: PC8 Alternate: I2C0_SDA, USART0_TX, I2C1_SDA, EVENTOUT, TIMER2_CH2, SDIO_D0, DCI_D2 Additional: BOOT0
PA15-WKUP1	5	I/O	5VT	Default: JTDI, PA15 Alternate: I2C0_SCL, USART0_RX, I2C1_SCL, EVENTOUT, SPI0_NSS Additional: WKUP1
PA13	6	I/O	5VT	Default: JTMS, SWDIO, PA13 Alternate: USART0_CTS, USART1_CTS, I2C0_SMBA, EVENTOUT, TSITG
PA14-BOOT1	7	I/O	5VT	Default: JTCK, SWCLK, PA14 Alternate: USART0_RTS / USART0_DE, USART1_RTS / USART1_DE, I2C1_SMBA, EVENTOUT Additional: BOOT1
PC14-OSC32IN	8	I/O	5VT	Default: PC14 Alternate: USART0_CK, USART1_CK, EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	9	I/O	5VT	Default: PC15 Alternate: IFRP_OUT, EVENTOUT Additional: RTC_TAMP0, RTC_OUT, RTC_TS, OSC32OUT
VBAT	10	P		Default: VBAT
AVDD33_ANA	11	P		Default: AVDD33_ANA
RF	12	AI/AO		Default: RF

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
NC	13			-
NC	14			-
PU	15	I		Default: PU
NRST	16	I/O		Default: NRST
AVDD33_PA	17	P		Default: AVDD33_PA
AVDD33_CLK	18	P		Default: AVDD33_CLK
XTAL1	19	AI		Default: XTAL1
XTAL2	20	AO		Default: XTAL2
VDDA	21	P		Default: VDDA
PA0	22	I/O	5VT	Default: PA0 Alternate: USART0_TX, TSI_G0_IO0, USART1_CTS, EVENTOUT, TIMER1_CH0, TIMER1_ETI, TIMER4_CH0 Additional: ADC_IN0
PA1	23	I/O	5VT	Default: PA1 Alternate: USART0_RX, TSI_G0_IO1, USART1_RTS / USART1_DE, EVENTOUT, TIMER1_CH1, TIMER4_CH1 Additional: ADC_IN1
PA2-WKUP0	24	I/O	5VT	Default: PA2 Alternate: USART0_CK, TSI_G0_IO2, TIMER0_CH0, EVENTOUT, TIMER1_CH2, TIMER4_CH2, I2S1_CKIN, USART1_TX, HPDF_AUDIO Additional: ADC_IN2, WKUP0, RTC_TAMP1
PA3	25	I/O	5VT	Default: PA3 Alternate: USART1_CK, TSI_G0_IO3, TIMER0_CH0_ON, HPDF_DATAIN1, EVENTOUT, TIMER1_CH3, TIMER4_CH3, I2S1_MCK, USART1_RX, RTC_OUT Additional: ADC_IN3
PC0	26	I/O	5VT	Default: PC0 Alternate: USART1_TX, TIMER0_CH3, I2C0_SMBA, HPDF_CKIN0, EVENTOUT, DCI_D4 Additional: ADC_IN4
PC1	27	I/O	5VT	Default: PC1 Alternate: I2S1_SD, USART1_RX, DCI_HSYNC, TIMER0_BRKIN, I2C1_SMBA, HPDF_CKIN1, EVENTOUT, SPI1_MOSI, DCI_D8 Additional: ADC_IN5
PC2	28	I/O	5VT	Default: PC2 Alternate: HPDF_CKOUT, I2C1_SDA, I2C0_SCL,

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				TIMER4_CH0, TIMER0_CH0, DCI_VSYNC, TIMER0_ETI, EVENTOUT, SPI1_MISO, I2S1_ADD_SD, DCI_D9 Additional: ADC_IN6
PC3	29	I/O	5VT	Default: PC3 Alternate: I2S1_SD, HPDF_DATAIN0, I2C1_SCL, I2C0_SDA, TIMER4_CH1, TIMER0_CH0_ON, DCI_PIXCLK, TIMER1_CH0, TIMER1_ETI, EVENTOUT, SPI1_MOSI, DCI_D11 Additional: ADC_IN7
PA4	30	I/O	5VT	Default: PA4 Alternate: I2S1_ADD_SD, SPI1_MOSI, I2S1_SD, SPI0_MOSI, QSPI_SCK, TIMER4_CH2, DCI_HSYNC, USART1_TX, TIMER0_CH1, EVENTOUT, SPI0_NSS, USART1_CK Additional: ADC_IN8
PA5	31	I/O	5VT	Default: PA5 Alternate: I2S1_MCK, SPI0_MISO, QSPI_CSN, TIMER4_CH3, DCI_VSYNC, USART1_RX, TIMER0_CH1_ON, EVENTOUT, SPI0_SCK
PA6	32	I/O	5VT	Default: PA6 Alternate: I2S1_CKIN, SPI0_SCK, QSPI_IO0, TIMER2_CH0, DCI_PIXCLK, USART2_TX, TIMER0_CH1, TIMER1_CH1, EVENTOUT, SPI0_MISO, I2S1_MCK, SDIO_CMD, HPDF_AUDIO
PA7	33	I/O	5VT	Default: PA7 Alternate: SPI1_NSS, I2S1_WS, SPI0_NSS, QSPI_IO1, TIMER2_CH1, DCI_D7, USART2_RX, TIMER0_CH1_ON, TIMER1_CH2, EVENTOUT, TIMER0_CH0_ON, SPI0_MOSI
PC4	34	I/O	5VT	Default: PC4 Alternate: I2S1_ADD_SD, SPI0_IO2, QSPI_IO2, TIMER2_CH2, DCI_D6, EVENTOUT, SQPI_CLK, DCI_D12
PC5	35	I/O	5VT	Default: PC5 Alternate: CK_OUT1, SPI0_IO3, QSPI_IO3, TIMER2_CH3, TIMER2_CH0, DCI_D5, DCI_D7, EVENTOUT, USART2_RX, SQPI_CSN, DCI_D13
PB0	36	I/O	5VT	Default: PB0 Alternate: TSI_G1_IO0, TIMER3_CH0, TIMER2_CH1, DCI_D4, DCI_D6, EVENTOUT, TIMER0_CH1_ON,

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				SDIO_D1
PB1	37	I/O	5VT	Default: PB1 Alternate: TSI_G1_IO1, TIMER3_CH1, TIMER2_CH2, DCI_D3, DCI_D5, EVENTOUT, TIMER0_CH2_ON, SDIO_D2
PB2-WKUP2	38	I/O	5VT	Default: PB2 Alternate: TSI_G1_IO2, TIMER3_CH2, TIMER2_CH3, DCI_D2, DCI_D4, EVENTOUT, TIMER1_CH3, SDIO_CK Additional: WKUP2
PB10	39	I/O	5VT	Default: PB10 Alternate: TSI_G1_IO3, TIMER3_CH3, TIMER0_CH1, DCI_D1, DCI_D3, IFRP_OUT, EVENTOUT, TIMER1_CH2, TIMER3_ETI, USART2_TX, SDIO_D7
PB11	40	I/O	5VT	Default: PB11 Alternate: USBFS_ID, TSI_G2_IO0, TIMER0_CH1_ON, DCI_D0, DCI_D2, EVENTOUT, I2S1_CKIN, USART2_RX, SDIO_D6
PB12	41	I/O	5VT	Default: PB12 Alternate: I2S1_WS, USBFS_DP, TSI_G2_IO1, DCI_D1, TIMER0_CH3, EVENTOUT, TIMER0_BRKIN, SPI1_NSS, USART2_CK
PB13	42	I/O	5VT	Default: PB13 Alternate: USBFS_DM, TSI_G2_IO2, DCI_D0, EVENTOUT, TIMER15_CH0, TIMER0_CH0_ON, SPI1_SCK, I2S1_CK, USART2_CTS
PB14	43	I/O	5VT	Default: PB14 Alternate: TSI_G2_IO3, EVENTOUT, TIMER15_BRKIN, TIMER0_CH1_ON, SPI1_MISO, I2S1_ADD_SD, USART2_RTS / USART2_DE Additional: USBFS_VBUS
VDD	44	P		Default: VDD
PB15	45	I/O	5VT	Default: PB15 Alternate: I2S1_SD, USART1_TX, USART0_TX, I2C0_SCL, I2C1_SCL, IFRP_OUT, EVENTOUT, RTC_REFIN, TIMER0_CH2_ON, SPI1_MOSI
PA8	46	I/O	5VT	Default: PA8 Alternate: CK_OUT0, USART1_RX, USART0_RX, I2C0_SDA, I2C1_SDA, EVENTOUT, TIMER15_CH0, TIMER0_CH0, USART0_CK, USBFS_SOF, SDIO_D1, RTC_OUT
PA9	47	I/O	5VT	Default: PA9 Alternate: SPI0_MOSI, SDIO_CMD, SQPI_CLK,

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				QSPI_SCK, EVENTOUT, TIMER15_CH0_ON, TIMER0_CH1, SPI1_SCK, I2S1_CK, USART0_TX, SDIO_D2, DCI_D0
PA10	48	I/O	5VT	Default: PA10 Alternate: SPI0_MISO, SDIO_D0, SQPI_CSN, QSPI_CSN, EVENTOUT, TIMER16_CH0, TIMER0_CH2, DCI_D1
PA11	49	I/O	5VT	Default: PA11 Alternate: SPI0_SCK, SDIO_CK, SQPI_D0, QSPI_IO0, EVENTOUT, TIMER16_BRKIN, TIMER0_CH3, DCI_D2
PA12-WKUP3	50	I/O	5VT	Default: PA12 Alternate: SPI0_NSS, SDIO_D1, SQPI_D1, QSPI_IO1, EVENTOUT, TIMER16_CH0_ON, TIMER0_ETI, USART0_RTS / USART0_DE, DCI_D3 Additional: WKUP3
PB3	51	I/O	5VT	Default: JTDO, TRACESWO, PB3 Alternate: USART2_CTS, SPI0_IO2, SDIO_D2, SQPI_D2, QSPI_IO2, EVENTOUT, TIMER15_BRKIN, TIMER1_CH1, SPI0_SCK, USART0_RX
PB4	52	I/O	5VT	Default: NJTRST, PB4 Alternate: USART2_RTS / USART2_DE, SPI0_IO3, SDIO_D3, SQPI_D3, QSPI_IO3, TIMER1_CH0, TIMER1_ETI, EVENTOUT, SPI0_MISO
PC6	53	I/O	5VT	Default: PC6 Alternate: USART2_TX, TIMER1_CH1, TIMER0_CH1, TIMER0_BRKIN, TRACECK, TIMER16_BRKIN, TIMER2_CH0, I2S1_MCK, SDIO_D6, DCI_D0
PC7	54	I/O	5VT	Default: PC7 Alternate: USART2_RX, TIMER1_CH2, TIMER0_CH1_ON, TIMER0_ETI, TIMER16_CH0, TIMER2_CH1, SPI1_SCK, I2S1_CK, SDIO_D7, DCI_D1
PB5	55	I/O	5VT	Default: PB5 Alternate: USART2_CK, TIMER1_CH3, IFRP_OUT, EVENTOUT, TSITG, SPI0_MOSI, DCI_D10
PB6	56	I/O	5VT	Default: PB6 Alternate: SPI1_MISO, EVENTOUT, DCI_D5

Note:

(1) Type: I = input, O = output, A = analog, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

2.6.2. GD32W515Tx QFN36 pin definitions

Table 2-4. GD32W515Tx QFN36 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PC8-BOOT0	1	I/O	5VT	Default: PC8 Alternate: I2C0_SDA, USART0_TX, I2C1_SDA, EVENTOUT, TIMER2_CH2, SDIO_D0 Additional: BOOT0
PA15-WKUP1	2	I/O	5VT	Default: JTDI, PA15 Alternate: I2C0_SCL, USART0_RX, I2C1_SCL, EVENTOUT, SPI0_NSS Additional: WKUP1
PA13	3	I/O	5VT	Default: JTMS, SWDIO, PA13 Alternate: USART0_CTS, USART1_CTS, I2C0_SMBA, EVENTOUT, TSITG
PA14-BOOT1	4	I/O	5VT	Default: JTCK, SWCLK, PA14 Alternate: USART0_RTS / USART0_DE, USART1_RTS / USART1_DE, I2C1_SMBA, EVENTOUT Additional: BOOT1
PC14-OSC32IN	5	I/O	5VT	Default: PC14 Alternate: USART0_CK, USART1_CK, EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	6	I/O	5VT	Default: PC15 Alternate: IFRP_OUT, EVENTOUT Additional: RTC_TAMP0, RTC_OUT, RTC_TS, OSC32OUT
AVDD33_ANA	7	P		Default: AVDD33_ANA
RF	8	AI/AO		Default: RF
NC	9			-
PU	10	I		Default: PU
NRST	11	I/O		Default: NRST
AVDD33_PA	12	P		Default: AVDD33_PA
AVDD33_CLK	13	P		Default: AVDD33_CLK
XTAL1	14	AI		Default: XTAL1
XTAL2	15	AO		Default: XTAL2
VDDA	16	P		Default: VDDA
PA0	17	I/O	5VT	Default: PA0 Alternate: USART0_TX, TSI_G0_IO0, USART1_CTS, EVENTOUT, TIMER1_CH0, TIMER1_ETI, TIMER4_CH0

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Additional: ADC_IN0
PA1	18	I/O	5VT	Default: PA1 Alternate: USART0_RX, TSI_G0_IO1, USART1_RTS / USART1_DE, EVENTOUT, TIMER1_CH1, TIMER4_CH1 Additional: ADC_IN1
PA2-WKUP0	19	I/O	5VT	Default: PA2 Alternate: USART0_CK, TSI_G0_IO2, TIMER0_CH0, EVENTOUT, TIMER1_CH2, TIMER4_CH2, I2S1_CKIN, USART1_TX Additional: ADC_IN2, WKUP0, RTC_TAMP1
PA3	20	I/O	5VT	Default: PA3 Alternate: USART1_CK, TSI_G0_IO3, TIMER0_CH0_ON, EVENTOUT, TIMER1_CH3, TIMER4_CH3, I2S1_MCK, USART1_RX, RTC_OUT Additional: ADC_IN3
PA4	21	I/O	5VT	Default: PA4 Alternate: I2S1_ADD_SD, SPI1_MOSI, I2S1_SD, SPI0_MOSI, QSPI_SCK, TIMER4_CH2, USART1_TX, TIMER0_CH1, EVENTOUT, SPI0_NSS, USART1_CK Additional: ADC_IN8
PA5	22	I/O	5VT	Default: PA5 Alternate: I2S1_MCK, SPI0_MISO, QSPI_CSN, TIMER4_CH3, USART1_RX, TIMER0_CH1_ON, EVENTOUT, SPI0_SCK
PA6	23	I/O	5VT	Default: PA6 Alternate: I2S1_CKIN, SPI0_SCK, QSPI_IO0, TIMER2_CH0, USART2_TX, TIMER0_CH1, TIMER1_CH1, EVENTOUT, SPI0_MISO, I2S1_MCK, SDIO_CMD
PA7	24	I/O	5VT	Default: PA7 Alternate: SPI1_NSS, I2S1_WS, SPI0_NSS, QSPI_IO1, TIMER2_CH1, USART2_RX, TIMER0_CH1_ON, TIMER1_CH2, EVENTOUT, TIMER0_CH0_ON, SPI0_MOSI
PB11	25	I/O	5VT	Default: PB11 Alternate: USBFS_ID, TSI_G2_IO0, TIMER0_CH1_ON, EVENTOUT, I2S1_CKIN, USART2_RX, SDIO_D6
PB12	26	I/O	5VT	Default: PB12 Alternate: I2S1_WS, USBFS_DP, TSI_G2_IO1, TIMER0_CH3, EVENTOUT, TIMER0_BRKIN, SPI1_NSS, USART2_CK
PB13	27	I/O	5VT	Default: PB13

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Alternate: USBFS_DM, TSI_G2_IO2, EVENTOUT, TIMER15_CH0, TIMER0_CH0_ON, SPI1_SCK, I2S1_CK, USART2_CTS
VDD	28	P		Default: VDD
PB15	29	I/O	5VT	Default: PB15 Alternate: I2S1_SD, USART1_TX, USART0_TX, I2C0_SCL, I2C1_SCL, IFRP_OUT, EVENTOUT, RTC_REFIN, TIMER0_CH2_ON, SPI1_MOSI
PA8	30	I/O	5VT	Default: PA8 Alternate: CK_OUT0, USART1_RX, USART0_RX, I2C0_SDA, I2C1_SDA, EVENTOUT, TIMER15_CH0, TIMER0_CH0, USART0_CK, USBFS_SOF, SDIO_D1, RTC_OUT
PA9	31	I/O	5VT	Default: PA9 Alternate: SPI0_MOSI, SDIO_CMD, SQPI_CLK, QSPI_SCK, EVENTOUT, TIMER15_CH0_ON, TIMER0_CH1, SPI1_SCK, I2S1_CK, USART0_TX, SDIO_D2
PA10	32	I/O	5VT	Default: PA10 Alternate: SPI0_MISO, SDIO_D0, SQPI_CSN, QSPI_CSN, EVENTOUT, TIMER16_CH0, TIMER0_CH2
PA11	33	I/O	5VT	Default: PA11 Alternate: SPI0_SCK, SDIO_CK, SQPI_D0, QSPI_IO0, EVENTOUT, TIMER16_BRKIN, TIMER0_CH3
PA12-WKUP3	34	I/O	5VT	Default: PA12 Alternate: SPI0_NSS, SDIO_D1, SQPI_D1, QSPI_IO1, EVENTOUT, TIMER16_CH0_ON, TIMER0_ETI, USART0_RTS / USART0_DE Additional: WKUP3
PB3	35	I/O	5VT	Default: JTDO, TRACESWO, PB3 Alternate: USART2_CTS, SPI0_IO2, SDIO_D2, SQPI_D2, QSPI_IO2, EVENTOUT, TIMER15_BRKIN, TIMER1_CH1, SPI0_SCK, USART0_RX
PB4	36	I/O	5VT	Default: NJTRST, PB4 Alternate: USART2_RTS / USART2_DE, SPI0_IO3, SDIO_D3, SQPI_D3, QSPI_IO3, TIMER1_CH0, TIMER1_ETI, EVENTOUT, SPI0_MISO

Note:

(1) Type: I = input, O = output, A = analog, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

2.6.3. GD32W515xx pin alternate functions

Table 2-5. Port A alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0	USART0_TX	TIMER1_CH0/TIMER1_ETI	TIMER4_CH0		TSI_G0_IO0			USART1_CTS								EVENTOUT
PA1	USART0_RX	TIMER1_CH1	TIMER4_CH1		TSI_G0_IO1			USART1_RTS / USART1_DE								EVENTOUT
PA2	USART0_CK	TIMER1_CH2	TIMER4_CH2		TSI_G0_IO2	I2S1_CKIN	TIMER0_CH0	USART1_TX							HPDF_AUDIO(1)	EVENTOUT
PA3	USART1_CK	TIMER1_CH3	TIMER4_CH3		TSI_G0_IO3	I2S1_MCK		USART1_RX	TIMER0_CH0_ON	RTC_OUT					HPDF_DATAIN1(1)	EVENTOUT
PA4	USART1_TX	I2S1_ADD_SD	SPI0_MOSI	QSPI_SCK	TIMER4_CH2	SPI0_NSS	SPI1_MOSI/I2S1_SD	USART1_CK	TIMER0_CH1					DCI_HSYNC(1)		EVENTOUT
PA5	USART1_RX		I2S1_MCK	QSPI_CSN	SPI0_MISO	SPI0_SCK		TIMER4_CH3	TIMER0_CH1_ON					DCI_VSYNC(1)		EVENTOUT
PA6			TIMER2_CH0	QSPI_IO0	I2S1_CKIN	SPI0_MISO	I2S1_MCK	SPI0_SCK	TIMER0_CH1	TIMER1_CH1	USART2_TX		SDIO_CMD	DCI_PIXCLK(1)	HPDF_AUDIO(1)	EVENTOUT
PA7	SPI1_NSS/I2S1_WS	TIMER0_CH0_ON	TIMER2_CH1	QSPI_IO1	SPI0_NSS	SPI0_MOSI	TIMER0_CH1_ON	DCI_D7(1)	USART2_RX	TIMER1_CH2						EVENTOUT
PA8	CK_OUT0	TIMER0_CH0	USART0_RX	USART1_RX		I2C0_SDA	I2C1_SDA	USART0_CK	TIMER15_CH0	RTC_OUT	USBFS_SOF		SDIO_D1			EVENTOUT
PA9	SPI0_MOSI	TIMER0_CH1	SDIO_CMD	SQPI_CLK	QSPI_SCK	SPI1_SCK/I2S1_CK		USART0_TX	TIMER15_CH0_ON				SDIO_D2	DCI_D0(1)		EVENTOUT
PA10	SPI0_MISO	TIMER0_CH2	SDIO_D0	SQPI_CSN	QSPI_CSN			TIMER16_CH0						DCI_D1(1)		EVENTOUT
PA11	SPI0_SCK	TIMER0_CH3	SDIO_CK	SQPI_D0	QSPI_IO0			TIMER16_BRKIN						DCI_D2(1)		EVENTOUT
PA12		TIMER0_ETI			QSPI_IO1		SPI0_NSS	USART0_RTS / USART0_DE	SQPI_D1		TIMER16_CH0_ON		SDIO_D1	DCI_D3(1)		EVENTOUT
PA13	JTMS/SWDIO			TSITG	I2C0_SMBA			USART0_CTS	USART1_CTS							EVENTOUT
PA14	JTCK/SWCLK				I2C1_SMBA			USART0_RTS / USART0_DE	USART1_RTS / USART1_DE							EVENTOUT

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA15	JTDI				I2C0_SCL	SPI0_NSS	I2C1_SCL	USART0_RX								EVENTOUT

Table 2-6. Port B alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB0		TIMER0_CH1_ON(1)	TIMER2_CH1(1)	TIMER3_CH0(1)	TSI_G1_IO0(1)								SDIO_D1(1)	DCI_D4(1)	DCI_D6(1)	EVENTOUT(1)
PB1		TIMER0_CH2_ON(1)	TIMER3_CH1(1)	TIMER2_CH2(1)	TSI_G1_IO1(1)								SDIO_D2(1)	DCI_D3(1)	DCI_D5(1)	EVENTOUT(1)
PB2		TIMER1_CH3(1)	TIMER3_CH2(1)	TIMER2_CH3(1)	TSI_G1_IO2(1)								SDIO_CK(1)	DCI_D2(1)	DCI_D4(1)	EVENTOUT(1)
PB3	JTDO/TRACESWO	TIMER1_CH1		QSPI_IO2		SPI0_SCK	SPI0_IO2	USART0_RX	SQPI_D2		USART2_CTS	TIMER15_BRKIN	SDIO_D2			EVENTOUT
PB4	NJTRST	TIMER1_CH0/TIMER1_ETI		QSPI_IO3		SPI0_MISO	SPI0_IO3	USART2_RTS / USART2_DE	SQPI_D3				SDIO_D3			EVENTOUT
PB5	IFRP_OUT(1)	TIMER1_CH3(1)			TSITG(1)	SPI0_MOSI(1)		USART2_CK(1)						DCI_D10(1)		EVENTOUT(1)
PB6						SPI1_MISO(1)								DCI_D5(1)		EVENTOUT(1)
PB7			TIMER3_CH1(1)		I2C0_SDA(1)	SPI1_NSS(1)/I2S1_WS(1)		USART0_RX(1)						DCI_VSYNC(1)		EVENTOUT(1)
PB8			TIMER3_CH2(1)			SPI1_SCK(1)/I2S1_CK(1)							SDIO_D4(1)	DCI_D6(1)		EVENTOUT(1)
PB9		TIMER1_CH1(1)	TIMER3_CH3(1)			SPI1_MOSI(1)/I2S1_SD(1)							SDIO_D5(1)	DCI_D7(1)		EVENTOUT(1)
PB10		TIMER1_CH2(1)	TIMER3_ETI(1)	TIMER3_CH3(1)	TSI_G1_IO3(1)			USART2_TX(1)	TIMER0_CH1(1)	IFRP_OUT(1)			SDIO_D7(1)	DCI_D1(1)	DCI_D3(1)	EVENTOUT(1)
PB11			TIMER0_CH1_ON		TSI_G2_IO0	I2S1_CKIN		USART2_RX			USBFS_ID		SDIO_D6	DCI_D0(1)	DCI_D2(1)	EVENTOUT
PB12		TIMER0_BRKIN	TIMER0_CH3		TSI_G2_IO1	SPI1_NSS/I2S1_WS		USART2_CK			USBFS_DP			DCI_D1(1)		EVENTOUT
PB13		TIMER0_CH0_ON			TSI_G2_IO2	SPI1_SCK/I2S1_CK		USART2_CTS	TIMER15_CH0		USBFS_DM			DCI_D0(1)		EVENTOUT
PB14		TIMER0_CH1_O			TSI_G2_IO3(1)	SPI1_MISO(1)	I2S1_ADD_SD(1)	USART2_RTS(1) /	TIMER15_BRKIN(1							EVENTOUT(1)

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		N(1)						USART2_DE(1)	)							
PB15	RTC_REFIN	TIMER0_CH2_ON			I2C0_SCL	SPI1_MOSI/I2S1_SD	I2C1_SCL	USART1_TX	USART0_TX	IFRP_OUT						EVENTOUT

Table 2-7. Port C alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC0	USART1_TX(1)		TIMER0_CH3(1)		I2C0_SMBA(1)									DCI_D4(1)	HPDF_CKIN0(1)	EVENTOUT(1)
PC1	USART1_RX(1)	TIMER0_BRKIN(1)			I2C1_SMBA(1)			SPI1_MOSI(1)/I2S1_SD(1)					DCI_HSYNC(1)	DCI_D8(1)	HPDF_CKIN1(1)	EVENTOUT(1)
PC2	TIMER0_ETI(1)	TIMER0_CH0(1)	TIMER4_CH0(1)		I2C0_SCL(1)	SPI1_MISO(1)	I2S1_ADD_SD(1)			I2C1_SDA(1)			DCI_VSYNC(1)	DCI_D9(1)	HPDF_CKOUT(1)	EVENTOUT(1)
PC3		TIMER1_CH0(1)/TIMER1_ETI(1)	TIMER4_CH1(1)		I2C0_SDA(1)	SPI1_MOSI(1)/I2S1_SD(1)	I2C1_SCL(1)		TIMER0_CH0_ON(1)				DCI_PIXCLK(1)	DCI_D11(1)	HPDF_DATAIN0(1)	EVENTOUT(1)
PC4		I2S1_ADD_SD(1)	TIMER2_CH2(1)	QSPI_IO2(1)			SPI0_IO2(1)		SQPI_CLK(1)				DCI_D6(1)	DCI_D12(1)		EVENTOUT(1)
PC5	CK_OUT1(1)	TIMER2_CH0(1)	TIMER2_CH3(1)	QSPI_IO3(1)			SPI0_IO3(1)	USART2_RX(1)	SQPI_CSN(1)				DCI_D7(1)	DCI_D13(1)	DCI_D5(1)	EVENTOUT(1)
PC6	TRACECK(1)	TIMER0_BRKIN(1)	TIMER2_CH0(1)			I2S1_MCK(1)		TIMER16_BRKIN(1)	TIMER0_CH1(1)	TIMER1_CH1(1)	USART2_TX(1)		SDIO_D6(1)	DCI_D0(1)		
PC7	TIMER0_ETI(1)		TIMER2_CH1(1)	TIMER0_CH1_ON(1)		SPI1_SCK(1)/I2S1_CK(1)		TIMER16_CH0(1)	USART2_RX(1)	TIMER1_CH2(1)			SDIO_D7(1)	DCI_D1(1)		
PC8			TIMER2_CH2			I2C0_SDA	I2C1_SDA	USART0_TX					SDIO_D0	DCI_D2(1)		EVENTOUT
PC14	USART0_CK	USART1_CK														EVENTOUT
PC15	IFRP_OUT															EVENTOUT

Note:

(1) Functions are available on GD32W515Px devices only.

3. Functional description

3.1. Arm® Cortex®-M33 core

The Cortex®-M33 processor is a 32-bit processor that possesses low interrupt latency and low-cost debug. The characteristics of integrated and advanced make the Cortex®-M33 processor suitable for market products that require microcontrollers with high performance and low power consumption.

32-bit Arm® Cortex®-M33 processor core

- Up to 180 MHz operation frequency
- Ultra-low power, energy-efficient operation
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M33 processor is based on the ARMv8 architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M33:

- Internal Bus Matrix connected with Code bus, System bus, and Private Peripheral Bus (PPB) and debug accesses
- Nested Vectored Interrupt Controller (NVIC)
- Breakpoint Unit (BPU)
- Data Watchpoint and Trace (DWT)
- Instrumentation Trace Macrocell (ITM)
- Serial Wire JTAG Debug Port (SWJ-DP)
- Trace Port Interface Unit (TPIU)
- Arm® TrustZone® technology, using the ARMv8-M main extension supporting secure and non-secure states
- Memory Protection Unit (MPU), supporting 8 regions for secure and 8 regions for non-secure.
- Configurable secure attribute unit (SAU) supporting up to 8 memory regions
- Floating Point Unit (FPU)
- DSP Extension (DSP)

3.2. On-chip memory

- Up to 2048 Kbytes of SIP Flash memory
- Up to 32M bytes of EXT Flash memory
- Up to 448 Kbytes of SRAM with hardware parity checking

2048 Kbytes of inner Flash or 32M bytes of EXT Flash memory, and 448 Kbytes of inner SRAM at most is available for storing programs and data. ***Table 2-2. GD32W515xx memory map*** shows the memory map of the GD32W515xx series of devices, including

code, SRAM, peripheral, and other pre-defined regions.

3.3. Clock, reset and supply management

- Internal 16 MHz factory-trimmed RC and external 20 to 52 MHz crystal oscillator
- Internal 32 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator
- Integrated system clock PLL
- 1.62 to 3.63 V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control Unit (CCTL) provides a range of oscillator and clock functions. These include speed internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum frequency of the AHB, APB2 and APB1 domains is 180 MHz/90 MHz/45MHz. See ***Figure 2-4. GD32W515xx clock tree*** for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 1.54 V and down to 1.50V. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- V_{DD} range: 1.62 to 3.63 V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA} is 0 V.
- V_{DDA} range: 2.7 to 3.63 V, external analog power supplies for ADC, reset blocks, RCs and PLL.
- V_{BAK} range: 1.62 to 3.63 V, power supply for RTC unit, LXTAL oscillator, BPOR, and two pads, including PC14 to PC15 when V_{DD} is not present.

3.4. Boot modes

At startup, a BOOT0 pin, a BOOT1 pin are used to select the boot memory address.

The BOOT0 value may come from the BOOT0 pin or from the value of SWBOOT0 bit in the EFUSE_CTL register to free the GPIO pad if needed.

The BOOT1 value may come from the PA14 pin or from the value of SWBOOT1 bit in the EFUSE_CTL register to free the GPIO pad if needed.

Table 3-1. BOOT0 modes

SWBOOT0	EFBOOT0	BOOT0 PC8 pin	BOOT0
0	-	0	0
0	-	1	1
1	0	-	0
1	1	-	1

Table 3-2. BOOT1 modes

SWBOOT1	EFBOOT1	BOOT1 PA14 pin	BOOT1
0	-	0	0
0	-	1	1
1	0	-	0
1	1	-	1

Refer to ***Table 3-3. Boot address modes when TrustZone is disabled (TZEN=0)*** and ***Table 3-4. Boot modes when TrustZone is enabled (TZEN=1)*** for boot address when TrustZone is disabled and enabled respectively. When the EFBOOTLK bit in the EFUSE_CTL register is set, the boot memory address selected according to boot1 and boot0.

Table 3-3. Boot address modes when TrustZone is disabled (TZEN=0)

EFBOOTLK	BOOT0	BOOT1	Boot address	Boot area
0	0	-	0x08000000	SIP Flash when cfg_qspi is 0 QSPI Flash when cfg_qspi is 1
0	1	0	0x0BF40000	Bootloader / ROM
0	1	1	0x0A000000	SRAM0
1	0	-	0x08000000	SIP Flash when cfg_qspi is 0 QSPI Flash when cfg_qspi is 1
1	1	-	0x0BF40000	Bootloader / ROM

When TrustZone is enabled by setting the TZEN option bit, the boot space must be in secure area.

Table 3-4. Boot modes when TrustZone is enabled (TZEN=1)

GSSACMD == 8'hc(1)	EFBOOTLK	BOOT0	BOOT1	EFSB	Boot address	Boot area
0	0	0	-	0	0x0C000000	SPI Flash when cfg_qspi is 0 QSPI Flash when

GSSACMD == 8'hc(1)	EFBOOTLK	BOOT0	BOOT1	EFSB	Boot address	Boot area
						cfg_qspi is 1
0	0	0	-	1	0X0FF84000	secure boot
0	0	1	0	-	0x0FF80000	GSSA
0	0	1	1	-	0x0E000000	SRAM0
-	1	0	-	0	0x0C000000	SPI Flash when cfg_qspi is 0 QSPI Flash when cfg_qspi is 1
-	1	0	-	1	0X0FF84000	secure boot
-	1	1	-	-	0x0FF80000	GSSA
1	0	-	-	-	0x0FF80000	GSSA

Note: (1) When the GSSACMD bit field is 0x0C, it means 1, otherwise it means 0.

The BOOTx (x=0/1) value (either coming from the pin or the EFBOOTx bit) is latched upon reset release. It is up to the user to set BOOTx values to select the required boot mode. The BOOTx pin or EFBOOTx bit (depending on the EFBOOTLK and SWBOOTx bit value in the EFUSE_CTL register) is also re-sampled when exiting from Standby mode. Consequently, they must be kept in the required Boot mode configuration in Standby mode. After startup delay, the selection of the boot area is done before releasing the processor reset.

The embedded boot loader is located in the System memory, which is used to reprogram the Flash memory. The boot loader can be activated through one of the following serial interfaces: USART0 (PA8, PB15), USART1 (PA2, PA3), USART2 (PB10, PB11) and USBFS (PB12/PB13/PB14).

3.5. Power saving modes

The MCU supports five kinds of power saving modes to achieve even lower power consumption. They are Sleep, Deep-sleep, Standby, SRAM_sleep and WIFI_sleep mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep** mode
  In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.
- **Deep-sleep** mode
  In Deep-sleep mode, all clocks in the 1.2V domain are off, and all of IRC16M, HXTAL and PLLs are disabled. The contents of SRAM0 and registers are preserved. In non-secure mode, any interrupt or wakeup event from EXTI lines can wake up the system

from the deep-sleep mode including the 16 external lines, the RTC alarm non-secure, LVD output, VLVDF interrupt, WIFI11N wakeup, USBFS wakeup, RTC Tamper and Timestamp non-secure, RTC Wakeup event non-secure, I2C0 wakeup and USART0/USART2 wakeup. In secure mode, any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 16 external lines, the RTC Alarm secure, LVD output, VLVDF interrupt, WIFI11N wakeup, USBFS wakeup, RTC Tamper and Timestamp secure, RTC Wakeup event secure, I2C0 wakeup and USART0/USART2 wakeup. When exiting the deep-sleep mode, the IRC16M is selected as the system clock.

- **Standby** mode
  In Standby mode, the whole 1.2V domain is power off, the LDO is shut down, and all of IRC16M, HXTAL and PLLs are disabled. There are four wakeup sources for the Standby mode, including the external reset from NRST pin, the RTC alarm/time stamp/tamper/auto wakeup events, the FWDGT reset, and the rising edge on WKUP pins.
- **SRAM_sleep** mode
  In SRAM_sleep mode, at least one of SRAM1/SRAM2/SRAM3 is power off. When the SRAM enters SRAM_sleep mode, the content of SRAM will lost. SRAM1/SRAM2/SRAM3 can be configured power on or power off when in run/sleep/deep_sleep mode. SRAM1/SRAM2/SRAM3 are power off when in standby mode/BKP_ONLY mode.
- **WIFI_sleep** mode
  In WIFI_sleep mode, WIFI_OFF domain power off. When exit from WIFI_sleep mode, Wi-Fi is active mode, all Wi-Fi power on.

3.6. Electronic fuse (EFUSE)

- One-time programmable nonvolatile EFUSE storage cells organized as 256*8 bit.
- All bits in the efuse cannot be rollback from 1 to 0.
- Can only be accessed through corresponding registers.

The Efuse controller has efuse macro that store system parameters. As a non-volatile unit of storage, the bit of efuse macro cannot be restored to 0 once it is programmed to 1. According to the software operation, the Efuse controller can program all the bits in the system parameters.

3.7. Instruction cache (ICACHE)

- Support 32KB cache with 2 ways, 1024 cache lines per way and 16B per cache line.
- Support fetch address without any wait state if cache hit.
- Support two performance counters: 32-bit hit monitor counter and16-bit miss monitor counter.
- Support TrustZone security and configure registers to be protected at system level.

The instruction cache (ICACHE) is based on C-AHB code bus of Cortex-M33 processor. It is necessary to improve performance in fetching instruction and data from both internal and external memories.

3.8. General-purpose inputs / outputs (GPIOs)

- Up to 43 fast GPIOs, all mappable on 16 external interrupt lines
- Analog input/output configurable
- Alternate function input/output configurable

There are up to 43 general purpose I/O pins (GPIO) in GD32W515xx, named PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC8, and PC14 ~ PC15 to implement logic input/output functions. Each GPIO port has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt/Event Controller Unit (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins.

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), input, peripheral alternate function or analog mode. Most of the GPIO pins are shared with digital or analog alternate functions.

3.9. TrustZone protection controller union (TZPCU)

- TZSPC, TZBMPC and TZIAC have independent 32-bit AHB interface.
- For TZSPC, whether non-secure/non-privilege access is supported that is defined by secure/privilege configuration registers.
- For TZBMPC and TZIAC, only secure access is supported.
- For securable slave/master peripherals, secure/privilege state is defined in TZSPC registers.
- For off-chip memories, the size of non-secure area is defined in TZSPC registers.
- For on-chip RAM, the secure states of all blocks is defined in TZBMPC registers.

This section describes the TrustZone® protection controller union. Three different sub-blocks, TrustZone® security privilege controller (TZSPC), TrustZone® block-based memory protection controller (TZBMPC) and TrustZone® illegal access controller (TZIAC), are used to configure system security or privileg in a product with programmable-security and privileged attributes. TZSPC is used to defines the secure/privilege state for securable slave/master peripherals. TrustZone® mark memory protection controller (TZMMPC) do the security checking of off-chip memories based on the size of non-secure area which is defined in TZSPC. For the on-chip RAM, the security checking is done based on block level which is configured by the TZBMPC through an AHB interface. TZIAC is used to enable all illegal access events for slave/master peripherals in system. If an interrupt is enabled, a dedicated interrupt signal is asserted and generates a secure

interrupt towards NVIC whenever a security violation is detected. The interrupt is cleared by writing to the appropriate register of TZIAC.

3.10. CRC calculation unit (CRC)

- 32-bit data input and 32-bit data output. Calculation period is 4 AHB clock cycles for 32-bit input data size from data entered to the calculation result available.
- Free 8-bit register is unrelated to calculation and can be used for any other goals by any other peripheral devices.
- Fixed polynomial: 0x4C11DB7
  $X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^{8}+X^{7}+X^{5}+X^{4}+X^{2}+X+1$

A cyclic redundancy check (CRC) is an error-detecting code commonly used in digital networks and storage devices to detect accidental changes to raw data. This CRC calculation unit can be used to calculate 32 bit CRC code with fixed polynomial.

3.11. True Random number generator (TRNG)

- About 40 periods of TRNG_CLK are needed between two consecutive random numbers
- Disable TRNG module will significantly reduce the chip power consumption
- 32-bit random value seed is generated from analog noise, so the random number is a true random number.

The true random number generator (TRNG) module can generate a 32-bit random value by using continuous analog noise.

3.12. Direct memory access controller (DMA)

- 8 channels for DMA0 controller and 8 channels for DMA1 controller.
- Peripherals supported: Timers, ADC, SPIs, I2S, QSPI, I2Cs, USARTs, DCI, CAU, HAU, SDIO and HPDF.

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby increasing system performance by off-loading the MCU from copying large amounts of data and avoiding frequent interrupts to serve peripherals needing more data or having available data. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory.

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

3.13. Analog to digital converter (ADC)

- 12-bit SAR ADC's conversion rate is up to 2.5 MSPS
- Hardware oversampling ratio adjustable from 2x to 256x improves resolution to 16-bit
- Input voltage range: 0 to V_{DDA}
- Temperature sensor

A 12-bit 2.5 MSPS multi-channel ADC is integrated in the device. It has a total of 12 multiplexed channels: up to 9 external channels, 1 channel for internal temperature sensor (V_{SENSE}), 1 channel for internal reference voltage (V_{REFINT}) and one channel for external battery power supply (V_{BAT}) channel. The input voltage range is between 0 and V_{DDA}. An on-chip hardware oversampling scheme improves performance while off-loading the related computational burden from the CPU. The analog watchdog allows the application to detect whether the input voltage goes outside the user-defined higher or lower thresholds. A configurable channel management block can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced use.

The ADC can be triggered from the events generated by the general level 0 timers (TIMERx, x=1, 2, 3, 4) and the advanced timers (TIMER0) with internal connection. The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected to the ADC_IN9 input channel which is used to convert the sensor output voltage in a digital value.

To ensure a high accuracy on ADC, the independent power supply V_{DDA} is implemented to achieve better performance of analog circuits. V_{DDA} can be externally connected to V_{DD} through the external filtering circuit that avoids noise on V_{DDA}, and V_{SSA} should be connected to V_{SS} through the specific circuit independently.

3.14. Real time clock (RTC)

- Independent binary-coded decimal (BCD) format timer / counter with twenty 32-bit backup registers.
- Calendar with sub-second, second, minute, hour, week day, day, month and year automatically correction.
- Alarm function with wake up from deep-sleep and standby mode capability.
- On-the-fly correction for synchronization with master clock. Digital calibration with 0.95 ppm resolution for compensation of quartz crystal inaccuracy.

The real time clock is an independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt or an expected interrupt. It is not reset by a system or power reset, or when the device wakes up from standby mode. In the RTC unit, there are two prescalers used for

implementing the calendar and other functions. One prescaler is a 7-bit asynchronous prescaler and the other is a 15-bit synchronous prescaler.

3.15. Timers and PWM generation

- One 16-bit advanced timer (TIMER0), two 32-bit general timer (TIMER1, TIMER2), up to four 16-bit general timers (TIMER3, TIMER4, TIMER15 ~ TIMER16), and one 16-bit basic timer (TIMER5)
- Up to 4 independent channels of PWM, output compare or input capture for each general timer and external trigger input
- 16-bit, motor control PWM advanced timer with programmable dead-time generation for output match
- Encoder interface controller with two inputs using quadrature decoder
- Two 24-bit SysTick timers down counter, a Non-secure SysTick timer and a Secure SysTick timer
- 2 watchdog timers (free watchdog timer and window watchdog timer)

The advanced timer (TIMER0) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general timer. The 4 independent channels can be used for input capture, output compare, PWM generation (edge- or center- aligned counting modes) and single pulse mode output. If configured as a general 16-bit timer, it has the same functions as the TIMERx. It can be synchronized with external signals or to interconnect with other general timers together which have the same architecture and features.

The general timer can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TIMER1 and TIMER2 are based on a 32-bit auto-reload up/down counter and a 16-bit prescaler. TIMER3 and TIMER4 is based on a 16-bit auto-reload up/down counter and a 16-bit prescaler. TIMER15 ~ TIMER16 are based on a 16-bit auto-reload up counter and a 16-bit prescaler. The general timer also supports an encoder interface with two inputs using quadrature decoder.

The basic timer TIMER5, is mainly used as a simple 16-bit time base.

The GD32W515xx have two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-stage prescaler. It is clocked from an independent 32 KHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wakeup interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. The features are shown below:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.16. Universal synchronous asynchronous receiver transmitter (USART)

- Maximum speed up to 11.25 MBits/s
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- ISO 7816-3 compliant smart card interface
- Dual clock domain
- Wake up from Deep-sleep mode

The USART (USART0, USART1, USART2) are used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART transmitter and receiver. The USART also supports DMA function for high speed data communication.

3.17. Inter-integrated circuit (I2C)

- Support both master and slave mode with a frequency up to 1 MHz (Fast mode plus)
- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Supports 7-bit and 10-bit addressing mode and general call addressing mode
- SMBus 3.0 and PMBus 1.3 compatible
- Wakeup from Deep-sleep mode on I2C0 address match

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides different data transfer rates: up to 100

KHz in standard mode, up to 400 KHz in the fast mode and up to 1 MHz in the fast mode plus. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

3.18. Serial peripheral interface (SPI)

- Up to two SPI interfaces with a frequency of up to 22.5 MHz
- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking
- Quad-SPI configuration available in master mode (only in SPI0)

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). All SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking. Quad-SPI master mode is also supported in SPI0.

3.19. Inter-IC sound (I2S)

- Sampling frequency from 8 KHz to 192 KHz
- Support either master or slave mode

The Inter-IC sound (I2S) bus provides a standard communication interface for digital audio applications by 4-wire serial lines. GD32W515xx contain an I2S-bus interface that can be operated with 16/32 bit resolution in master or slave mode, pin multiplexed with SPI1. The audio sampling frequency from 8 KHz to 192 KHz is supported.

3.20. Serial / Quad Parallel Interface (SQPI)

- SQPI controller support configuring output clock frequency which is divided by HCLK.
- SQPI controller support no address phase and data phase operation which is named special command by the controller.
- SQPI controller support 256MB external memory space.
  Logic memory address range: 0x6000_0000 - 0x6FFF_FFFF.
- SQPI controller support 6 types mode for different combination of command, address, waitcycle, and data phase.

Serial/Quad Parallel Interface (SQPI) is a controller for external serial/dual/quad parallel interface memory peripheral. For example: SQPI-PSRAM and SQPI-FLASH. With this controller, users can use external SQPI interface memory as SRAM simply.

3.21. Quad-SPI interface (QSPI)

- Four functional modes: indirect(address extend), status-polling, memory-mapped and FMC mode
- Fully programmable command format for both indirect and memory mapped mode
- Integrated FIFO for transmission/reception
- 8, 16, or 32-bit data accesses
- DMA channel for indirect mode
- Support TrustZone architecture to isolate the secure area and non-secure area

The QSPI is a specialized interface that communicate with Flash memories. This interface support single, dual or quad SPI FLASH.

3.22. Secure digital input and output card interface (SDIO)

- Support SD2.0/SDIO2.0/MMC4.2 host interface

The Secure Digital Input and Output Card Interface (SDIO) provides access to external SD memory cards specifications version 2.0, SDIO card specification version 2.0 and multi-media card system specification version 4.2 with DMA supported. In addition, this interface is also compliant with CE-ATA digital protocol rev1.1.

3.23. Universal serial bus full-speed interface (USBFS)

- One USB device/host/OTG full-speed Interface with frequency up to 12 Mbit/s
- Internal main PLL for USBCLK compliantly
- Internal USBFS PHY support

The Universal Serial Bus (USB) is a 4-wire bus with 4 bidirectional endpoints. The device controller enables 12 Mbit/s data exchange with integrated transceivers. Transaction formatting is performed by the hardware, including CRC generation and checking. It supports both host and device modes, as well as OTG mode with Host Negotiation Protocol (HNP) and Session Request Protocol (SRP). The controller contains a full-speed USB PHY internal. For full-speed or low-speed operation, no more external PHY chip is needed. It supports all the four types of transfer (control, bulk, Interrupt and isochronous) defined in USB 2.0 protocol. The required precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use an HXTAL crystal oscillator).

3.24. Digital camera interface (DCI)

- Digital video/picture capture
- 8/10/12/14 data width supported

- High transfer efficiency with DMA interface
- Video/picture crop supported
- Various pixel formats supported including JPEG/YCrCb/RGB
- Hard/embedded synchronous signals supported

DCI is an 8-bit to 14-bit parallel interface that able to capture video or picture from a camera via Digital Camera Interface. It supports 8/10/12/14 bits data width through DMA operation.

3.25. Touch sensing interface (TSI)

- 3 fully parallel groups implemented.
- 9 IOs configurable for capacitive sensing Channel Pins and 3 for Sample Pins.
- Configurable transfer sequence frequency.

Touch Sensing Interface (TSI) provides a convenient solution for touch keys, sliders and capacitive proximity sensing applications. The controller builds on charge transfer method. Placing a finger near fringing electric fields adds capacitance to the system and TSI is able to measure this capacitance change using charge transfer method.

3.26. Cryptographic acceleration Unit (CAU)

- Supports DES, TDES or AES (128, 192, or 256) algorithms.
- DES/TDES supports Electronic codebook (ECB) or Cipher block chaining (CBC) mode
- AES supports 128bits-key, 192bits-key or 256 bits-key
- AES supports Electronic codebook (ECB), Cipher block chaining (CBC) mode, Counter mode (CTR) mode, Galois/counter mode (GCM), Galois message authentication code mode (GMAC), Counter with CBC-MAC (CCM), cipher message authentication code mode (CMAC), Cipher Feedback mode (CFB) and Output Feedback mode (OFB).
- DMA transfer for incoming and outgoing data is supported

The Cryptographic Acceleration Unit supports acceleration of DES, TDES or AES (128, 192, or 256) algorithms. The DES/TDES supports Electronic codebook (ECB) or Cipher block chaining (CBC) mode. The AES supports Electronic codebook (ECB), Cipher block chaining (CBC) mode, Counter mode (CTR) mode, Galois/counter mode (GCM), Galois message authentication code mode (GMAC), Counter with CBC-MAC (CCM), Cipher Feedback mode (CFB) and Output Feedback mode (OFB).

3.27. Hash acceleration unit (HAU)

- Supports SHA-1, SHA-224 and SHA-256 algorithms, compliant with FIPS PUB 180-

2 (Federal Information Processing Standards Publication 180-2)

- Supports MD5 compliant with IETF RFC 1321 (Internet Engineering Task Force Request For Comments number 1321)
- Supports HMAC (keyed-hash message authentication code) algorithm
- Automatic swapping to comply with the big-endian or little-endian for MD5, SHA-1, SHA-224 and SHA-256 algorithms
- Automatic padding to fit module 512
- Support DMA mode for input data flow

The HAU supports acceleration of SHA-1, SHA-224, SHA-256, MD5 algorithm and the HMAC (keyed-hash message authentication code) algorithm, which calling the SHA-1, SHA-224, SHA-256 or MD5 hash function to calculate key, message, digest three times.

3.28. Public Key Cryptographic Acceleration Unit (PKCAU)

- Support RSA/DH algorithms with up to 3136 bits of operands
- Support ECC algorithm with up to 640 bits of operands
- Embedded RAM of 3584 bytes
- Conversion between the Montgomery domain and the natural domain
- only 32-bit access is supported

Public key encryption is also called asymmetric encryption, asymmetric encryption algorithms use different keys for encryption and decryption. The Public Key Cryptographic Acceleration Unit (PKCAU) can accelerate RSA (Rivest, Shamir and Adleman), Diffie-Hellmann (DH key exchange) and ECC (elliptic curve cryptography) in GF(p) (Galois domain). These operations are performed in the Montgomery domain to improve computational efficiency.

3.29. High-Performance Digital Filter (HPDF)

- Two multiplex digital serial input channels
- Two internal digital parallel input channels
- Up to 24 bit output data resolution
- Flexible conversion configuration function
- Configurable Sinc filter and integrator

A high performance digital filter module (HPDF) for external sigma delta (Σ-Δ) modulator is integrated in GD32W515xx. HPDF supports SPI interface and Manchester-coded single-wire interface. The external sigma delta modulator can be connected with MCU by the serial interface, and the serial data stream output by sigma delta modulator can be filtered. In addition, HPDF also supports the parallel data stream input function to filter the data in the internal memory of the MCU.

3.30. Infrared ray port (IFRP)

- The IFRP output signal is decided by TIMER15_CH0 and TIMER16_CH0.
- To get correct infrared ray signal, TIMER15 should generate low frequency modulation envelope signal, and TIMER16 should generate high frequency carrier signal.

Infrared ray port (IFRP) is used to control infrared light LED, and send out infrared data to implement infrared ray remote control.

There is no register in this module, which is controlled by TIMER15 and TIMER16. The IFRP_OUT pin can be configured by GPIO alternate function selected register.

3.31. Wi-Fi

3.31.1. Standards Supported

- 802.11b/g/n(2.4G) compatible
- 802.11e QoS Enhancement (WMM)
- 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services
- Wi-Fi WPS
- Wi-Fi Direct
- Integrated TCP/IP protocol

3.31.2. Wi-Fi MAC

- Transmission and reception of aggregated MPDUs (A-MPDU) for high throughput (HT).
- Support for immediate ACK and Block-ACK policies.
- Support for power management schemes, including WMM power-save, power-save multi-poll (PSMP), and multiphase PSMP operation.
- Interframe space timing support, including RIFS.
- Support for RTS/CTS and CTS-to-self frame sequences for protecting frame exchanges.
- Back-off counters in hardware for supporting multiple priorities as specified in the WMM specification.
- Timing synchronization function (TSF), network allocation vector (NAV) maintenance, and target beacon transmission time (TBTT) generation in hardware.
- Hardware engine for AES-CCMP, legacy WPA TKIP, legacy WEP ciphers, and support for key management.
- Programmable independent basic service set (IBSS) or infrastructure basic service set or Access Point functionality.

3.31.3. Wi-Fi PHY

- Single antenna 1x1 stream in 20MHz and 40MHz channels
- Supports IEEE 802.11b DSSS-CCK modulation: 1, 2, 5.5, 11Mbps
- Supports IEEE 802.11g OFDM modulation: 6, 9, 12,18, 24, 36, 48, 54Mbps
- Supports IEEE 802.11n HT modulations MCS0-7, 20MHz, 800ns guard interval: 6.5, 13.0, 19.5, 26, 39, 52.0, 58.5, 65.0Mbps
- Supports IEEE 802.11n HT modulations MCS0-7, 20MHz, 400ns guard interval: 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65, 72.2Mbps
- Supports IEEE 802.11n HT modulations MCS0-7, 40MHz, 800ns guard interval: 13.5, 27, 40.5, 54, 81, 108, 121.5, 135Mbps
- Supports IEEE 802.11n HT modulations MCS0-7, 40MHz, 400ns guard interval: 15, 30, 45, 60, 90, 120, 135, 150Mbps
- IEEE 802.11n mixed mode operation
- Per packet TX power control
- Advanced channel estimation/equalization, automatic gain control, CCA, carrier/symbol recovery, and frame detection
- Digital calibration algorithms to handle CMOS RF chip process, voltage, and temperature (PVT) variations
- Per-packet channel quality and signal-strength measurements
- Compliance with FCC and other worldwide regulatory requirements

3.31.4. Wi-Fi Radio

- Fractional-N for multiple reference clock support
- Integrated PA with power control
- Optimized Tx gain distribution for linearity and noise performance
- Direct conversion architecture
- On-chip gain selectable LNA with optimized noise figure
- High dynamic range AGC
- Frequency Range 2.4G-2.5G

3.32. Debug mode

- Serial wire JTAG debug port (SWJ-DP)

The Arm® SWJ-DP Interface is embedded and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

3.33. Package and operation temperature

- QFN56 (GD32W515Px) and QFN36 (GD32W515Tx).
- Operation temperature range: -40°C to +85°C (industrial level).

4. Electrical characteristics

4.1. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1. Absolute maximum ratings (1)(4)

Symbol	Parameter	Min	Max	Unit
V_{DD}	External voltage range(2)	- 0.3	3.63	V
V_{DDA}	External analog supply voltage	- 0.3	3.63	V
V_{BAT}	External battery supply voltage	- 0.3	3.63	V
AVDD33_ANA	Wi-Fi Analog voltage	- 0.3	3.63	V
AVDD33_PA	Wi-Fi PA voltage	- 0.3	3.63	V
AVDD33_CLK	Wi-Fi Clock voltage	- 0.3	3.63	V
V_{IN}	Input voltage on 5V tolerant pin(3)	- 0.3	V_{DD} + 3.63	V
	Input voltage on other I/O	- 0.3	3.63	V
$\|\Delta V_{DDx}\|$	Variations between different VDD power pins	—	50	mV
I_{IO}	Maximum current for GPIO pin	—	±25	mA
T_A	Operating temperature range	-40	+85	°C
P_D	Power dissipation at T_A = 85°C of QFN56	—	1044	mW
	Power dissipation at T_A = 85°C of QFN36	—	939	
T_{STG}	Storage temperature range	-65	+150	°C
T_J	Maximum junction temperature	—	125	°C

(1) Guaranteed by design, not tested in production.

(2) All main power and ground pins should be connected to an external power source within the allowable range. When the RF function dose not used, the power supply of AVDD33_PA can be disconnected, and when EFUSE function dose not used, the power supply of AVDD33_ANA can be disconnected.

(3) V_{IN} maximum value cannot exceed 5.5 V.

(4) It is recommended that VDD and VDDA are powered by the same source. The maximum difference between VDD and VDDA does not exceed 300 mV during power-up and operation.

4.2. Operating conditions characteristics

Table 4-2. DC operating conditions

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DD}	Supply voltage	—	1.62(2)	3.3	3.63	V
		—	2.7	3.3	3.63	
V_{DDA}	Analog supply voltage	—	2.7	3.3	3.63	V
V_{BAT}	Battery supply voltage	—	1.62(2) (3)	3.3	3.63	V

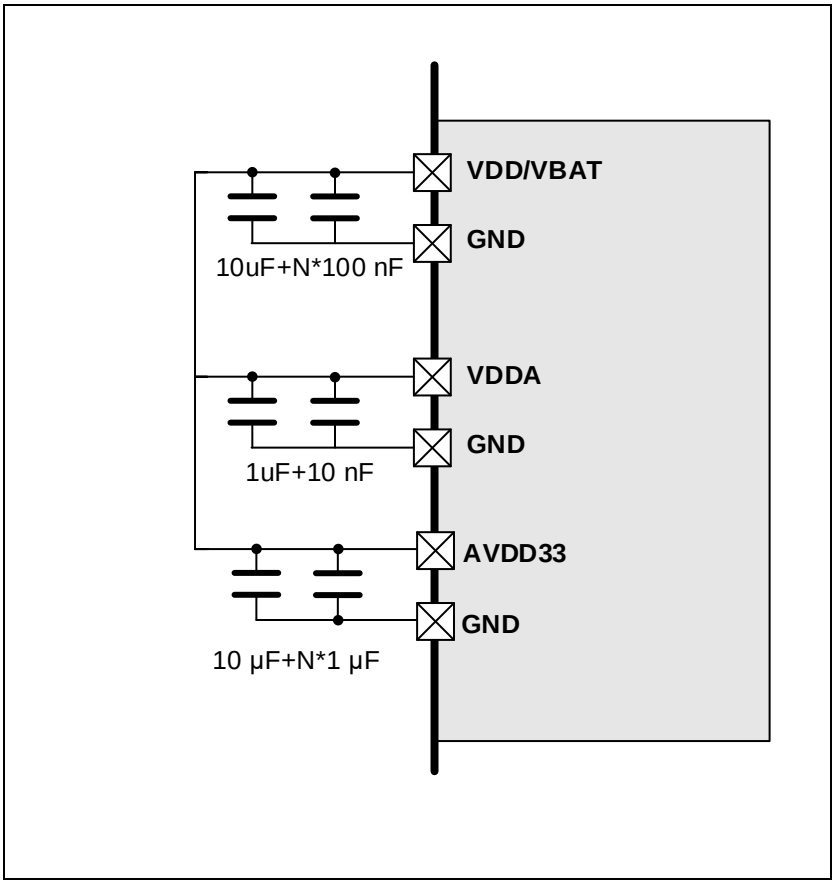
Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
		—	2.7(3)	3.3	3.63	
AVDD33_ANA	Wi-Fi Analog voltage	—	3.0	3.3	3.63	V
AVDD33_PA	Wi-Fi PA voltage	—	3.0	3.3	3.63	V
AVDD33_CLK	Wi-Fi Clock voltage	—	3.0	3.3	3.63	V

(1) Based on characterization, not tested in production.

(2) Only for GD32W515P0Q6.

(3) In the application which V_{BAT} supply the backup domains, if the V_{BAT} voltage drops below the minimum value, when V_{DD} is powered on again, it is necessary to refresh the registers of backup domains and enable LXTAL again

Figure 4-1. Recommended power supply decoupling capacitors(1)(2)(3)



(1) When using precision internal reference voltage, and a bypass capacitor about 0.1 µF (or 1 µF connected in parallel, which is recommended) to ground is required.

(2) AVDD33 include AVDD33_PA, AVDD33_ANA, AVDD33_CLK. When the W515 does not use the Wi-Fi function, AVDD33_CLK and AVDD33_ANA normally supplies power and attaches 1uF decoupling capacitor. It is recommended that AVDD33_PA supply power without decoupling capacitor to save BOM.

(3) All decoupling capacitors need to be as close as possible to the pins on the PCB board.

Table 4-3. Clock frequency (1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	AHB clock frequency	—	—	180	MHz
f_{APB1}	APB1 clock frequency	—	—	45	MHz
f_{APB2}	APB2 clock frequency	—	—	90	MHz

(1) Guaranteed by design, not tested in production.

Table 4-4. Operating conditions at Power up / Power down (1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	—	—	∞	μs /V
	V_{DD} fall time rate		20	—	

(1) Guaranteed by design, not tested in production.

Table 4-5. Start-up timings of Operating conditions (1)(2)(3)

Symbol	Parameter	Conditions	Typ	Unit
$t_{start-up}$	Start-up time	Clock source from HXTAL	1415	μs
		Clock source from IRC16M	246	

(1) Based on characterization, not tested in production.

(2) After power-up, the start-up time is the time between the rising edge of NRST high and the first I/O instruction.

(3) PLL is off.

Table 4-6. Power saving mode wakeup timings characteristics (1)(2)

Symbol	Parameter	Typ	Unit
t_{Sleep}	Wakeup from Sleep mode	7.2	μs
$t_{Deep-sleep}$	Wakeup from Deep-sleep mode (LDO On)	1.7	
	Wakeup from Deep-sleep mode (LDO in low power mode)	1.7	
	Wakeup from Deep-sleep mode (LDO On and Low driver mode)	62	
	Wakeup from Deep-sleep mode (LDO in low power and Low driver mode)	62	
$t_{Standby}$	Wakeup from Standby mode	261	

(1) Based on characterization, not tested in production.

(2) The wakeup time is measured from the wakeup event to the point at which the application code reads the first instruction under the below conditions: V_{DD} = V_{DDA} = 3.3 V, IRC16M = System clock = 16 MHz.

4.3. Power consumption

GD32W515xx is designed with advanced power management technologies and suitable for Internet of Things applications.

Table 4-7. Wi-Fi Power consumption characteristics

Power Mode	MCU State	Wi-Fi State
Active	Active	Active
Wi-Fi Sleep	Active	Power save mode: Wi-Fi wake up periodically to listen beacon frame to stay connected to the AP.
Mild Sleep	Power on, PLL off, Clock gated	Power save mode: Wi-Fi wake up periodically to listen beacon frame to stay connected to the AP.
Hibernation	Mostly power off, only the wake up source is power on	Power off
Shutdown	—	Power off

Table 4-8. Wi-Fi Power consumption characteristics(1)(2)(3)

Power Mode	Description	Consumption	unit
Active	Wi-Fi Tx 802.11b, CCK 1Mbps, Pout = +18dBm(4)	338	mA
	Wi-Fi Tx 802.11b, CCK 11Mbps, Pout = +17dBm(4)	323	mA
	Wi-Fi Tx 802.11g, OFDM 6Mbps, Pout = +18dBm(4)	327	mA
	Wi-Fi Tx 802.11g, OFDM 54Mbps, Pout = +15dBm(4)	289	mA
	Wi-Fi Tx 802.11n, HT 20M MCS0, Pout = +16dBm(4)	297	mA
	Wi-Fi Tx 802.11n, HT 20M MCS7, Pout = +13dBm(4)	272	mA
	Wi-Fi Tx 802.11n, HT 40M MCS0, Pout = +14dBm(4)	280	mA
	Wi-Fi Tx 802.11n, HT 40M MCS7, Pout = +12dBm(4)	267	mA
	Wi-Fi Rx 802.11b, CCK 1Mbps, -90dBm(5)	101	mA
	Wi-Fi Rx 802.11b, CCK 11Mbps, -80Bm(5)	102	mA
	Wi-Fi Rx 802.11g, OFDM 6Mbps, -80dBm(5)	120	mA
	Wi-Fi Rx 802.11g, OFDM 54Mbps, -70dBm(5)	126	mA
	Wi-Fi Rx 802.11n, HT 20M MCS0, -75dBm(5)	120	mA
	Wi-Fi Rx 802.11n, HT 20M MCS7, -65dBm(5)	126	mA
	Wi-Fi Rx 802.11n, HT 40M MCS0, -72dBm(5)	124	mA
	Wi-Fi Rx 802.11n, HT 40M MCS7, -62dBm(5)	129	mA
Wi-Fi Sleep	MCU in Run mode(6)	56.5	mA
Mild Sleep	DTIM=1	1.5	mA
	DTIM=3	0.75	mA
Hibernation	MCU in Standby mode(7)	5.4	μA
Shutdown	—	—	mA

(1) Below data are measured at antenna port of GD Wi-Fi Demo board.
(2) Unless otherwise specified, all values given for TA condition and test result is mean value.
(3) DC Power = 3.3 V, HXTAL = 40 MHz, System clock = 180 MHz.
(4) Continuous Tx, Duty cycle = 100%.
(5) Rx Packet Length = 1024 Bytes.
(6) V_{DD} = V_{DDA} = 3.3 V, HXTAL = 40 MHz, System clock = 180 MHz, all peripherals enabled, except Wi-Fi.
(7) V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC32K on, RTC on.

Table 4-9. Power consumption characteristics (2)(3)(4)(5)(6)(7)

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
I_{DD}+I_{DDA}	Supply current (Run mode)	V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 180 MHz, All peripherals enabled	—	56.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 180 MHz, All peripherals	—	29.7	—	mA

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		disabled				
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 168 MHz, All peripherals enabled	—	52.9	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 168 MHz, All peripherals disabled	—	27.8	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 120 MHz, All peripherals enabled	—	38.4	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 120 MHz, All peripherals disabled	—	20.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 108 MHz, All peripherals enabled	—	34.8	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 108 MHz, All peripherals disabled	—	18.6	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 96 MHz, All peripherals enabled	—	31.2	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 96 MHz, All peripherals disabled	—	16.8	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 72 MHz, All peripherals enabled	—	24	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 72 MHz, All peripherals disabled	—	13.2	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 48 MHz, All peripherals enabled	—	16.6	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 48 MHz, All peripherals disabled	—	9.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 36 MHz, All peripherals enabled	—	13	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 36 MHz, All peripherals	—	7.7	—	mA

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		disabled				
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 25 MHz, PLL off, All peripherals enabled	—	9.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 25 MHz, PLL off, All peripherals disabled	—	5.8	—	mA
		V_{DD} = V_{DDA} = 3.3 V, use IRC16M, System clock = 16 MHz, PLL off, All peripherals enabled	—	7.8	—	mA
		V_{DD} = V_{DDA} = 3.3 V, use IRC16M, System clock = 16 MHz, PLL off, All peripherals disabled	—	4.8	—	mA
		V_{DD} = V_{DDA} = 3.3 V, use IRC16M, System clock = 8 MHz, PLL off, All peripherals enabled	—	5.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, use IRC16M, System clock = 8 MHz, PLL off, All peripherals disabled	—	3.6	—	mA
		V_{DD} = V_{DDA} = 3.3 V, use IRC16M, System clock = 4 MHz, PLL off, All peripherals enabled	—	4.4	—	mA
		V_{DD} = V_{DDA} = 3.3 V, use IRC16M, System clock = 4 MHz, PLL off, All peripherals disabled	—	3.1	—	mA
		V_{DD} = V_{DDA} = 3.3 V, use IRC16M, System clock = 2 MHz, PLL off, All peripherals enabled	—	3.8	—	mA
		V_{DD} = V_{DDA} = 3.3 V, use IRC16M, System clock = 2 MHz, PLL off, All peripherals disabled	—	2.8	—	mA
	Supply current (Sleep mode)	V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 180 MHz, CPU clock off, All peripherals enabled	—	43.1	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 180 MHz, CPU clock off, All peripherals disabled	—	16.1	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 168 MHz, CPU clock off, All peripherals enabled	—	40.3	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 168 MHz, CPU clock off,	—	15.1	—	mA

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		All peripherals disabled				
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 120 MHz, CPU clock off, All peripherals enabled	—	29	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 120 MHz, CPU clock off, All peripherals disabled	—	11	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 108 MHz, CPU clock off, All peripherals enabled	—	26.2	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 108 MHz, CPU clock off, All peripherals disabled	—	9.9	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 96 MHz, CPU clock off, All peripherals enabled	—	23.4	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 96 MHz, CPU clock off, All peripherals disabled	—	8.9	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 72 MHz, CPU clock off, All peripherals enabled	—	17.7	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 72 MHz, CPU clock off, All peripherals disabled	—	6.9	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 48 MHz, CPU clock off, All peripherals enabled	—	12.1	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 48 MHz, CPU clock off, All peripherals disabled	—	4.9	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 36 MHz, CPU clock off, All peripherals enabled	—	9.3	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 36 MHz, CPU clock off, All peripherals disabled	—	3.8	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 25 MHz, PLL off, CPU clock off, All peripherals enabled	—	6.4	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 25 MHz, PLL off, CPU	—	2.7	—	mA

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		clock off, All peripherals disabled				
		V_{DD} = V_{DDA} = 3.3 V, use IRC16M, System Clock = 16 MHz, PLL off, CPU clock off, All peripherals enabled	—	5.3	—	mA
		V_{DD} = V_{DDA} = 3.3 V, use IRC16M, System Clock = 16 MHz, PLL off, CPU clock off, All peripherals disabled	—	2.4	—	mA
		V_{DD} = V_{DDA} = 3.3 V, use IRC16M, System Clock = 8 MHz, PLL off, CPU clock off, All peripherals enabled	—	3.6	—	mA
		V_{DD} = V_{DDA} = 3.3 V, use IRC16M, System Clock = 8 MHz, PLL off, CPU clock off, All peripherals disabled	—	1.7	—	mA
		V_{DD} = V_{DDA} = 3.3 V, use IRC16M, System Clock = 4 MHz, PLL off, CPU clock off, All peripherals enabled	—	2.7	—	mA
		V_{DD} = V_{DDA} = 3.3 V, use IRC16M, System Clock = 4 MHz, PLL off, CPU clock off, All peripherals disabled	—	1.4	—	mA
		V_{DD} = V_{DDA} = 3.3 V, use IRC16M, System Clock = 2 MHz, PLL off, CPU clock off, All peripherals enabled	—	2.3	—	mA
		V_{DD} = V_{DDA} = 3.3 V, use IRC16M, System Clock = 2 MHz, PLL off, CPU clock off, All peripherals disabled	—	1.3	—	mA
	Supply current (Deep-Sleep mode)	V_{DD} = V_{DDA} = 3.3 V, LDO in normal power and normal driver mode, IRC32K off, RTC off	—	379.3	—	μA
		V_{DD} = V_{DDA} = 3.3 V, LDO in low power and normal driver mode, IRC32K off, RTC off	—	325	—	μA
		V_{DD} = V_{DDA} = 3.3 V, LDO in normal power and low driver mode, IRC32K off, RTC off	—	229.7	—	μA
		V_{DD} = V_{DDA} = 3.3 V, LDO in low power and low driver mode, IRC32K off, RTC off	—	200.8	—	μA
		V_{DD} = V_{DDA} = 3.3 V, LDO in low power and low driver mode, IRC32K off, RTC off, Wi-Fi、SRAM1、SRAM2、SRAM3 sleep	—	129	—	μA
	Supply current (Standby mode)	V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC32K on, RTC on	—	5.75	—	μA
		V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC32K on, RTC off	—	5.55	—	μA

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC32K off, RTC off	—	5.25	—	μA
I_{BAT}	Battery supply current (Backup mode)	V_{DD} off, V_{DDA} off, V_{BAT} = 3.63V, LXTAL on with external crystal, RTC on, LXTAL Highest driving	—	1.98	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3V, LXTAL on with external crystal, RTC on, LXTAL Highest driving	—	1.88	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 2.7V, LXTAL on with external crystal, RTC on, LXTAL Highest driving	—	1.77	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 1.62V, LXTAL on with external crystal, RTC on, LXTAL Highest driving	—	1.43	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.63V, LXTAL on with external crystal, RTC on, LXTAL Higher driving	—	1.57	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3V, LXTAL on with external crystal, RTC on, LXTAL Higher driving	—	1.48	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 2.7V, LXTAL on with external crystal, RTC on, LXTAL Higher driving	—	1.37	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 1.62V, LXTAL on with external crystal, RTC on, LXTAL Higher driving	—	1.17	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.63V, LXTAL on with external crystal, RTC on, LXTAL High driving	—	1.16	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3V, LXTAL on with external crystal, RTC on, LXTAL High driving	—	1.08	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 2.7V, LXTAL on with external crystal, RTC on, LXTAL High driving	—	0.97	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 1.62V, LXTAL on with external crystal, RTC on, LXTAL High driving	—	0.82	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.63V, LXTAL on with external crystal, RTC on, LXTAL Lower driving	—	1.03	—	μA

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3V, LXTAL on with external crystal, RTC on, LXTAL Lower driving	—	0.94	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 2.7V, LXTAL on with external crystal, RTC on, LXTAL Lower driving	—	0.83	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 1.62V, LXTAL on with external crystal, RTC on, LXTAL Lower driving	—	0.68	—	μA

(1) Based on characterization, not tested in production.
(2) Unless otherwise specified, all values given for T_A condition and test result is mean value.
(3) When System Clock is greater than 16 MHz, a crystal 25 MHz is used, and the HXTAL bypass function is closed, using PLL.
(4) When analog peripheral blocks such as ADCs, HXTAL, LXTAL, IRC16M, or IRC32K are ON, an additional power consumption should be considered.
(5) With large margin, it will be adjusted according to the mass production data.
(6) When Wi-Fi power off.
(7) All GPIOs are configured as analog mode except standby mode.

4.4. EMC characteristics

EMS (electromagnetic susceptibility) includes ESD (Electrostatic discharge, positive and negative) and FTB (Burst of Fast Transient voltage, positive and negative) testing result is given in ***Table 4-10. EMS characteristics***, based on the EMS levels and classes compliant with IEC 61000 series standard.

Table 4-10. EMS characteristics (1)

Symbol	Parameter	Conditions	Level/Class
V_{ESD}	Voltage applied to all device pins to induce a functional disturbance	V_{DD} = V_{DDA} = AVDD33 = 3.3 V, T_A = 25 °C, Wi-Fi on, QFN56, f_{HCLK} = 180 MHz conforms to IEC 61000-4-2	2A
V_{FTB}	Fast transient voltage burst applied to induce a functional disturbance through 100 pF on VDD and GND	V_{DD} = V_{DDA} = AVDD33 = 3.3 V, T_A = 25 °C, Wi-Fi on, QFN56, f_{HCLK} = 180 MHz conforms to IEC 61000-4-4	4A

(1) Based on characterization, not tested in production.

4.5. Power supply supervisor characteristics

Table 4-11. Power supply supervisor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LVD}(1)	Low Voltage Detector	LVDT[2:0] = 000, rising edge	—	2.21	—	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Threshold	LVDT[2:0] = 000, falling edge	—	2.11	—	V
		LVDT[2:0] = 001, rising edge	—	2.37	—	V
		LVDT[2:0] = 001, falling edge	—	2.25	—	V
		LVDT[2:0] = 010, rising edge	—	2.51	—	V
		LVDT[2:0] = 010, falling edge	—	2.39	—	V
		LVDT[2:0] = 011, rising edge	—	2.65	—	V
		LVDT[2:0] = 011, falling edge	—	2.54	—	V
		LVDT[2:0] = 100, rising edge	—	2.80	—	V
		LVDT[2:0] = 100, falling edge	—	2.68	—	V
		LVDT[2:0] = 101, rising edge	—	2.94	—	V
		LVDT[2:0] = 101, falling edge	—	2.83	—	V
		LVDT[2:0] = 110, rising edge	—	3.08	—	V
		LVDT[2:0] = 110, falling edge	—	2.98	—	V
		LVDT[2:0] = 111, rising edge	—	3.23	—	V
		LVDT[2:0] = 111, falling edge	—	3.13	—	V
V_{VLVD}(1)	V_{DDA} Low Voltage Detector Threshold	—	—	2.36	—	V
$V_{LVDhyst}$(2)	LVD hysteresis	—	—	100	—	mV
V_{POR}(1)	Power on reset threshold	—	—	1.55	—	V
V_{PDR}(1)	Power down reset threshold		—	1.51	—	V
$V_{PDRhyst}$(2)	PDR hysteresis		—	40	—	mV
$t_{RSTTEMPO}$(2)	Reset temporization		—	2.45	—	ms

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

4.6. Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on the two measurement methods.

Table 4-12. ESD characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25 °C; ESDA/JEDEC JS-001-2017	—	—	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25 °C; ESDA/JEDEC JS-002-2018	—	—	500	V

(1) Based on characterization, not tested in production.
(2) There is space for adjustment, it will be tested soon.

Table 4-13. Static latch-up characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LU	I-test	T_A = 25 °C; JESD78E	—	—	±200	mA
	V_{supply} over voltage		—	—	5.4	V

(1) Based on characterization, not tested in production.
(2) There is space for adjustment, it will be tested soon.

4.7. External clock characteristics

Table 4-14. High speed external clock (HXTAL) generated from a crystal / ceramic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL}(1)	Frequency Range	—	19.2	40	52	MHz
C_{HXTAL}(2)	Crystal load Capacitance	—	9	10	12	pF
ESR(2)	Equivalent Series Resistance	—	—	—	70	Ω
f_tol(2)	Frequency tolerance	Initial and over temperature	-20	—	20	ppm
$t_{SUHXTAL}$(1)	Crystal startup time	V_{DD} = 3.3 V, T_A = 25 °C, f_{HXTAL} = 40 MHz	—	1.2	—	ms

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

Table 4-15. High speed external user clock characteristics (HXTAL in bypass mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL_ext}(1)	Frequency Range	—	—	40	—	MHz
V_{HXTAL}(2)	OSCIN Input Voltage	—	0.7	—	3.3	V
$Ducy_{(HXTAL)}$(2)	Duty cycle	—	45	50	55	%
PN(2)	Phase Noise	@1kHz, f_{HXTAL} = 40 MHz	—	—	-125	dBc/Hz
		@10kHz f_{HXTAL} = 40 MHz	—	—	-138	dBc/Hz
		@100kHz f_{HXTAL} = 40 MHz	—	—	-143	dBc/Hz
f_tol(2)	Frequency tolerance	Initial and over temperature	-20	—	20	ppm

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Table 4-16. Low speed external clock (LXTAL) generated from a crystal / ceramic characteristics

	Parameter	Conditions	Min	Typ	Max	Unit
f_{LXTAL}(1)	Crystal or ceramic frequency	V_{DD} = 3.3 V	—	32.768	—	kHz
C_{LXTAL}(2)(3)	Recommended matching capacitance on OSC32IN and OSC32OUT	—	—	15	—	pF
g_m(2)	Oscillator transconductance	Lower driving capability	—	4.5	—	µA/V
		Medium low driving capability	—	6.5	—	
		Medium high driving capability	—	13	—	
		Higher driving capability	—	19	—	
$I_{DDLXTAL}$(1)	Crystal or ceramic operating current	V_{DD} = V_{DDA} = 3.3 V, Lower driving capability	—	0.8	—	µA
		V_{DD} = V_{DDA} = 3.3 V, Medium low driving capability	—	0.94	—	
		V_{DD} = V_{DDA} = 3.3 V, Medium high driving capability	—	1.34	—	
		V_{DD} = V_{DDA} = 3.3 V, Higher driving capability	—	1.74	—	
$t_{SULXTAL}$(1)(4)	Crystal or ceramic startup time	V_{DD} = 3.3 V	—	2	—	s

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) C_{LXTAL1} = C_{LXTAL2} = 2*(C_{LOAD} - C_S), For C_{LXTAL1} and C_{LXTAL2}, it is recommended matching capacitance on OSC32IN and OSC32OUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

(4) $t_{SULXTAL}$ is the startup time measured from the moment it is enabled (by software) to the 32.768 kHz oscillator stabilization flags is SET. This value varies significantly with the crystal manufacturer.

Table 4-17. Low speed external user clock characteristics (LXTAL in bypass

mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LXTAL_ext}(1)	External clock source or oscillator frequency	V_{DD} = 3.3 V	—	32.768	1000	kHz
V_{LXTALH}(2)	OSC32IN input pin high level voltage	V_{DD} = 3.3 V	0.7*V_{DD}	—	—	V
V_{LXTALL}(2)	OSC32IN input pin low level voltage		—	—	0.3*V_{DD}	
$t_{H/L(LXTAL)}$(2)	OSC32IN high or low time	—	450	—	—	ns
$t_{R/F(LXTAL)}$(2)	OSC32IN rise or fall time	—	—	—	50	
C_{IN}(2)	OSC32IN input capacitance	—	—	5	—	pF
$Ducy_{(LXTAL)}$(2)	Duty cycle	—	30	—	70	%

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

4.8. Internal clock characteristics

Table 4-18. High speed internal clock (IRC16M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC16M}	High Speed Internal Oscillator (IRC16 M) frequency	V_{DD} = V_{DDA} = 3.3 V	—	16	—	MHz
ACC_{IRC16M}	IRC16 M oscillator Frequency accuracy, Factory-trimmed	2.7 V ≤ V_{DD} = V_{DDA} ≤ 3.63 V, T_A = -40 °C ~ +85 °C(1)	—	-1.6 to 1.3	—	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = 25°C	-1	—	1	%
	IRC16 M oscillator Frequency accuracy, User trimming step(1)	—	—	0.5	—	%
$Ducy_{IRC16M}$(2)	IRC16 M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V	45	—	55	%
$I_{DDAIRC16M}$(1)	IRC16 M oscillator operating current	V_{DD} = V_{DDA} = 3.3 V	—	80	—	μA
$t_{SUIRC16M}$(1)	IRC16 M oscillator startup time	V_{DD} = V_{DDA} = 3.3 V	—	1.5	—	μs

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Table 4-19. Low speed internal clock (IRC32K) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC32K}(1)	Low Speed Internal oscillator (IRC32K) frequency	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +85 °C	—	32	—	kHz
$I_{DDAIRC32K}$(2)	IRC32K oscillator operating current	V_{DD} = V_{DDA} = 3.3 V	—	0.4	—	μA
$t_{SUIRC32K}$(2)	IRC32K oscillator startup time	V_{DD} = V_{DDA} = 3.3 V	—	40	—	μs

(1) Guaranteed by design, not tested in production.
(2) Based on characterization, not tested in production.

4.9. PLL characteristics

Table 4-20. PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}(1)	PLL input clock frequency	—	1	—	2	MHz
f_{PLLOUT}(2)	PLL output clock frequency	—	—	—	200	MHz
f_{VCO}(2)	PLL VCO output clock frequency	—	—	—	400	MHz
t_{LOCK}(2)	PLL lock time	—	—	—	300	µs
I_{DDA}(2)	Current consumption on V_{DDA}	VCO freq = 400 MHz	—	2	—	mA
$Jitter_{PLL}$(3)	Cycle to cycle Jitter (rms)	VCO freq = 360 MHz	—	30	—	ps
	Cycle to cycle Jitter (peak to peak)		—	210	—	

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) Value given with main PLL running.

Table 4-21. PLLDIG characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}(1)	PLL input clock frequency	—	19.2	40	52	MHz
f_{PLLOUT}(2)	PLL output clock frequency	—	—	—	480	MHz
f_{VCO}(2)	PLL VCO output clock frequency	—	—	960	—	MHz
t_{LOCK}(2)	PLL lock time	—	—	—	50	µs
I_{DDA}(2)	Current consumption	—	—	3.5	—	mA
$Jitter_{PLL}$	Absolute RMS Jitter	XTAL freq = 40 MHz	—	6.5	—	ps

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

Table 4-22. PLLI2S characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}(1)	PLL input clock frequency	—	2	—	16	MHz
f_{VCO}(2)	PLL VCO output clock frequency	—	—	—	550	MHz
t_{LOCK}(2)	PLL lock time	—	—	—	300	µs
I_{DDA}(2)	Current consumption on V_{DDA}	VCO freq = 550 MHz	—	1.5	—	mA
$Jitter_{PLL}$(3)	Cycle to cycle rms Jitter	System clock	—	40	—	ps

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) Value given with main PLL running.

4.10. Memory characteristics

Table 4-23. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PE_{CYC}(1)	Number of guaranteed program /erase cycles before failure(Endurance)	T_A = -40 °C ~ +85 °C	100	—	—	kcycles
t_{RET}(1)	Data retention time	—	—	20	—	years
t_{PROG}(2)	word programming time	T_A = -40 °C ~ +105 °C	—	47.5	106	μs
t_{ERASE}(2)	Page(3) erase time	T_A = -40 °C ~ +105 °C	—	45	300	ms
t_{MERASE}(2)	Mass erase time	T_A = -40 °C ~ +105 °C	—	6	20	s

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) 4KB.

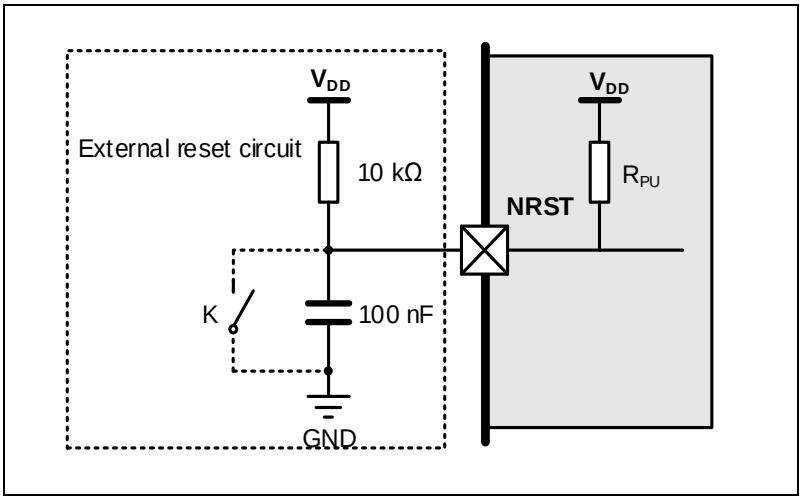
4.11. NRST pin characteristics

Table 4-24. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage	V_{DD} = V_{DDA} = 2.7 V	-0.5	—	0.35 V_{DD}	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage		0.65 V_{DD}	—	V_{DD} + 0.5	
V_{hyst}(1)	Schmidt trigger Voltage hysteresis		—	250	—	mV
$V_{IL(NRST)}$(1)	NRST Input low level voltage	V_{DD} = V_{DDA} = 3.3 V	-0.5	—	0.35 V_{DD}	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage		0.65 V_{DD}	—	V_{DD} + 0.5	
V_{hyst}(1)	Schmidt trigger Voltage hysteresis		—	280	—	mV
$V_{IL(NRST)}$(1)	NRST Input low level voltage	V_{DD} = V_{DDA} = 3.63 V	-0.5	—	0.35 V_{DD}	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage		0.65 V_{DD}	—	V_{DD} + 0.5	
V_{hyst}(1)	Schmidt trigger Voltage hysteresis		—	300	—	mV
R_{pu}(2)	Pull-up equivalent resistor	—	—	40	—	kΩ

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

Figure 4-2. Recommended external NRST pin circuit(1)



(1) Unless the voltage on NRST pin go below $V_{IL(NRST)}$ level, the device would not generate a reliable reset.

4.12. GPIO characteristics

Table 4-25. I/O port DC characteristics (1)(3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard IO Low level input voltage	1.62 V ≤ V_{DD} ≤ 3.63 V	—	—	0.35 V_{DD}	V
	5V-tolerant IO Low level input voltage	1.62 V ≤ V_{DD} ≤ 3.63 V	—	—	0.35 V_{DD}	V
V_{IH}	Standard IO Low level input voltage	1.62 V ≤ V_{DD} ≤ 3.63 V	0.65 V_{DD}	—	—	V
	5V-tolerant IO Low level input voltage	1.62 V ≤ V_{DD} ≤ 3.63 V	0.65 V_{DD}	—	—	V
V_{OL} (IO_speed = 166 MHz)	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.62V	—	0.142	—	V
		V_{DD} = 2.7V	—	0.1	—	V
		V_{DD} = 3.3 V	—	0.1	—	
		V_{DD} = 3.63V	—	0.1	—	
V_{OL} (IO_speed = 166 MHz)	Low level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 1.62V	—	0.427	—	V
		V_{DD} = 2.7V	—	0.2	—	V
		V_{DD} = 3.3 V	—	0.2	—	
		V_{DD} = 3.63V	—	0.2	—	
V_{OH} (IO_speed = 166 MHz)	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.62V	—	1.406	—	V
		V_{DD} = 2.7V	—	2.6	—	V
		V_{DD} = 3.3 V	—	3.2	—	
		V_{DD} = 3.63V	—	3.5	—	
V_{OH} (IO_speed = 166 MHz)	High level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 1.62V	—	1.265	—	V
		V_{DD} = 2.7V	—	2.3	—	V
		V_{DD} = 3.3 V	—	3.0	—	
		V_{DD} = 3.63V	—	3.3	—	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL} (IO_speed = 25 MHz)	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.62V	—	0.204	—	V
		V_{DD} = 2.7V	—	0.1	—	V
		V_{DD} = 3.3 V	—	0.1	—	
		V_{DD} = 3.63V	—	0.1	—	
V_{OL} (IO_speed = 25 MHz)	Low level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 1.62V	—	1.477	—	V
		V_{DD} = 2.7V	—	0.3	—	V
		V_{DD} = 3.3 V	—	0.3	—	
		V_{DD} = 3.63V	—	0.3	—	
V_{OH} (IO_speed = 25 MHz)	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.62V	—	1.297	—	V
		V_{DD} = 2.7V	—	2.5	—	V
		V_{DD} = 3.3 V	—	3.1	—	
		V_{DD} = 3.63V	—	3.4	—	
V_{OH} (IO_speed = 25 MHz)	High level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 1.62V	—	1.125	—	V
		V_{DD} = 2.7V	—	2.2	—	V
		V_{DD} = 3.3 V	—	2.9	—	
		V_{DD} = 3.63V	—	3.2	—	
V_{OL} (IO_speed = 10 MHz)	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.62V	—	0.403	—	V
		V_{DD} = 2.7V	—	0.2	—	V
		V_{DD} = 3.3 V	—	0.2	—	
		V_{DD} = 3.63V	—	0.2	—	
V_{OL} (IO_speed = 10 MHz)	Low level output voltage for an IO Pin (I_{IO} = +16 mA)	V_{DD} = 1.62V	—	1.381	—	V
		V_{DD} = 2.7V	—	0.5	—	V
		V_{DD} = 3.3 V	—	0.4	—	
		V_{DD} = 3.63V	—	0.4	—	
V_{OH} (IO_speed = 10 MHz)	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.62V	—	1.073	—	V
		V_{DD} = 2.7V	—	2.4	—	V
		V_{DD} = 3.3 V	—	3.1	—	
		V_{DD} = 3.63V	—	3.4	—	
V_{OH} (IO_speed = 10 MHz)	High level output voltage for an IO Pin (I_{IO} = +16 mA)	V_{DD} = 1.62V	—	0.927	—	V
		V_{DD} = 2.7V	—	2.1	—	V
		V_{DD} = 3.3 V	—	2.8	—	
		V_{DD} = 3.63V	—	3.1	—	
V_{OL} (IO_speed = 2 MHz)	Low level output voltage for an IO Pin (I_{IO} = +1 mA)	V_{DD} = 1.62V	—	0.160	—	V
		V_{DD} = 2.7V	—	0.1	—	V
		V_{DD} = 3.3 V	—	0.1	—	
		V_{DD} = 3.63V	—	0.1	—	
V_{OL} (IO_speed = 2 MHz)	Low level output voltage for an IO Pin (I_{IO} = +2 mA)	V_{DD} = 1.62V	—	0.359	—	V
	Low level output voltage for an IO Pin	V_{DD} = 2.7V	—	0.4	—	V
		V_{DD} = 3.3 V	—	0.4	—	

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
	(I_{IO} = +4 mA)		V_{DD} = 3.63V	—	0.4	—	
V_{OH} (IO_speed = 2 MHz)	High level output voltage for an IO Pin (I_{IO} = +1 mA)		V_{DD} = 1.62V	—	1.375	—	V
			V_{DD} = 2.7V	—	2.6	—	V
			V_{DD} = 3.3 V	—	3.2	—	
			V_{DD} = 3.63V	—	3.5	—	
V_{OH} (IO_speed = 2 MHz)	High level output voltage for an IO Pin (IIO = +2 mA)		V_{DD} = 1.62V	—	1.130	—	V
	High level output voltage for an IO Pin (I_{IO} = +4 mA)		V_{DD} = 2.7V	—	2.2	—	V
			V_{DD} = 3.3 V	—	2.9	—	
			V_{DD} = 3.63V	—	3.2	—	
R_{PU}(2)	Internal pull-up resistor	All pins	—	—	40	—	kΩ
		PU	—	—	10	—	
R_{PD}(2)	Internal pull-down resistor	All pins	—	—	40	—	kΩ
		PU	—	—	10	—	

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) All pins except PC13 / PC14 / PC15. Since PC13 to PC15 are supplied through the Power Switch, which can only be obtained by a small current, the speed of GPIOs PC13 to PC15 should not exceed 2 MHz when they are in output mode (maximum load: 30 pF).

Table 4-26. I/O port AC characteristics (1)(2)

GPIOx_MDy[1:0] bit value(3)	Parameter	Conditions	Typ	Unit
GPIOx_CTL->MDy[1:0]=10 (IO_Speed = 2 MHz)	Maximum frequency(4)	1.62 V ≤ V_{DD} ≤ 3.63 V , CL = 10pF	5	MHz
		1.62 V ≤ V_{DD} ≤ 3.63 V , CL = 30pF	4	
		1.62 V ≤ V_{DD} ≤ 3.63 V , CL = 50pF	4	
GPIOx_CTL->MDy[1:0] = 01 (IO_Speed = 10 MHz)	Maximum frequency(4)	1.62 V ≤ V_{DD} ≤ 3.63 V , CL = 10pF	25	MHz
		1.62 V ≤ V_{DD} ≤ 3.63 V , CL = 30pF	23	
		1.62 V ≤ V_{DD} ≤ 3.63 V , CL = 50pF	22	
GPIOx_CTL->MDy[1:0]=11 (IO_Speed = 25 MHz)	Maximum frequency(4)	1.62 V ≤ V_{DD} ≤ 3.63 V , CL = 10pF	86	MHz
		1.62 V ≤ V_{DD} ≤ 3.63 V , CL = 30pF	61	
		1.62 V ≤ V_{DD} ≤ 3.63 V, CL = 50pF	53	
GPIOx_CTL->MDy[1:0]=11(IO_Speed = 166 MHz)	Maximum frequency(4)	1.62 V ≤ V_{DD} ≤ 3.63 V, CL = 10pF	180	MHz
		1.62 V ≤ V_{DD} ≤ 3.63 V , CL = 30pF	155	
		1.62 V ≤ V_{DD} ≤ 3.63 V , CL = 50pF	133	

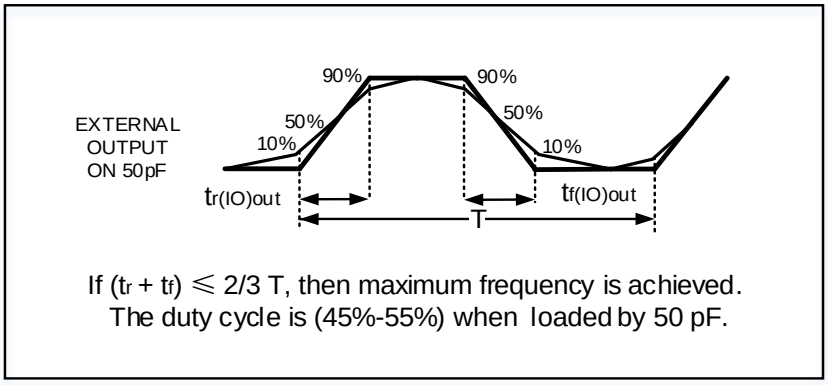
(1) Based on characterization, not tested in production.

(2) Unless otherwise specified, all test results given for T_A = 25 ℃.

(3) The I/O speed is configured using the GPIOx_OSPD0->OSPDy [1:0] bits. Refer to the GD32W515xx user manual which is selected to set the GPIO port output speed.

(4) The maximum frequency is defined in Figure 4-3, and maximum frequency cannot exceed 100 MHz.

Figure 4-3. I/O port AC characteristics definition



4.13. ADC characteristics

Table 4-27. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}(1)	Operating voltage	—	2.7	3.3	3.6	V
V_{IN}(1)	ADC input voltage range	—	0	—	V_{DDA}	V
f_{ADC}(1)	ADC clock	—	0.1	—	35	MHz
f_S(1)	Sampling rate	12-bit	0.007	—	2.5	MSPS
V_{AIN}(1)	Analog input voltage	9 external; 3 internal	0	—	V_{DDA}	V
R_{AIN}(2)	External input impedance	See ***Equation 1***	—	—	440.7	kΩ
R_{ADC}(2)	Input sampling switch resistance	—	—	—	0.5	kΩ
C_{ADC}(2)	Input sampling capacitance	No pin / pad capacitance included	—	—	3.2	pF
t_s(2)	Sampling time	f_{ADC} = 35 MHz	0.04	—	13.7	μs
t_{CONV}(2)	Total conversion time(including sampling time)	12-bit	—	14	—	1 / f_{ADC}
t_{SU}(2)	Startup time	—	—	—	1	μs

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Equation 1: R_{AIN} max formula $R_{AIN} < \frac{T_s}{f_{ADC} * C_{ADC} * \ln(2^{N+2})} - R_{ADC}$

The formula above (Equation 1) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 4-28. ADC R_{AIN} max for f_{ADC} = 35 MHz (1)

T_s(cycles)	t_s(μs)	R_{AINmax}(kΩ)
1.5	0.04	0.88
14.5	0.41	12.84
27.5	0.79	24.80

T_s(cycles)	t_s(μs)	R_{AINmax}(kΩ)
55.5	1.59	50.57
83.5	2.39	76.33
111.5	3.19	102.1
143.5	4.10	131.5
479.5	13.7	440.7

(1) Based on characterization, not tested in production.

Table 4-29. ADC dynamic accuracy at f_{ADC} = 35 MHz (1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 35 MHz, V_{DDA} = 3.3 V, Input Frequency = 20 kHz, Temperature = 25℃	—	10.6	—	bits
SNDR	Signal-to-noise and distortion ratio		—	65.7	—	dB
SNR	Signal-to-noise ratio		—	66.5	—	
THD	Total harmonic distortion		—	-72	—	

(1) Based on characterization, not tested in production.

Table 4-30. ADC static accuracy at f_{ADC} = 35 MHz

Symbol	Parameter	Test conditions	Typ(1)	Max	Unit
Offset	Offset error	f_{ADC} = 35 MHz, V_{DDA} = 3.3 V	±1	—	LSB
DNL	Differential linearity error		±1	—	
INL	Integral linearity error		±2	—	

(1) Based on characterization, not tested in production.

4.14. Temperature sensor characteristics

Table 4-31. Temperature sensor characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
T_L	V_{SENSE} linearity with temperature	—	±1	—	℃
Avg_Slope	Average slope	—	4.3	—	mV/℃
V_{25}	Voltage at 25 °C	—	1.42	—	V
t_{START}	Startup time	—	8	—	μs
t_{S_temp}(2)	ADC sampling time when reading the temperature	—	13.7	—	μs

(1) Based on characterization, not tested in production.

(2) Shortest sampling time can be determined in the application by multiple iterations.

4.15. I2C characteristics

Table 4-32. I2C characteristics (1)(2)(3)

Symbol	Parameter	Conditions	Standard mode		Fast mode		Fast mode plus		Unit
			Min	Max	Min	Max	Min	Max	
$t_{SCL(H)}$	SCL clock high time	—	4.0	—	0.6	—	0.2	—	μs
$t_{SCL(L)}$	SCL clock low time	—	4.7	—	1.3	—	0.5	—	μs
$t_{SU(SDA)}$	SDA setup time	—	250	—	100	—	50	—	ns
$t_{H(SDA)}$	SDA data hold time	—	0(3)	3450	0	900	0	450	ns
$t_{R(SDA/SCL)}$	SDA and SCL rise time	—	—	1000	—	300	—	120	ns
$t_{F(SDA/SCL)}$	SDA and SCL fall time	—	—	300	3(4)(5)	300	3(4)(6)	120	ns
$t_{H(STA)}$	Start condition hold time	—	4.0	—	0.6	—	0.26	—	μs
$t_{SU(STA)}$	Repeated Start condition setup time	—	4.7	—	0.6	—	0.26	—	μs
$t_{SU(STO)}$	Stop condition setup time	—	4.0	—	0.6	—	0.26	—	μs
t_{BUFF}	Stop to Start condition time (bus free)	—	4.7	—	1.3	—	0.5	—	μs

(1) Guaranteed by design, not tested in production.

(2) To ensure the standard mode I2C frequency, f_{PCLK1} must be at least 2 MHz. To ensure the fast mode I2C frequency, f_{PCLK1} must be at least 4 MHz. To ensure the fast mode plus I2C frequency, f_{PCLK1} must be at least a multiple of 10 MHz.

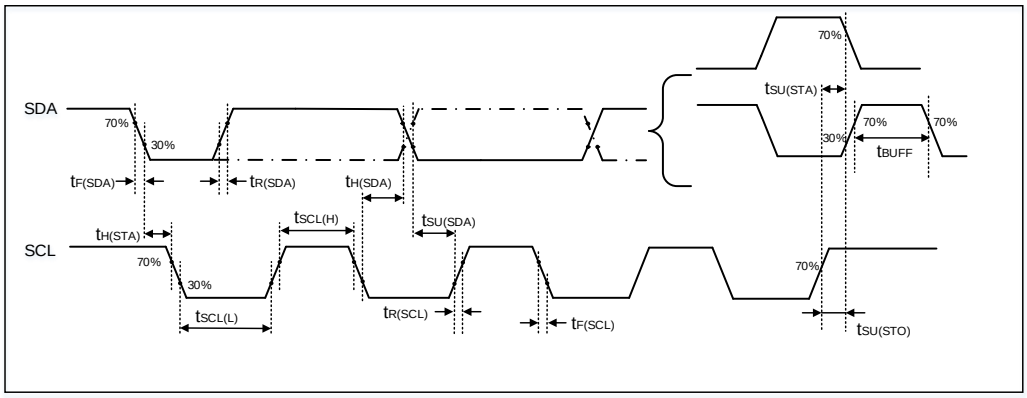
(3) The external device should provide a data hold time of 300 ns at least in order to bridge the undefined region of the falling edge of SCL.

(4) Based on characterization, not tested in production.

(5) In the condition of I2C frequency = 400 kHz, IO_Speed = 50 MHz and Pull-up resistor = 1 kΩ.

(6) In the condition of I2C frequency = 1 MHz, IO_Speed = 50 MHz and Pull-up resistor = 1 kΩ.

Figure 4-4. I2C bus timing diagram



4.16. SPI characteristics

Table 4-33. Standard SPI characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	V_{DD} = V_{DDA} = 3.3 V	—	—	22.5	MHz
$T_{SCK(H)}$	SCK clock high time		—	22.22	—	ns
$T_{SCK(L)}$	SCK clock low time		—	22.22	—	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time	V_{DD} = V_{DDA} = 3.3 V	—	—	7	ns
$t_{SU(MI)}$	Data input setup time		2	—	—	ns
$t_{H(MI)}$	Data input hold time		0	—	—	ns
SPI slave mode						
$t_{SU(NSS)}$	NSS enable setup time	V_{DD} = V_{DDA} = 3.3 V, f_{PCLK} = 90 MHz	0	—	—	ns
$t_{H(NSS)}$	NSS enable hold time		2	—	—	ns
$t_{A(SO)}$	Data output access time		—	6	—	ns
$t_{DIS(SO)}$	Data output disable time	V_{DD} = V_{DDA} = 3.3 V	—	9	—	ns
$t_{V(SO)}$	Data output valid time		—	9	—	ns
$t_{SU(SI)}$	Data input setup time		0	—	—	ns
$t_{H(SI)}$	Data input hold time		1	—	—	ns

(1) Based on characterization, not tested in production.

Figure 4-5. SPI timing diagram - master mode

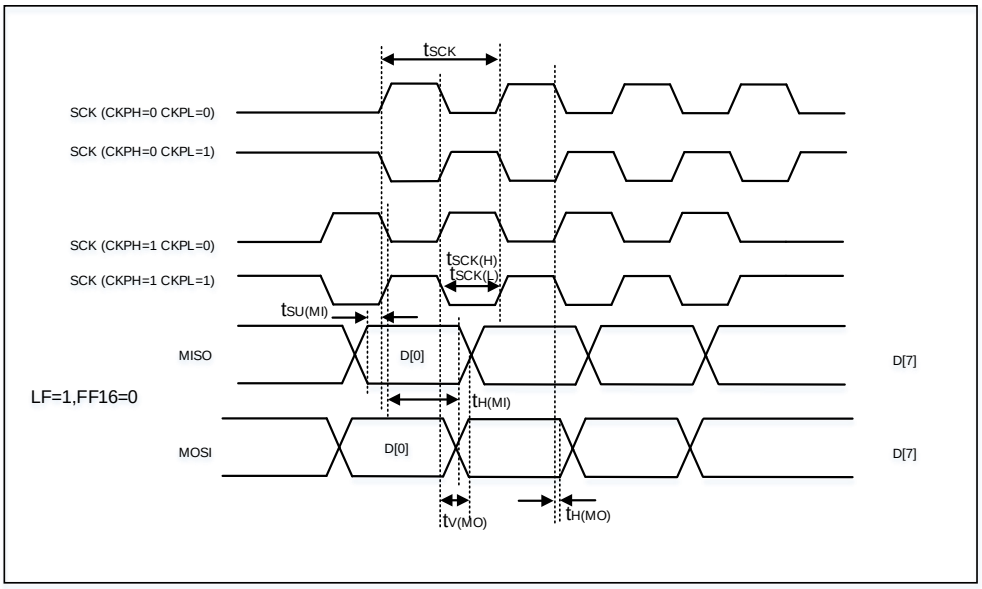
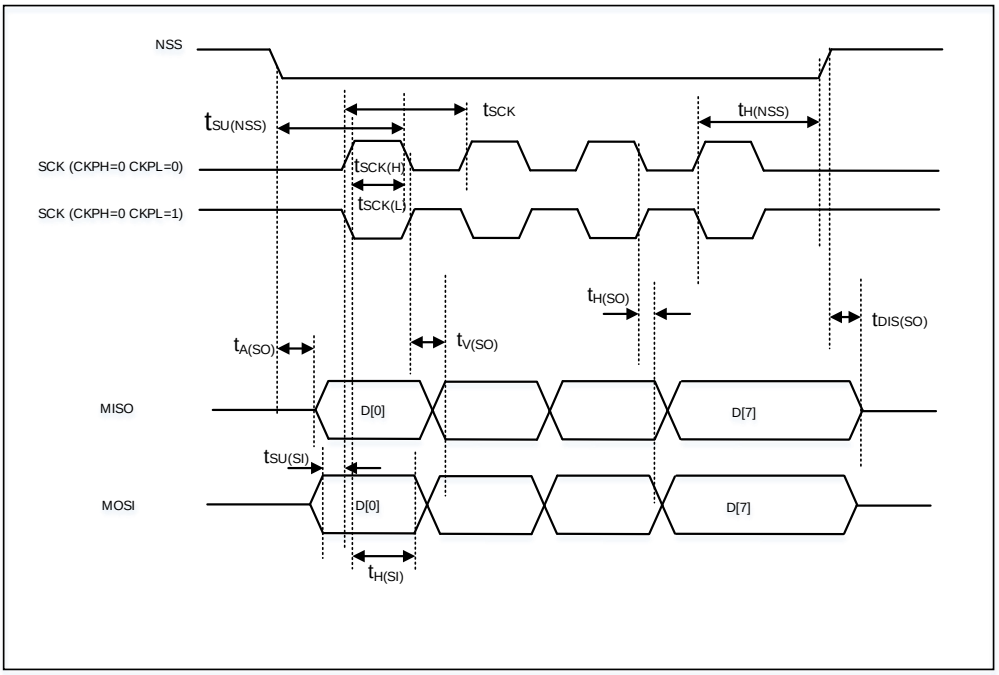


Figure 4-6. SPI timing diagram - slave mode



4.17. I2S characteristics

Table 4-34. I2S characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	Clock frequency	Master mode (data: 32 bits, Audio frequency = 96 kHz)	—	6.25	—	MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		Slave mode	—	—	12.5	
t_H	Clock high time	f_{CK} = 6.25 MHz	—	81	—	ns
t_L	Clock low time		—	81	—	ns
$t_{V(WS)}$	WS valid time	Master mode	—	3	—	ns
$t_{H(WS)}$	WS hold time	Master mode	—	3	—	ns
$t_{SU(WS)}$	WS setup time	Slave mode	0	—	—	ns
$t_{H(WS)}$	WS hold time	Slave mode	2	—	—	ns
$Ducy_{(SCK)}$	I2S slave input clock duty cycle	Slave mode	—	50	—	%
$t_{SU(SD\_MR)}$	Data input setup time	Master mode	2	—	—	ns
$t_{SU(SD\_SR)}$	Data input setup time	Slave mode	0	—	—	ns
$t_{H(SD\_MR)}$	Data input hold time	Master receiver	0	—	—	ns
$t_{H(SD\_SR)}$		Slave receiver	1	—	—	ns
$t_{V(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	—	—	9	ns
$t_{H(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	3	—	—	ns
$t_{V(SD\_MT)}$	Data output valid time	Master transmitter (after enable edge)	—	—	9	ns
$t_{H(SD\_MT)}$	Data output hold time	Master transmitter (after enable edge)	0	—	—	ns

(1) Based on characterization, not tested in production.

Figure 4-7. I2S timing diagram - master mode

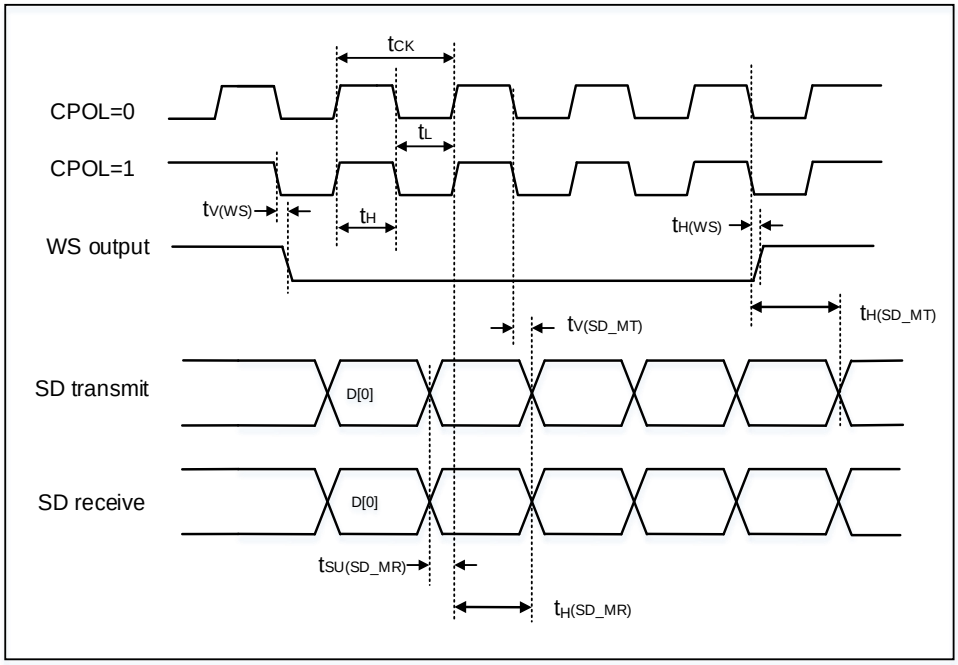
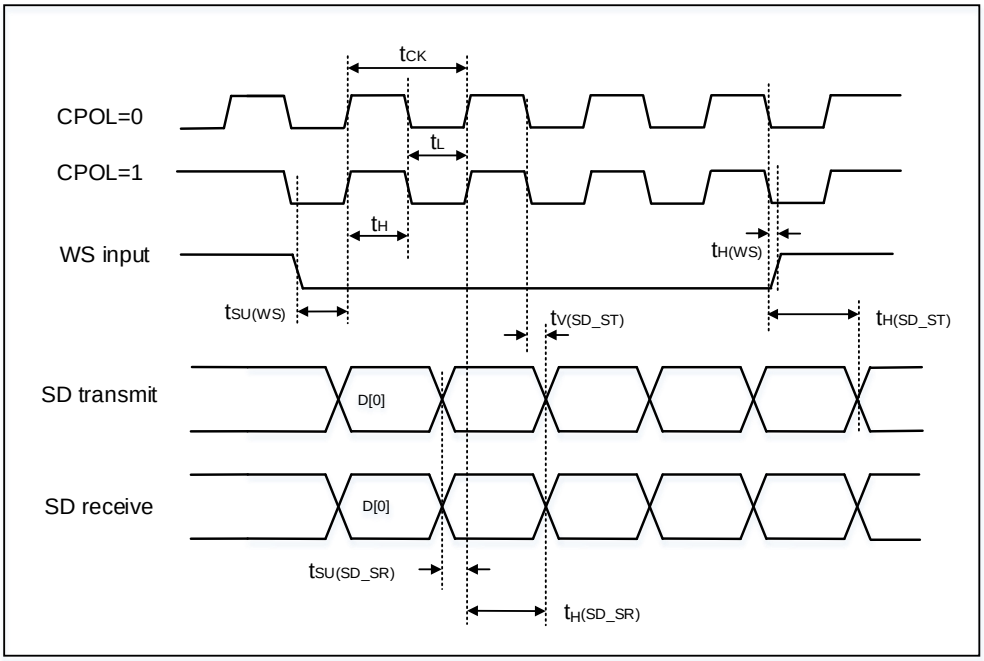


Figure 4-8. I2S timing diagram - slave mode



4.18. USART characteristics

Table 4-35. USART characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	f_{PCLKx} = 45 MHz	—	—	22.5	MHz
$t_{SCK(H)}$	SCK clock high time	f_{PCLKx} = 45 MHz	22.22	—	—	ns
$t_{SCK(L)}$	SCK clock low time	f_{PCLKx} = 45 MHz	22.22	—	—	ns

(1) Guaranteed by design, not tested in production.

4.19. SDIO characteristics

Table 4-36. SDIO characteristics (1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}(3)	Clock frequency in data transfer mode	—	0	—	48	MHz
$t_{W(CKL)}$(3)	Clock low time	f_{pp} = 48 MHz	10.5	11	—	ns
$t_{W(CKH)}$(3)	Clock high time	f_{pp} = 48 MHz	9.5	10	—	ns
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t_{ISU}(4)	Input setup time HS	f_{pp} = 48 MHz	4	—	—	ns
t_{IH}(4)	Input hold time HS	f_{pp} = 48 MHz	3	—	—	ns
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t_{OV}(3)	Output valid time HS	f_{pp} = 48 MHz	—	—	13.8	ns
t_{OH}(3)	Output hold time HS	f_{pp} = 48 MHz	12	—	—	ns
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}(4)	Input setup time SD	f_{pp} = 24 MHz	3	—	—	ns
t_{IHD}(4)	Input hold time SD	f_{pp} = 24 MHz	3	—	—	ns
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}(3)	Output valid default time SD	f_{pp} = 24 MHz	—	2.4	2.8	ns
t_{OHD}(3)	Output hold default time SD	f_{pp} = 24 MHz	0.8	—	—	ns

(1) CLK timing is measured at 50% of V_{DD}.

(2) Capacitive load C_L = 30 pF.

(3) Based on characterization, not tested in production.

(4) Guaranteed by design, not tested in production

4.20. USBFS characteristics

Table 4-37. USBFS start up time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USBFS startup time	1	µs

(1) Guaranteed by design, not tested in production.

Table 4-38. USBFS DC electrical characteristics

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
Input levels(1)	V_{DD}	USBFS operating voltage	—	3	—	3.6	V
	V_{DI}	Differential input sensitivity	—	0.2	—	—	
	V_{CM}	Differential common mode range	Includes V_{DI} range	0.8	—	2.5	
	V_{SE}	Single ended receiver threshold	—	1.3	—	2.0	
Output levels (2)	V_{OL}	Static output level low	R_L of 1.0 kΩ to 3.6 V	—	0.002	0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to GND	2.8	3.48	3.6	
R_{PD}(2)		PB13, PB12(USBFS_DM/DP)	V_{IN} = V_{DD}	17	19.02	24	kΩ
		PB14(USBFS_VBUS)		0.65	—	2.0	
R_{PU}(2)		PB13, PB12(USBFS_DM/DP)	V_{IN} = GND	1.5	1.589	2.1	
		PB14(USBFS_VBUS)		0.25	—	0.55	

(1) Guaranteed by design, not tested in production.

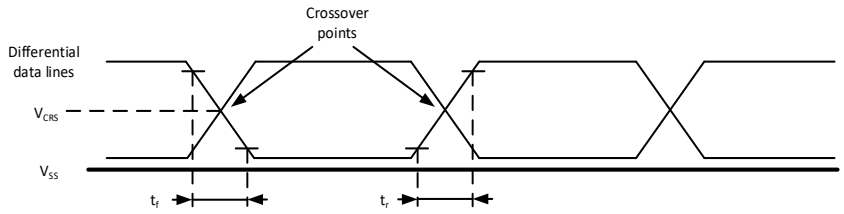
(2) Based on characterization, not tested in production.

Table 4-39. USBFS full speed-electrical characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_R	Rise time	CL = 50 pF	4	—	20	ns
t_F	Fall time	CL = 50 pF	4	—	20	ns
t_{RFM}	Rise / fall time matching	t_R / t_F	90	—	110	%
V_{CRS}	Output signal crossover voltage	—	1.3	—	2.0	V

(1) Guaranteed by design, not tested in production.

Figure 4-9. USBFS timings: definition of data signal rise and fall time



4.21. TIMER characteristics

Table 4-40. TIMER characteristics (1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{res}	Timer resolution time	—	1	—	t_{CK_TIMERx}
		f_{CK_TIMERx} = 180 MHz	5.56	—	ns
f_{EXT}	Timer external clock frequency	—	0	2*f_{CK_TIMERx}	MHz
		f_{CK_TIMERx} = 180 MHz	0	360	MHz
RES	Timer resolution	TIMERx except	—	16	bit

Symbol	Parameter	Conditions	Min	Max	Unit
		(TIMER1& TIMER2)			
		TIMER1& TIMER2	—	32	
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	—	1	65536	t_{CK_TIMERx}
		f_{CK_TIMERx} = 180 MHz	0.0056	364	μs
	32-bit counter clock period when internal clock is selected	—	1	65536x65536	t_{CK_TIMERx}
		f_{CK_TIMERx} = 180 MHz	—	23.9	s
t_{MAX_COUNT}	Maximum possible count (32-bit)	—	—	65536x65536	t_{CK_TIMERx}
		f_{CK_TIMERx} = 180 MHz	—	23.9	s

(1) Guaranteed by design, not tested in production.

4.22. WDGT characteristics

Table 4-41. FWDGT min/max timeout period at 32 kHz (IRC32K) (1)

Prescaler divider	PSC[2:0] bits	Min timeout RLD[11:0] =0x000	Max timeout RLD[11:0] = 0xFFF	Unit
1/4	000	0.03125	511.90625	ms
1/8	001	0.03125	1023.78125	
1/16	010	0.03125	2047.53125	
1/32	011	0.03125	4095.03125	
1/64	100	0.03125	8190.03125	
1/128	101	0.03125	16380.03125	
1/256	110 or 111	0.03125	32760.03125	

(1) Guaranteed by design, not tested in production.

Table 4-42. WWDGT min-max timeout value at 45 MHz (f_{PCLK1}) (1)

Prescaler divider	PSC[2:0]	Min timeout value CNT[6:0] = 0x40	Unit	Max timeout value CNT[6:0] = 0x7F	Unit
1/1	00	91.02	μs	5.83	ms
1/2	01	182.04		11.65	
1/4	10	364.09		23.30	
1/8	11	728.18		46.60	

(1) Guaranteed by design, not tested in production.

4.23. HPDF Characteristics

Table 4-43. HPDF characteristics (1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{HPDFCLK}$	HPDF clock	—	—	f_{APB2}	f_{SYSCLK}	MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CKIN} ($1 / T_{CKIN}$)	Input clock frequency	SPI mode(SITYP[1:0]=01)	—	—	20 ($f_{HPDFCLK}$ / 4)	
f_{CKOUT}	Output clock frequency	—	—	—	20	
$Duty_{CKOUT}$	Output clock frequency duty cycle	—	30	50	75	%
$t_{wh(CKIN)}$ $t_{wl(CKIN)}$	Input clock high and low time	SPI mode(SITYP[1:0]=01), External clock mode(SPICKSS[1:0]=0)	T_{CKIN} / 2-0.5	T_{CKIN} / 2	—	ns
t_{SU}	Data input setup time	SPI mode(SITYP[1:0]=01), External clock mode(SPICKSS[1:0]=0)	1	—	—	
t_h	Data input hold time	SPI mode(SITYP[1:0]=01), External clock mode(SPICKSS[1:0]=0)	1	—	—	
$T_{Manchester}$	Manchester data period(recovered clock period)	Manchester mode(SITYP[1:0]=10 or 11), Internal clock mode(SPICKSS[1:0]≠0)	(CKOUTDIV+1)*$T_{HPDFCLK}$	—	(2*CKOUTDIV)*$T_{HPDFCLK}$	

(1) Guaranteed by design, not tested in production.

(2) Output speed is set to OSPEEDRy[1:0]=10； Capacitive load C = 30 pF； Measurement points are done at COMS levels: 0.5*VDD.

4.24. Serial / Quad Parallel Interface (SQPI) Characteristics

Table 4-44. SQPI characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{CLK}(2)	CLK period	11.0(4)	—	—	ns
t_{CD}(2)	CLK high level duty for even clock divided	45	50	55	%
	CLK high level duty for odd clock divided	45	—	71	
t_{KHKL}(1)(3)	CLK rise or fall time	—	2.0	—	ns
t_{CPH}(2)	CE# high between subsequent burst operations	22.2	—	—	ns
t_{CEM}(2)	CE# low pulse width	88.8	—	—	ns
t_{CSP}(2)	CE# setup time to CLK rising edge	5.5	—	177.7	ns
t_{CHD}(2)	CE# hold time from CLK rising edge	5.5	—	177.7	ns
t_{SP}(2)	Setup time to active CLK edge	5.5	—	177.7	ns
t_{HD}(2)	Hold time from active CLK edge	5.5	—	177.7	ns
t_{HZ}(2)	CE# rise to data output high-Z	—	0	—	ns
t_{ACLK}(2)	CLK fall to data output valid delay	—	0	—	ns
t_{KOH}(2)	Data hold time from CLK falling edge	—	0	—	ns

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) Output driven mode is 50 MHz. Measured from 10% to 90% of VDD.
(4) This is designed minimal period. The operating minimal clock period is 22.2 ns (45 MHz = 180 MHz / 4).

4.25. Wi-Fi Radio characteristics

Below data are measured at antenna port of GD Wi-Fi Demo board.

Table 4-45. Transmitter power characteristics (1)(2)

Parameter	Rate	Typ	Unit
Tx Power	11b	21	dBm
	11g	18.3	
	11n, BW20M	17.3	
	11n, BW40M	17.3	

(1) Tx Power level is Limited by 802.11 Mask & EVM spec.
(2) Based on characterization, not tested in production.

Table 4-46. Receiver sensitivity characteristics (1)

Parameter	Rate	Typ	Unit
Rx Sensitivity	11b,1Mbps	-97.6	dBm
	11b,2Mbps	-94.4	
	11b,5.5Mbps	-92.1	
	11b,11Mbps	-87.6	
	11g,6Mbps	-94.3	
	11g,9Mbps	-92.5	

Parameter	Rate	Typ	Unit
	11g,12Mbps	-91.0	
	11g,18Mbps	-89.1	
	11g,24Mbps	-84.6	
	11g,36Mbps	-82.4	
	11g,48Mbps	-77.0	
	11g,54Mbps	-76.3	
	11n,HT20,MCS0	-94.0	
	11n,HT20,MCS1	-90.3	
	11n,HT20,MCS2	-88.5	
	11n,HT20,MCS3	-84.4	
	11n,HT20,MCS4	-82.0	
	11n,HT20,MCS5	-76.6	
	11n,HT20,MCS6	-75.6	
	11n,HT20,MCS7	-74.2	
	11n,HT40,MCS0	-89.6	
	11n,HT40,MCS1	-85.4	
	11n,HT40,MCS2	-83.5	
	11n,HT40,MCS3	-80.3	
	11n,HT40,MCS4	-77.9	
	11n,HT40,MCS5	-72.7	
	11n,HT40,MCS6	-71.8	
	11n,HT40,MCS7	-70.7	

(1) Based on characterization, not tested in production.

Table 4-47. Rx Maximum Input Level (1)(2)

Parameter	Rate	Typ	Unit
Rx Maximum Level Input	11b,1Mbps	>8.5(1)	dBm
	11b,11Mbps	>8.5(1)	
	11g,6Mbps	>8.5(1)	
	11g,54Mbps	4.6	
	11n,HT20,MCS0	>8.5(1)	
	11n,HT20,MCS7	3.7	
	11n,HT40,MCS0	5.2	
	11n,HT40,MCS7	3.7	

(1) IQxel VSG max TX power = 10 dBm, cable loss = 1.5 dB => max input power = 8.5 dBm.

(2) Based on characterization, not tested in production.

Table 4-48. Adjacent Channel Rejection [1][4]

Parameter	Rate	Typ		Unit
		Interference pattern by IQxel[2]	In-house interference pattern[3]	
Adjacent Channel Rejection	11b, 11Mbps	47.4	48	dB
	11g, 6Mbps	34.6	46	
	11g, 54Mbps	15.0	25	
	11n, HT20,MCS0	31.8	45	
	11n,HT20,MCS7	12.3	20	
	11n,HT40,MCS0	17.1	32	
	11n,HT40,MCS7	8.6	16	

(1) ACR result depends on interference source.

(2) Waveform generated by LitePoint IQxel series instrument, gap = SIFS

(3) Waveform generated by GD32W515xx baseband, gap = SIFS

(4) Based on characterization, not tested in production.

4.26. Parameter conditions

Unless otherwise specified, all values given for V_{DD} = V_{DDA} = AVDD33_ANA = AVDD33_PA = AVDD33_CLK = 3.3 V, T_A = 25 ℃.

5. Package information

5.1. QFN56 package outline dimensions

Figure 5-1. QFN56 package outline

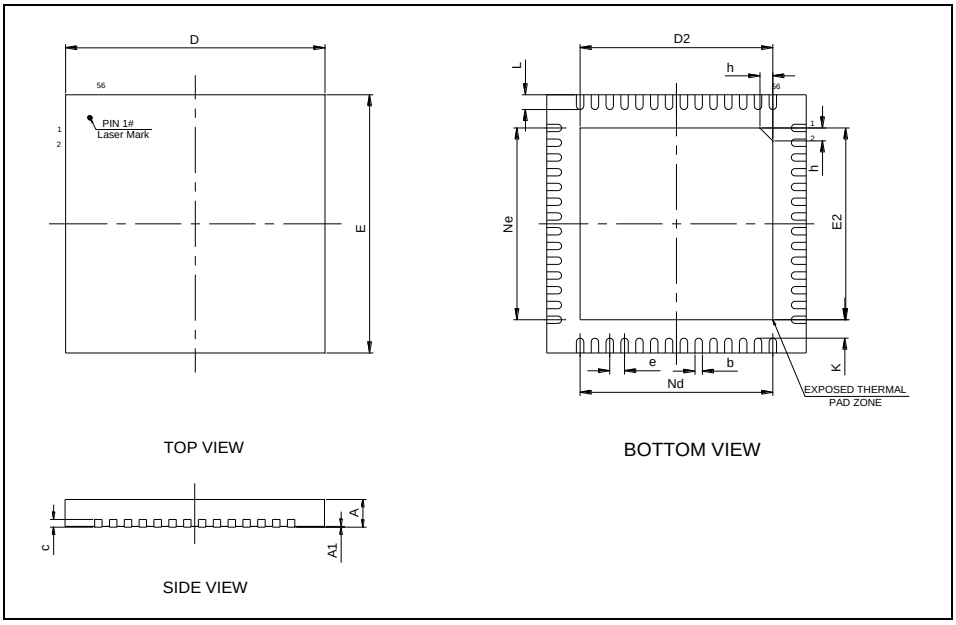
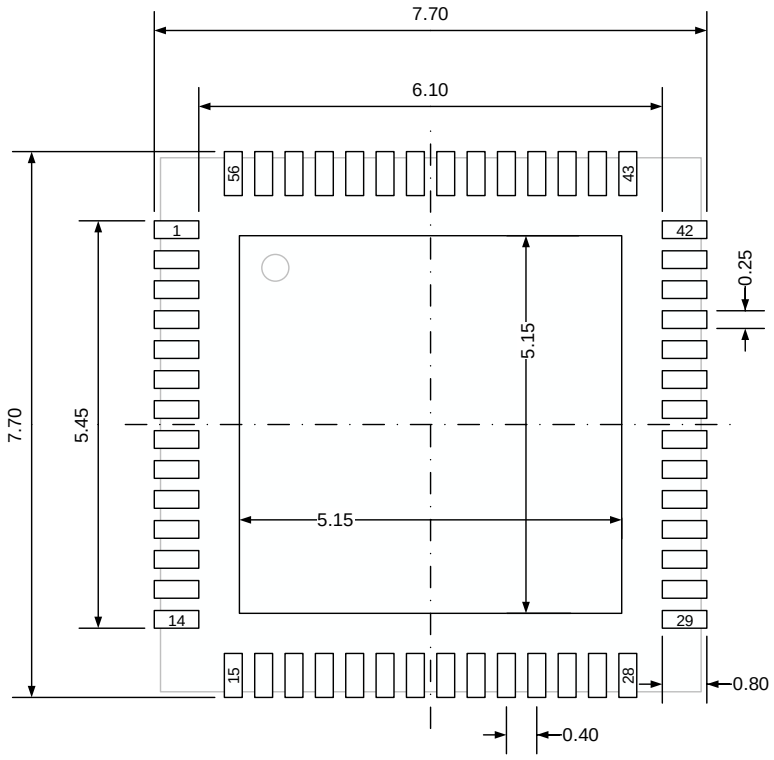


Table 5-1. QFN56 package dimensions

Symbol	Min	Typ	Max
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	6.90	7.00	7.10
D2	5.10	5.20	5.30
E	6.90	7.00	7.10
E2	5.10	5.20	5.30
e	—	0.40	—
h	0.30	0.35	0.40
K	0.20	—	—
L	0.35	0.40	0.45
Nd	—	5.20	—
Ne	—	5.20	—

(Original dimensions are in millimeters)

Figure 5-2. QFN56 recommended footprint



(Original dimensions are in millimeters)

5.2. QFN36 package outline dimensions

Figure 5-3. QFN36 package outline

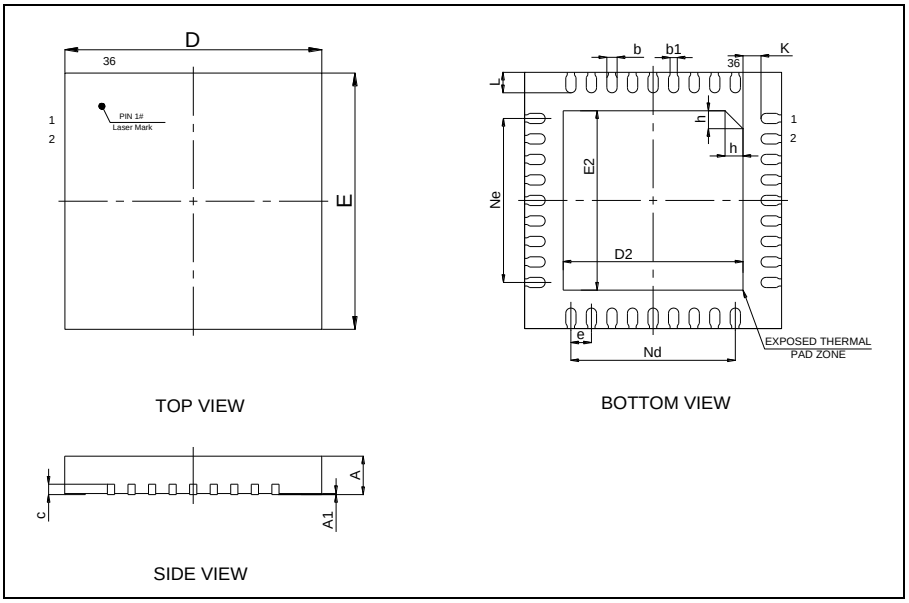
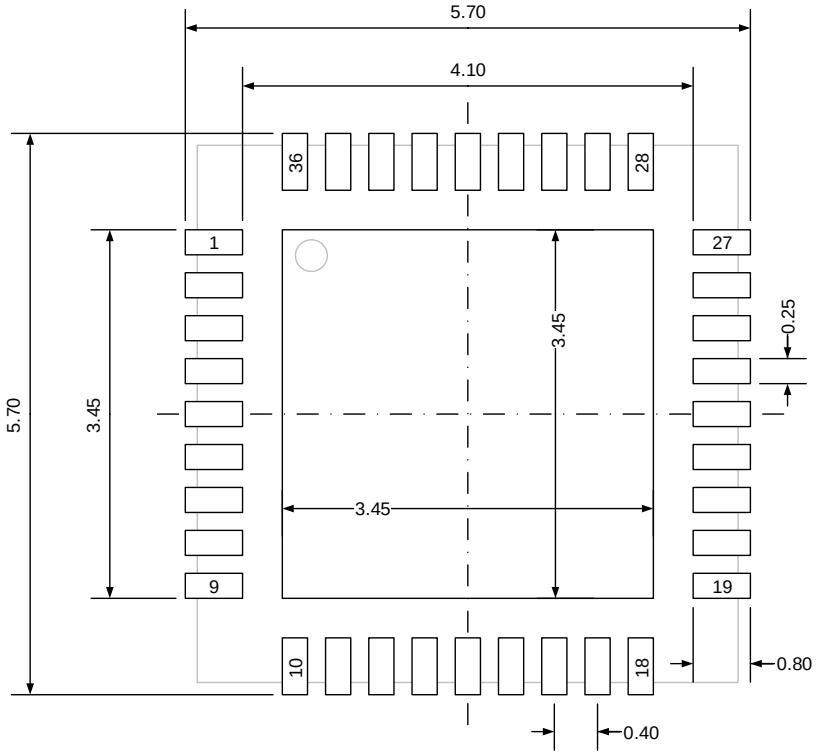


Table 5-2. QFN36 package dimensions

Symbol	Min	Typ	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1	—	0.14	—
c	—	0.203	—
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
e	—	0.40	—
h	0.30	0.35	0.40
K	—	0.35	—
L	0.35	0.40	0.45
Nd	—	3.20	—
Ne	—	3.20	—

(Original dimensions are in millimeters)

Figure 5-4. QFN36 recommended footprint



(Original dimensions are in millimeters)

5.3. Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter "θ". For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

θ_{JA}: Thermal resistance, junction-to-ambient.

θ_{JB}: Thermal resistance, junction-to-board.

θ_{JC}: Thermal resistance, junction-to-case.

Ψ_{JB}: Thermal characterization parameter, junction-to-board.

Ψ_{JT}: Thermal characterization parameter, junction-to-top center.

$$\theta_{JA}=(T_J-T_A)/P_D \quad (5\text{-}1)$$

$$\theta_{JB}=(T_J-T_B)/P_D \quad (5\text{-}2)$$

$$\theta_{JC}=(T_J-T_C)/P_D \quad (5\text{-}3)$$

Where, T_J = Junction temperature.

T_A = Ambient temperature

T_B = Board temperature

T_C = Case temperature which is monitoring on package surface

P_D = Total power dissipation

θ_{JA} represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower θ_{JA} can be considerate as better overall thermal performance. θ_{JA} is generally used to estimate junction temperature.

θ_{JB} is used to measure the heat flow resistance between the chip surface and the PCB board.

θ_{JC} represents the thermal resistance between the chip surface and the package top case. θ_{JC} is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

Table 5-3. Package thermal characteristics(1)

Symbol	Condition	Package	Value	Unit
θ_{JA}	Natural convection, 2S2P PCB	QFN56	38.32	°C/W
		QFN36	42.58	
θ_{JB}	Cold plate, 2S2P PCB	QFN56	17.23	°C/W
		QFN36	12.22	
θ_{JC}	Cold plate, 2S2P PCB	QFN56	13.28	°C/W
		QFN36	16.76	

Symbol	Condition	Package	Value	Unit
Ψ_{JB}	Natural convection, 2S2P PCB	QFN56	17.48	°C/W
		QFN36	12.81	
Ψ_{JT}	Natural convection, 2S2P PCB	QFN56	2.90	°C/W
		QFN36	0.69	

(1) Thermal characteristics are based on simulation, and meet JEDEC specification.

6. Ordering information

Table 6-1. Part ordering code for GD32W515xx devices

Ordering code	Flash (KB)	Package	Package type	Temperature operating range
GD32W515PIQ6	2048	QFN56	Green	Industrial -40 °C to +85 °C
GD32W515P0Q6	0	QFN56	Green	Industrial -40 °C to +85 °C
GD32W515TIQ6	2048	QFN36	Green	Industrial -40 °C to +85 °C
GD32W515TGQ6	1024	QFN36	Green	Industrial -40 °C to +85 °C

7. Revision history

Table 7-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Nov.23, 2021
1.1	1. Update the I2C characteristics in ***Table 7-2***. 2. Change the 16-bit general timers from five to four in chapter ***3.15***. 3. Delete TRACED0~3 in chapter 2.6, refers to ***Pin definitions***. 4. Update the I/O port DC characteristics in ***Table 7-3***. 5. Change the title of chapter ***3.2*** from Embedded memory to On-chip memory. 6. Add the pin definitions of USARTx_DE.	Jul.12, 2022
1.2	1. Add comments for ***Table 4-1***, ***Table 4-2*** and ***Table 4-7***. 2. Add BOOT pin USBFS (PB12/PB13/PB14). 3. Update ***Figure 4-4***. 4. Update PA14 to PA14-BOOT1 in chapter ***2.3*** and ***2.6***. 5. Change V_{DD} to VDD in chapter ***4.1***, ***4.2*** and ***4.4***.	Dec.28, 2022

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