



Rev. 1.2

# AS7C316098A

## 1024K X 16 BIT HIGH SPEED CMOS SRAM

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### REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issued	Jan.09. 2012
Rev. 1.1	Add 48 pin BGA package type.	Mar.12. 2012
Rev. 1.2	1."CE# $\geq V_{cc} - 0.2V$ " revised as "CE# $\leq 0.2$ " for TEST CONDITION of Average Operating Power supply Current Icc1 on page3 2.Revised <u>ORDERING INFORMATION</u> Page11	July.19. 2012

### FEATURES

- Fast access time : 10ns
- **low power consumption:**  
Operating current:  
90mA (typical)  
Standby current:  
4mA(Typical)
- Single 3.3V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control : LB# (DQ0 ~ DQ7)  
UB# (DQ8 ~ DQ15)
- Data retention voltage : 1.5V (MIN.)
- **Green package available**
- Package : 48-pin 12mm x 20mm TSOP-I  
48-ball 6mmx8mm TFBGA

### GENERAL DESCRIPTION

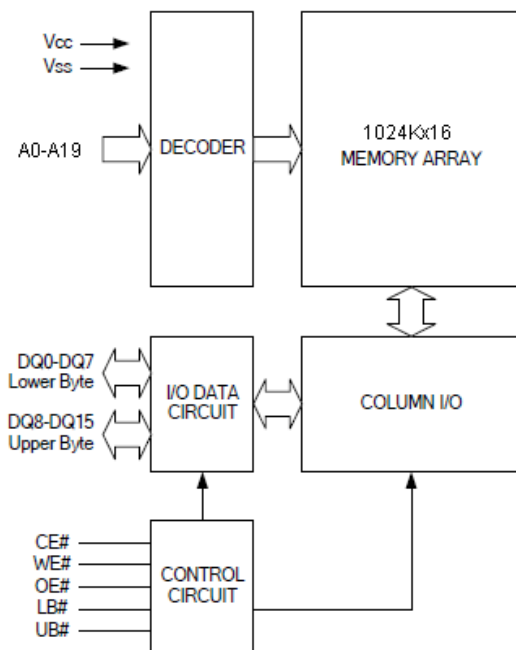
The AS7C316098A is a 16M-bit high speed CMOS static random access memory organized as 1024K words by 16 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The AS7C316098A operates from a single power supply of 3.3V and all inputs and outputs are fully TTL compatible

### PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(Isb1,TYP.)	Operating(Icc1,TYP.)
AS7C316098A(I)	-40 ~ 85°C	2.7 ~ 3.6V	10ns	4mA	90mA

### FUNCTIONAL BLOCK DIAGRAM



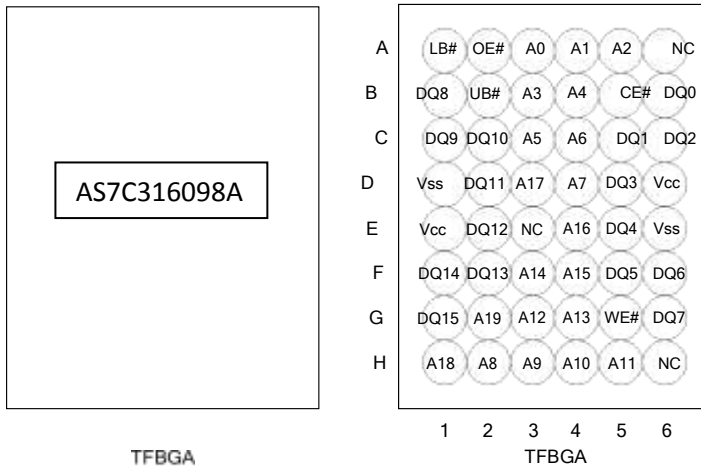
### PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A19	Address Inputs
DQ0 – DQ15	Data Inputs/Outputs
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
LB#	Lower Byte Control
UB#	Upper Byte Control
Vcc	Power Supply
Vss	Ground

### PIN CONFIGURATION



TSOP-I



TFBGA

TFBGA

### ABSOLUTE MAXIMUM RATINGS\*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on Vcc relative to Vss	V <sub>T1</sub>	-0.5 to 4.6	V
Voltage on any other pin relative to Vss	V <sub>T2</sub>	-0.5 to Vcc+0.5	V
Operating Temperature	T <sub>A</sub>	0 to 70(C grade)	°C
		-40 to 85(I grade)	
Storage Temperature	T <sub>STG</sub>	-65 to 150	°C
Power Dissipation	P <sub>D</sub>	1	W
DC Output Current	I <sub>OUT</sub>	50	mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

**TRUTH TABLE**

MODE	CE#	OE#	WE#	LB#	UB#	I/O OPERATION		SUPPLY CURRENT
						DQ0-DQ7	DQ8-DQ15	
Standby	H	X	X	X	X	High – Z	High – Z	I <sub>sb</sub> , I <sub>SB1</sub>
Output Disable	L	H	H	X	X	High – Z	High – Z	I <sub>cc</sub>
	L	X	X	H	H	High – Z	High – Z	
Read	L	L	H	L	H	D <sub>OUT</sub>	High – Z	I <sub>cc</sub>
	L	L	H	H	L	High – Z	D <sub>OUT</sub>	
	L	L	H	L	L	D <sub>OUT</sub>	D <sub>OUT</sub>	
Write	L	X	L	L	H	D <sub>IN</sub>	High – Z	I <sub>cc</sub>
	L	X	L	H	L	High – Z	D <sub>IN</sub>	
	L	X	L	L	L	D <sub>IN</sub>	D <sub>IN</sub>	

 Note: H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Don't care.

**DC ELECTRICAL CHARACTERISTICS**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. <sup>4</sup>	MAX.	UNIT	
Supply Voltage	V <sub>CC</sub>		2.7	3.3	3.6	V	
Input High Voltage	V <sub>IH</sub> <sup>1</sup>		2.2	-	V <sub>CC</sub> +0.3	V	
Input Low Voltage	V <sub>IL</sub> <sup>2</sup>		-0.3	-	0.8	V	
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> ≥ V <sub>IN</sub> ≥ V <sub>SS</sub>	-1	-	1	μA	
Output Leakage Current	I <sub>LO</sub>	V <sub>CC</sub> ≥ V <sub>OUT</sub> ≥ V <sub>SS</sub> , Output Disabled	-1	-	1	μA	
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -8mA	2.4	-	-	V	
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 4mA	-	-	0.4	V	
Average Operating Power supply Current	I <sub>CC</sub>	CE# = V <sub>IL</sub> , I <sub>I/O</sub> = 0mA ;f=max	-10	-	110	160	mA
	I <sub>CC1</sub>	CE# ≤ 0.2, Other pin is at 0.2V or V <sub>CC</sub> -0.2V I <sub>I/O</sub> = 0mA;f=max	-10	-	90	120	mA
Standby Power Supply Current	I <sub>SB</sub>	CE# ≥ V <sub>IH</sub> Other pin is at V <sub>IL</sub> or V <sub>IH</sub>	-	-	80	mA	
Standby Power Supply Current	I <sub>SB1</sub>	CE# ≥ V <sub>CC</sub> - 0.2V; Other pin is at 0.2V or V <sub>CC</sub> -0.2V	-	4	40	mA	

Notes:

- V<sub>IH</sub>(max) = V<sub>CC</sub> + 3.0V for pulse width less than 10ns.
- V<sub>IL</sub>(min) = V<sub>SS</sub> - 3.0V for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.  
Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub>(TYP.) and T<sub>A</sub> = 25 °C

**CAPACITANCE (T<sub>A</sub> = 25°C, f = 1.0MHz)**

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C <sub>IN</sub>	-	8	pF
Input/Output Capacitance	C <sub>I/O</sub>	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

**AC TEST CONDITIONS**

speed	10/12ns
Input Pulse Levels	0.2V to V <sub>cc</sub> -0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	V <sub>cc</sub> /2
Output Load	C <sub>L</sub> = 30pF + 1TTL, I <sub>OH</sub> /I <sub>OL</sub> = -8mA/4mA

**AC ELECTRICAL CHARACTERISTICS**
**(1) READ CYCLE**

PARAMETER	SYM.	AS7C316098A-10		UNIT
		MIN.	MAX.	
Read Cycle Time	t <sub>RC</sub>	10	-	ns
Address Access Time	t <sub>AA</sub>	-	10	ns
Chip Enable Access Time	t <sub>ACE</sub>	-	10	ns
Output Enable Access Time	t <sub>OE</sub>	-	4.5	ns
Chip Enable to Output in Low-Z	t <sub>CLZ</sub> *	2	-	ns
Output Enable to Output in Low-Z	t <sub>OLZ</sub> *	0	-	ns
Chip Disable to Output in High-Z	t <sub>CHZ</sub> *	-	4	ns
Output Disable to Output in High-Z	t <sub>OHZ</sub> *	-	4	ns
Output Hold from Address Change	t <sub>OH</sub>	2	-	ns
LB#, UB# Access Time	t <sub>BA</sub>	-	4.5	ns
LB#, UB# to High-Z Output	t <sub>BHZ</sub> *	-	4	ns
LB#, UB# to Low-Z Output	t <sub>BLZ</sub> *	0	-	ns

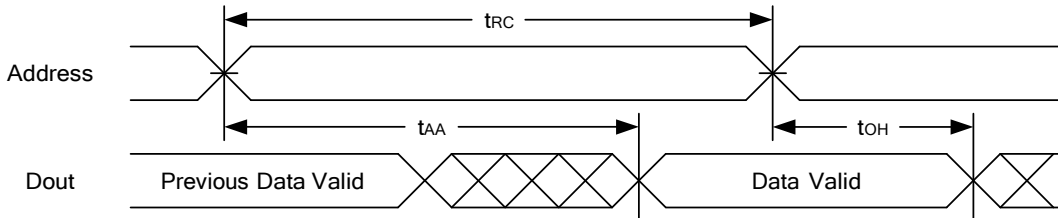
**(2) WRITE CYCLE**

PARAMETER	SYM.	AS7C316098A-10		UNIT
		MIN.	MAX.	
Write Cycle Time	t <sub>WC</sub>	10	-	ns
Address Valid to End of Write	t <sub>AW</sub>	8	-	ns
Chip Enable to End of Write	t <sub>CW</sub>	8	-	ns
Address Set-up Time	t <sub>AS</sub>	0	-	ns
Write Pulse Width	t <sub>WP</sub>	8	-	ns
Write Recovery Time	t <sub>WR</sub>	0	-	ns
Data to Write Time Overlap	t <sub>DW</sub>	6	-	ns
Data Hold from End of Write Time	t <sub>DH</sub>	0	-	ns
Output Active from End of Write	t <sub>OW</sub> *	2	-	ns
Write to Output in High-Z	t <sub>WHZ</sub> *	-	4	ns
LB#, UB# Valid to End of Write	t <sub>BW</sub>	8	-	ns

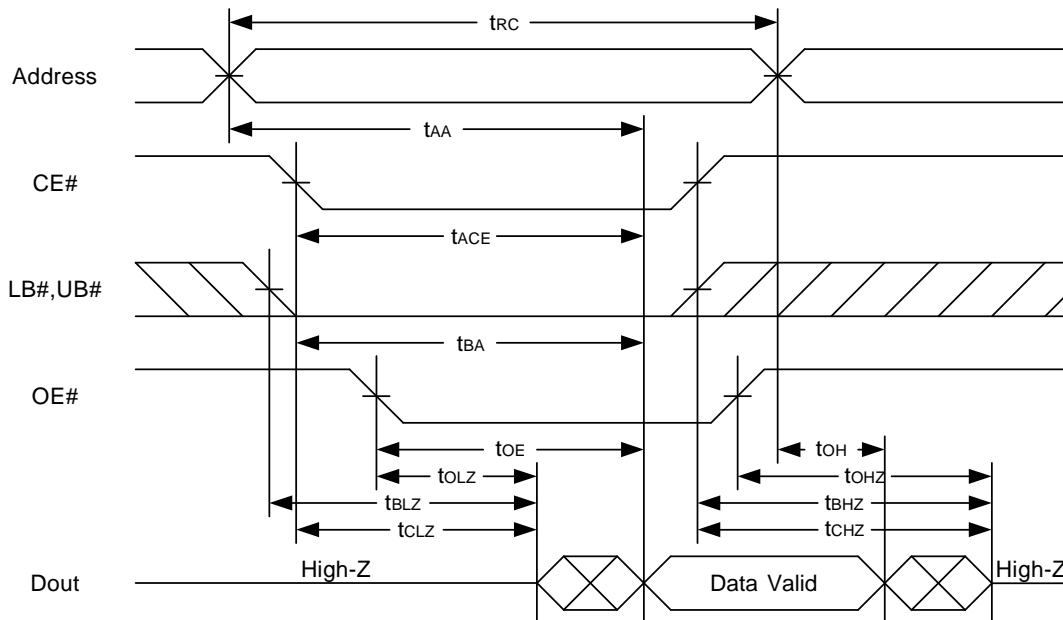
\*These parameters are guaranteed by device characterization, but not production tested.

## **TIMING WAVEFORMS**

### **READ CYCLE 1 (Address Controlled) (1,2)**

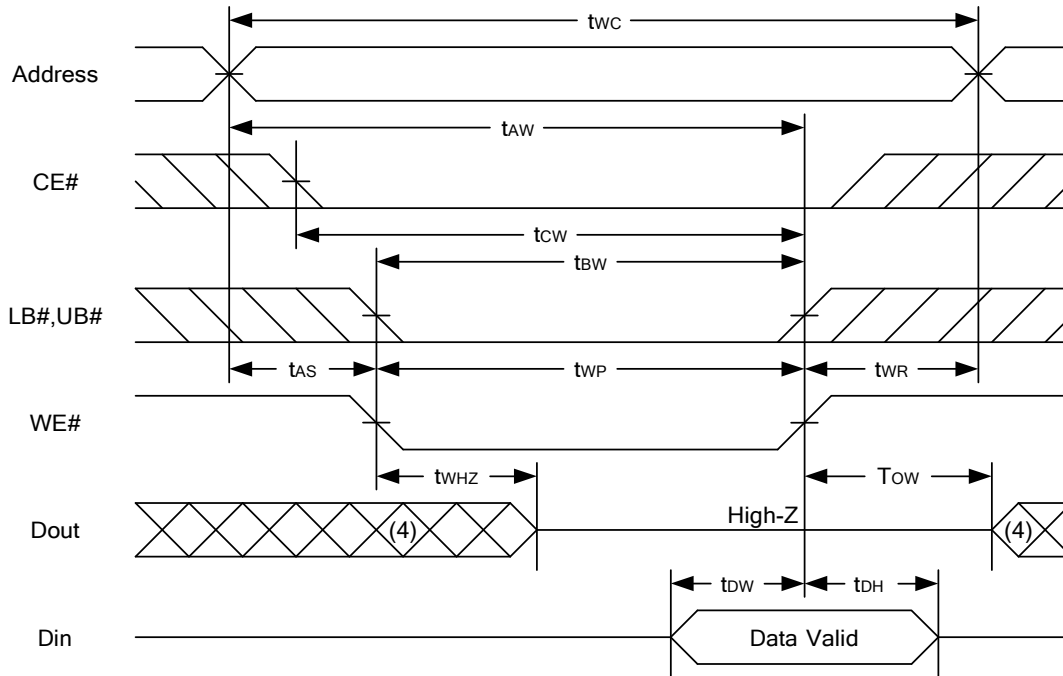
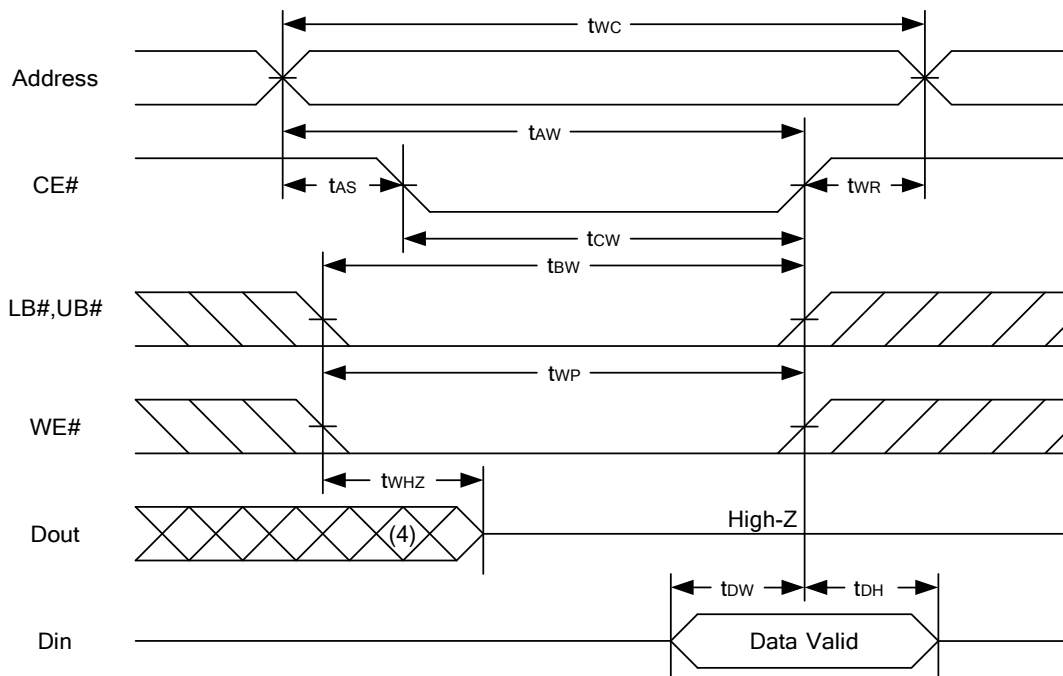


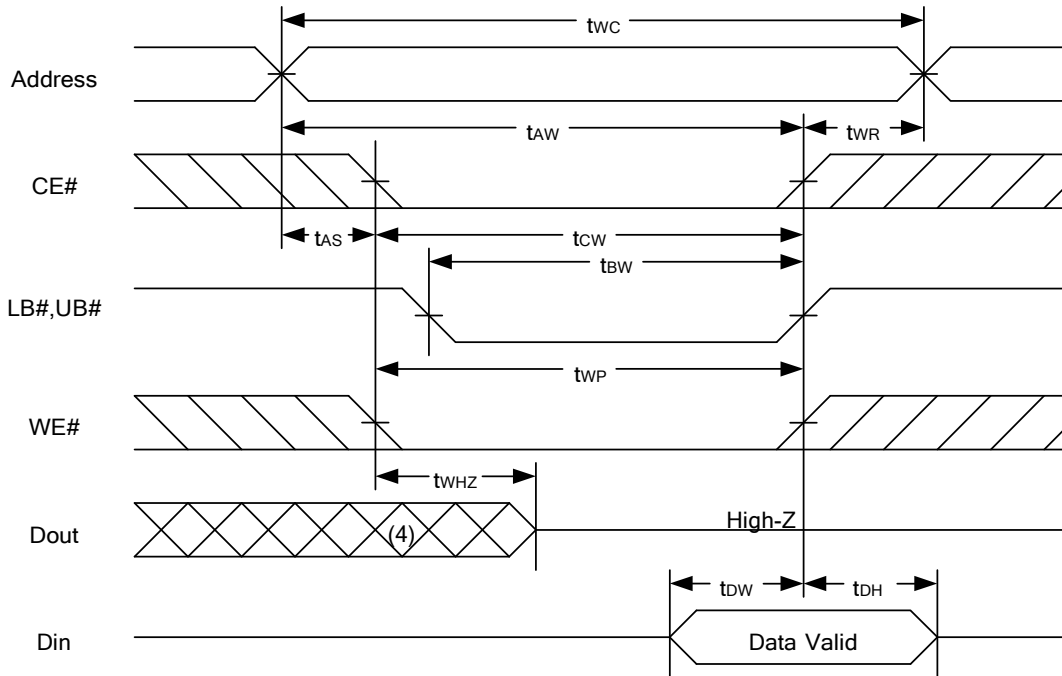
### **READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)**



**Notes :**

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, LB# or UB# = low.
3. Address must be valid prior to or coincident with CE# = low, LB# or UB# = low transition; otherwise tAA is the limiting parameter.
4. tCLZ, tBLZ, tOLZ, tCHZ, tBHZ and tOHZ are specified with CL = 5pF. Transition is measured ±500mV from steady state.
5. At any given temperature and voltage condition, tCHZ is less than tCLZ, tBHZ is less than tBLZ, tOHZ is less than tOLZ.

**WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)**

**WRITE CYCLE 2 (CE# Controlled) (1,2,5,6)**


**WRITE CYCLE 3 (LB#,UB# Controlled) (1,2,5,6)**

**Notes :**

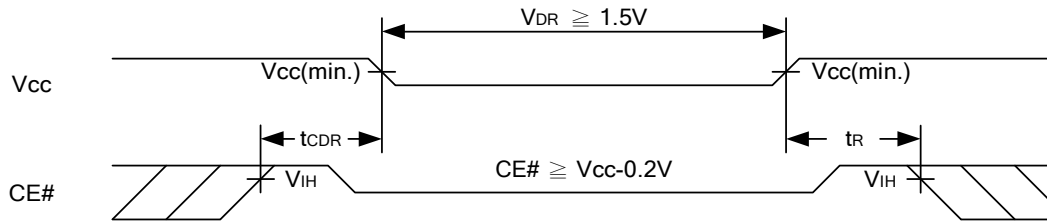
1. WE#, CE#, LB#, UB# must be high during all address transitions.
2. A write occurs during the overlap of a low CE#, low WE#, LB# or UB# = low.
3. During a WE# controlled write cycle with OE# low,  $t_{WP}$  must be greater than  $t_{WHZ} + t_{DW}$  to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE#, LB#, UB# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6.  $t_{DW}$  and  $t_{WHZ}$  are specified with  $C_L = 5\text{pF}$ . Transition is measured  $\pm 500\text{mV}$  from steady state.

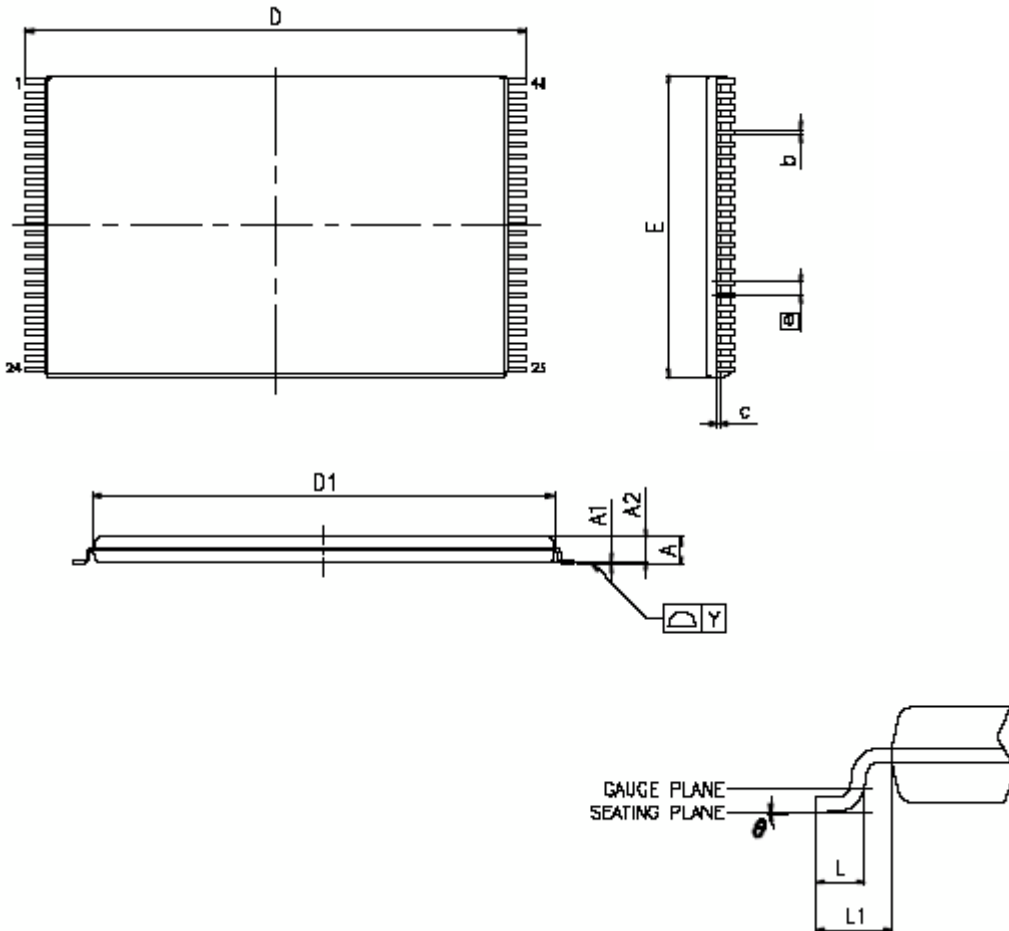


**DATA RETENTION CHARACTERISTICS**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V <sub>CC</sub> for Data Retention	V <sub>DR</sub>	CE# ≥ V <sub>CC</sub> - 0.2V	1.5	-	3.6	V
Data Retention Current	I <sub>DR</sub>	V <sub>CC</sub> = 1.5V CE# ≥ V <sub>CC</sub> - 0.2V; Other pin is at 0.2V or V <sub>CC</sub> -0.2V	-	4	40	mA
Chip Disable to Data Retention Time	t <sub>CDR</sub>	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t <sub>R</sub>		t <sub>RC*</sub>	-	-	ns

 t<sub>RC\*</sub> = Read Cycle Time

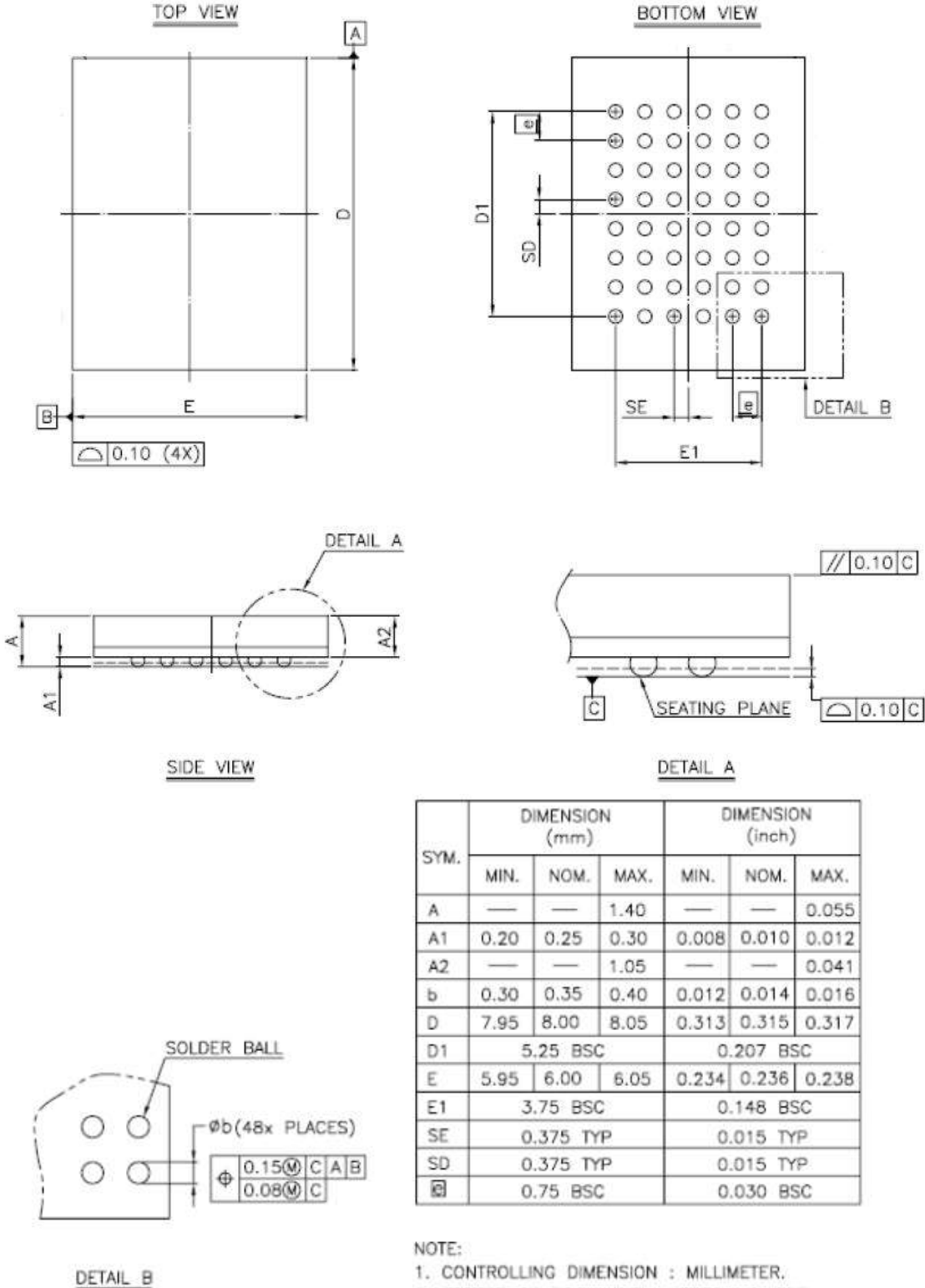
**DATA RETENTION WAVEFORM**


**PACKAGE OUTLINE DIMENSION**
**48-pin 12mm x 20mm TSOP-I Package Outline Dimension**

**VARIATIONS (ALL DIMENSIONS SHOWN IN MM)**

SYMBOLS	MIN.	NOM.	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.10	-	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	11.90	12.00	12.10
e	0.50 BASIC		
L	0.50	0.60	0.70
L1	-	0.80	-
Y	-	-	0.10
θ	0°	-	5°

**NOTES:**

- 1 JEDEC OUTLINE : MO-142 DD
2. PROFILE TOLERANCE ZONES FOR D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

**48-ball 6mm x 8mm TFBGA Package Outline Dimension**


**ORDERING INFORMATION**

<b>Alliance</b>	<b>Organization</b>	<b>VCC Range</b>	<b>Package</b>	<b>Operating Temp</b>	<b>Speed ns</b>
AS7C316098A-10TIN	1024K x 16	2.7 ~ 3.6V	48 pin TSOP-I	Industrial (-40 ~ 85°C)	10
AS7C316098A-10BIN	1024K x 16	2.7 ~ 3.6V	48 ball TFBGA 6mm x 8mm	Industrial (-40 ~ 85°C)	10



Rev. 1.2

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**1024K X 16 BIT HIGH SPEED CMOS SRAM**

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