

**1024K X 8 BIT SUPER LOW POWER CMOS SRAM**

Revision History**1024K x 8 BIT SUPER LOW POWER CMOS SRAM**

Revision	Details	Date
Rev 1.0	Initial Release	Jan 2008
Rev 1.1	Added I _{SB} Specs	May 2021



1024K X 8 BIT SUPER LOW POWER CMOS SRAM

FEATURES

- Fast access time : 55ns
- Low power consumption:
 Operating current : 30mA (TYP.)
 Standby current : 6µA (TYP.)
- Single 2.7V ~ 5.5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 1.5V (MIN.)
- Lead free and green package available
- Package : 44-pin 400 mil TSOP-II
 48-ball 6mm x 8mm TFBGA

GENERAL DESCRIPTION

The AS6C8008 is a 8,388,608-bit low power CMOS static random access memory organized as 1,048,576 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

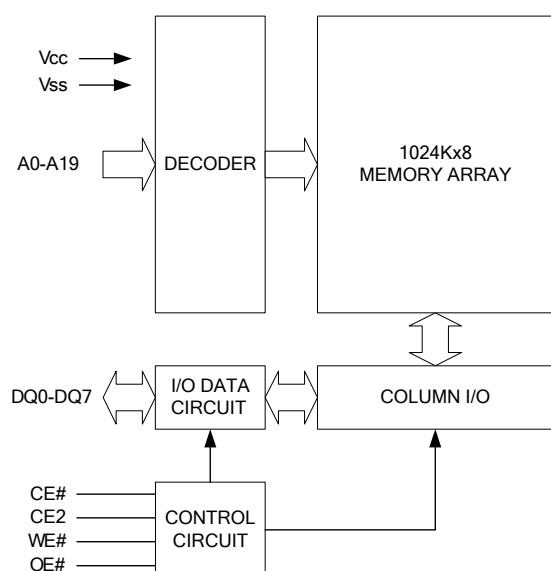
The AS6C8008 is well designed for very low power system applications, and particularly well suited for battery back-up nonvolatile memory application.

The AS6C8008 operates from a single power supply of 2.7V ~ 5.5V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(I _{SB1} ,TYP.)	Operating(I _{CC} ,TYP.)
AS6C8008	-40 ~ 85°C	2.7 ~ 5.5V	55ns	6µA	30mA

FUNCTIONAL BLOCK DIAGRAM



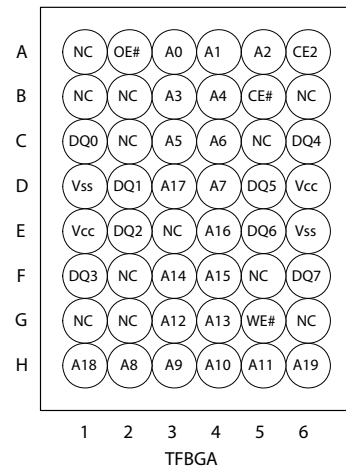
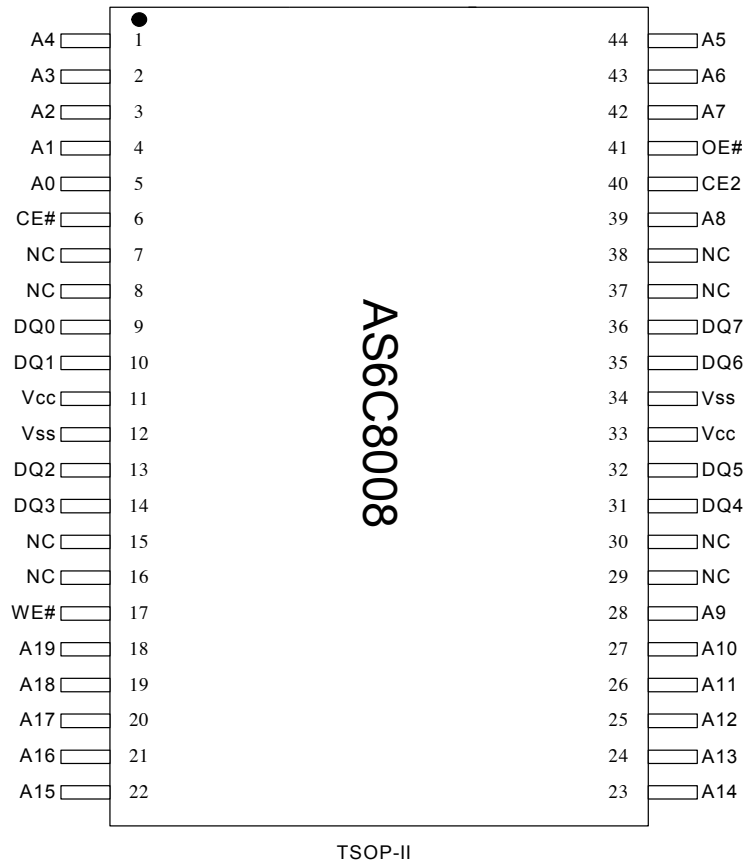
PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A19	Address Inputs
DQ0 - DQ7	Data Inputs/Outputs
CE#, CE2	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground
NC	No Connection



1024K X 8 BIT SUPER LOW POWER CMOS SRAM

PIN CONFIGURATION





1024K X 8 BIT SUPER LOW POWER CMOS SRAM

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V _{CC} relative to V _{SS}	V _{T1}	-0.5 to 6.5	V
Voltage on any other pin relative to V _{SS}	V _{T2}	-0.5 to V _{CC} +0.5	V
Operating Temperature	T _A	-40 to 85(I grade)	°C
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High-Z	I _{SB1}
	X	L	X	X	High-Z	I _{SB1}
Output Disable	L	H	H	H	High-Z	I _{CC} , I _{CC1}
Read	L	H	L	H	D _{OUT}	I _{CC} , I _{CC1}
Write	L	H	X	L	D _{IN}	I _{CC} , I _{CC1}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. ⁴	MAX.	UNIT
Supply Voltage	V _{CC}		2.7	3.0	5.5	V
Input High Voltage	V _{IH} ^{*1}	V _{CC} = 2.7 ~ 3.6V	2.2	-	V _{CC} +0.5	V
		V _{CC} = 4.5 ~ 5.5V	2.4	-	V _{CC} +0.5	V
Input Low Voltage	V _{IL} ^{*2}		-0.2	-	0.6	V
Input Leakage Current	I _{LI}	V _{CC} ≧ V _{IN} ≧ V _{SS}	-1	-	1	μA
Output Leakage Current	I _{LO}	V _{CC} ≧ V _{OUT} ≧ V _{SS} Output Disabled	-1	-	1	μA
Output High Voltage	V _{OH}	I _{OH} = -1mA	2.4	2.7	-	V
Output Low Voltage	V _{OL}	I _{OL} = 2mA	-	-	0.4	V
Average Operating Power supply Current	I _{CC}	Cycle time = Min. CE# = V _{IL} and CE2 = V _{IH} I _{IO} = 0mA Other pins at V _{IL} or V _{IH}	-55	30	60	mA
	I _{CC1}	Cycle time = 1μs CE# ≤ 0.2V and CE2 ≧ V _{CC} -0.2V I _{IO} = 0mA Other pins at 0.2V or V _{CC} -0.2V	-	4	12	mA
Standby Power Supply Current	I _{SB}	CE# = V _{IH} or CE2 = V _{IL} Other pins at V _{IL} or V _{IH}	-	0.15	2	mA
	I _{SB1}	CE# ≧ V _{CC} -0.2V or CE2 ≤ 0.2V Other pins at 0.2V or V _{CC} -0.2V	-	6	50	μA



1024K X 8 BIT SUPER LOW POWER CMOS SRAM

Notes:

1. $V_{IH(max)} = V_{CC} + 3.0V$ for pulse width less than 10ns.
2. $V_{IL(min)} = V_{SS} - 3.0V$ for pulse width less than 10ns.
3. Over/Undershoot specifications are characterized, not 100% tested.
4. Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at $V_{CC} = V_{CC(TYP.)}$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C$, $f = 1.0MHz$)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to $V_{CC} - 0.2V$
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 30pF + 1TTL$, $I_{OH}/I_{OL} = -1mA/2mA$

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	AS6C8008-55		UNIT
		MIN.	MAX.	
Read Cycle Time	t_{RC}	55	-	ns
Address Access Time	t_{AA}	-	55	ns
Chip Enable Access Time	t_{ACE}	-	55	ns
Output Enable Access Time	t_{OE}	-	30	ns
Chip Enable to Output in Low-Z	t_{CLZ}^*	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ}^*	5	-	ns
Chip Disable to Output in High-Z	t_{CHZ}^*	-	20	ns
Output Disable to Output in High-Z	t_{OHZ}^*	-	20	ns
Output Hold from Address Change	t_{OH}	10	-	ns

(2) WRITE CYCLE

PARAMETER	SYM.	AS6C8008-55		UNIT
		MIN.	MAX.	
Write Cycle Time	t_{WC}	55	-	ns
Address Valid to End of Write	t_{AW}	50	-	ns
Chip Enable to End of Write	t_{CW}	50	-	ns
Address Set-up Time	t_{AS}	0	-	ns
Write Pulse Width	t_{WP}	45	-	ns
Write Recovery Time	t_{WR}	0	-	ns
Data to Write Time Overlap	t_{DW}	25	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	ns
Output Active from End of Write	t_{OW}^*	5	-	ns
Write to Output in High-Z	t_{WHZ}^*	-	20	ns

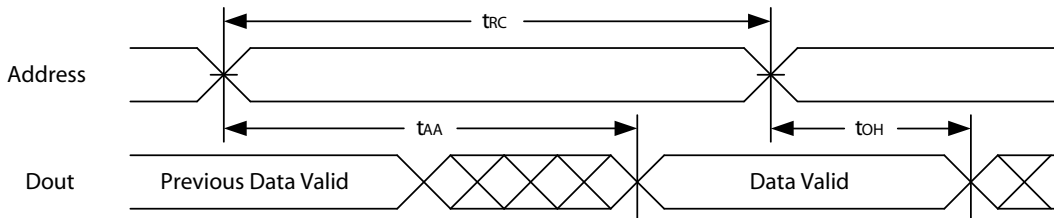
*These parameters are guaranteed by device characterization, but not production tested.



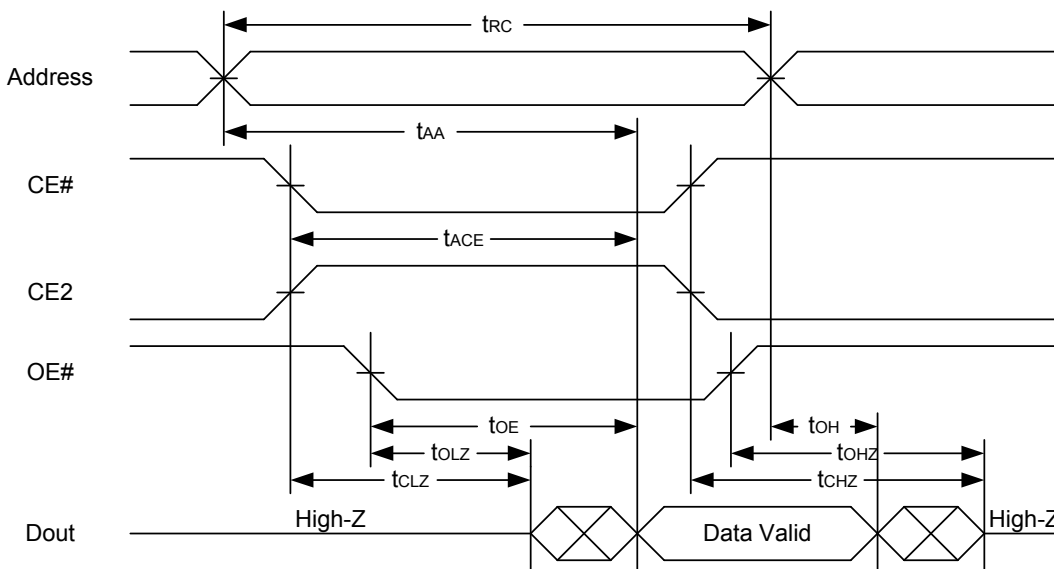
1024K X 8 BIT SUPER LOW POWER CMOS SRAM

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)



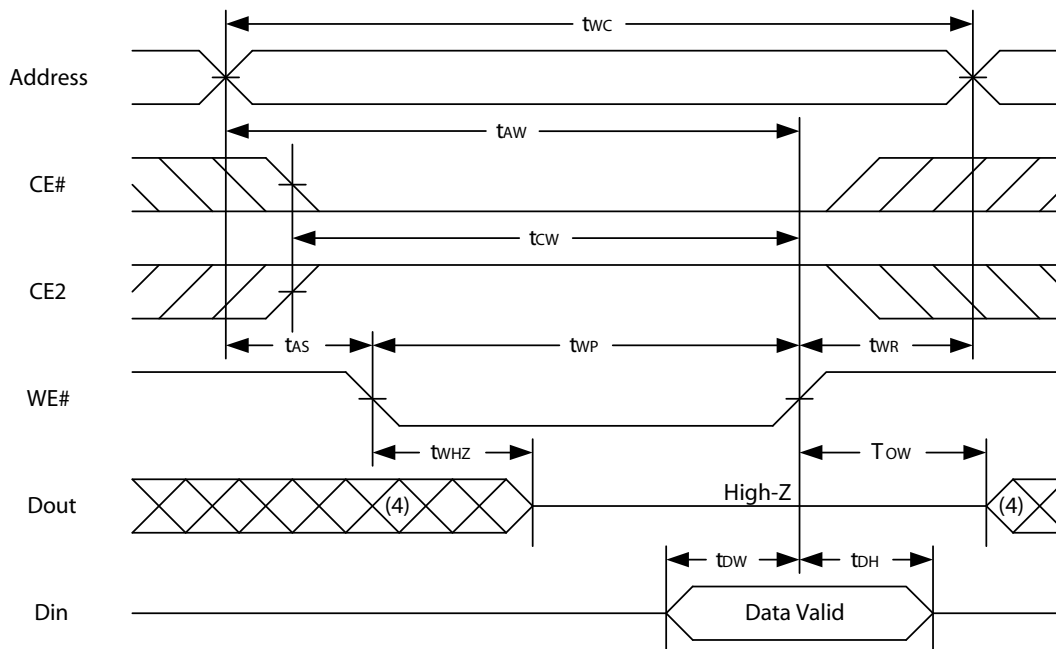
Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, CE2 = high.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{OLZ} , t_{CHZ} and t_{OHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ} .

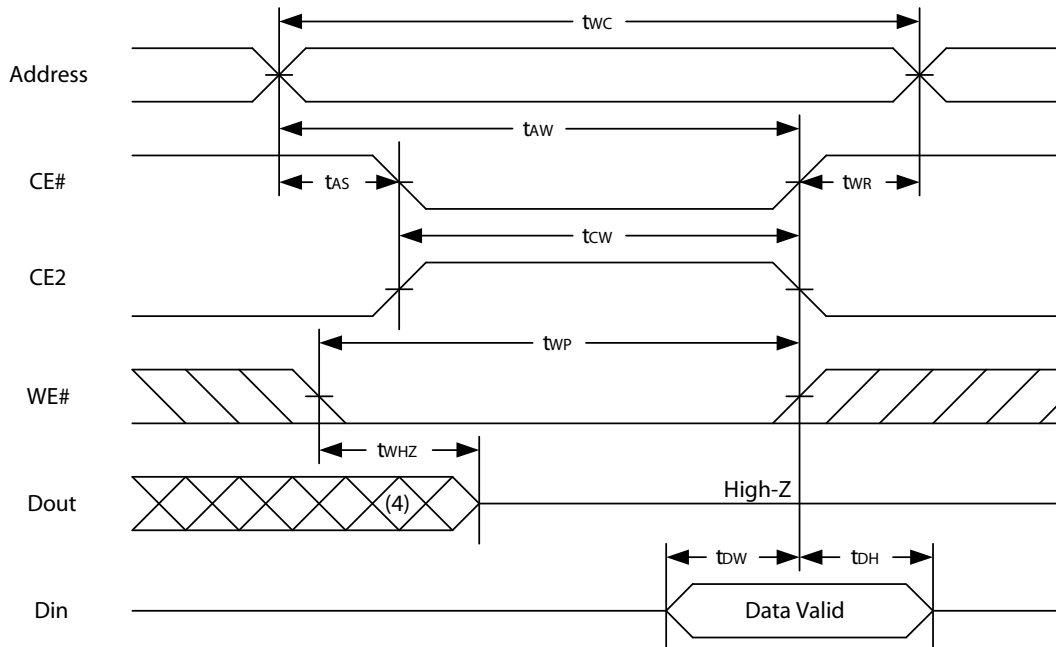


1024K X 8 BIT SUPER LOW POWER CMOS SRAM

WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)



WRITE CYCLE 2 (CE# and CE2 Controlled) (1,2,5,6)



Notes :

1. WE#, CE# must be high or CE2 must be low during all address transitions.
2. A write occurs during the overlap of a low CE#, high CE2, low WE#.
3. During a WE#-controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE#low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.



1024K X 8 BIT SUPER LOW POWER CMOS SRAM

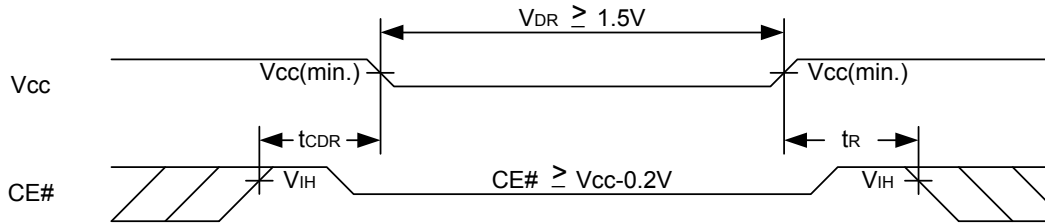
DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V _{CC} for Data Retention	V _{DR}	CE# ≥ V _{CC} - 0.2V or CE2 ≤ 0.2V	1.5	-	5.5	V
Data Retention Current	I _{DR}	V _{CC} = 1.5V CE# ≥ V _{CC} - 0.2V or CE2 ≤ 0.2V Other pins at 0.2V or V _{CC} - 0.2V	-	4	50	μA
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t _R		t _{RC*}	-	-	ns

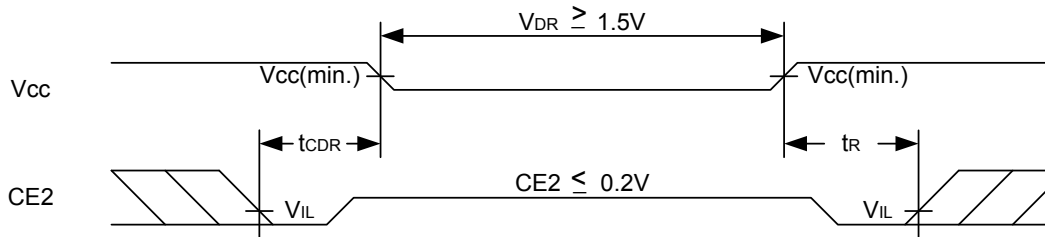
t_{RC*} = Read Cycle Time

DATA RETENTION WAVEFORM

Low V_{CC} Data Retention Waveform (1) (CE# controlled)



Low V_{CC} Data Retention Waveform (2) (CE2 controlled)

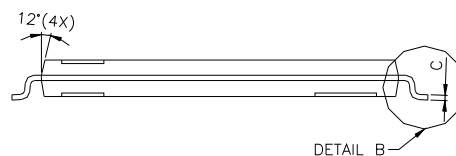
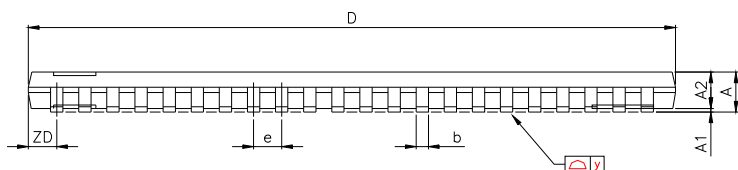
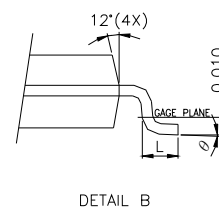
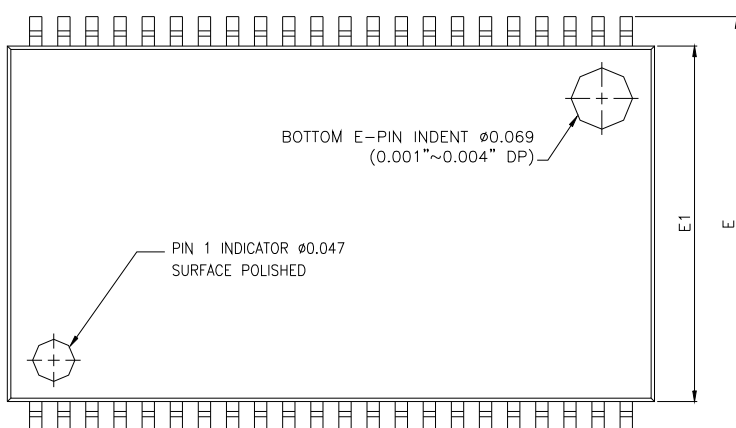




1024K X 8 BIT SUPER LOW POWER CMOS SRAM

PACKAGE OUTLINE DIMENSION

44-pin 400mil TSOP-II Package Outline Dimension

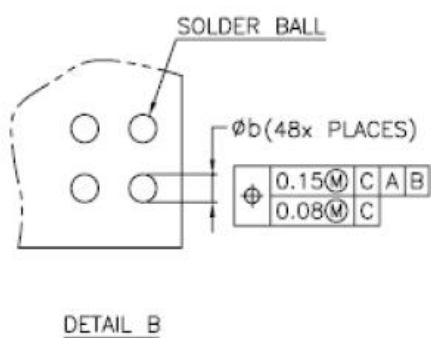
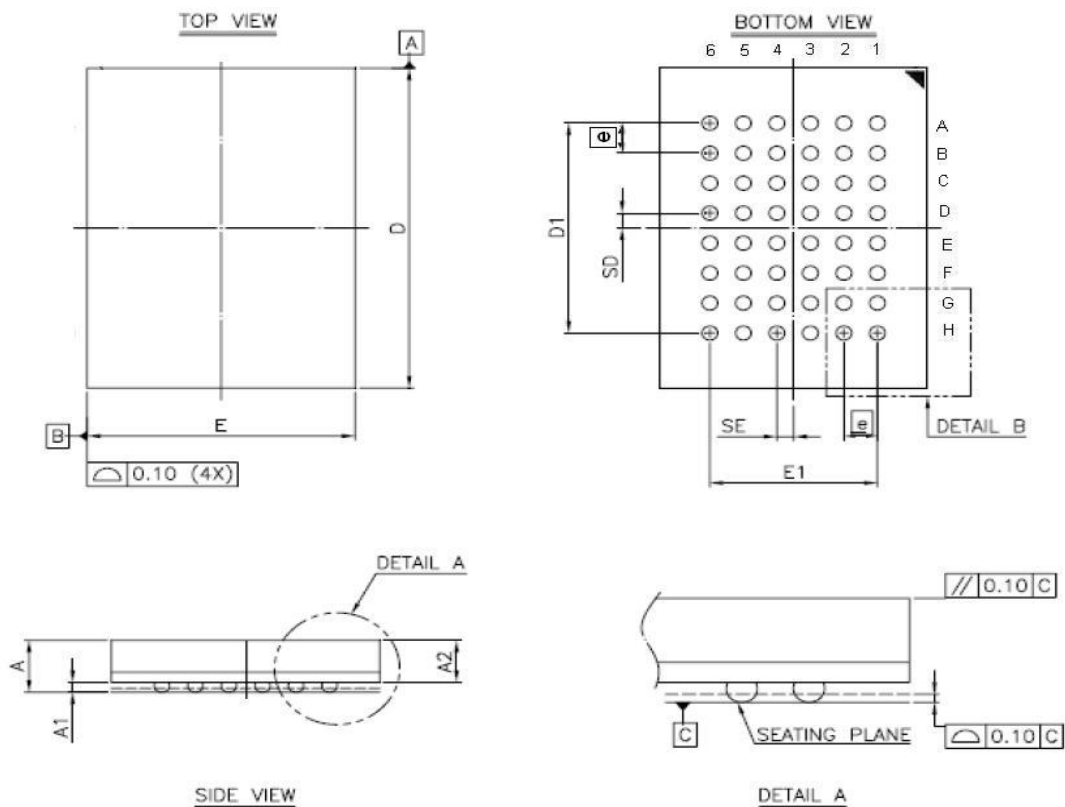


SYMBOLS	DIMENSIONS IN MILLMETERS			DIMENSIONS IN MILS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	47.2
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	0.95	1.00	1.05	37.4	39.4	41.3
b	0.30	-	0.45	11.8	-	17.7
c	0.12	-	0.21	4.7	-	8.3
D	18.212	18.415	18.618	717	725	733
E	11.506	11.760	12.014	453	463	473
E1	9.957	10.160	10.363	392	400	408
e	-	0.800	-	-	31.5	-
L	0.40	0.50	0.60	15.7	19.7	23.6
ZD	-	0.805	-	-	31.7	-
y	-	-	0.076	-	-	3
θ	0°	3°	6°	0°	3°	6°



1024K X 8 BIT SUPER LOW POWER CMOS SRAM

48-ball 6mm x 8mm TFBGA Package Outline Dimension



Symbol	DIMENSION (mm)			DIMENSION (inch)		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	1.40	-	-	0.055
A1	0.20	0.25	0.30	0.008	0.010	0.012
A2	-	-	1.05	-	-	0.041
b	0.30	0.35	0.40	0.012	0.014	0.016
D	7.95	8.00	8.05	0.313	0.315	0.317
D1	5.25 BSC			0.207 BSC		
E	5.95	6.00	6.05	0.234	0.236	0.238
E1	3.75 BSC			0.148 BSC		
SE	0.375 TYP			0.015 TYP		
SD	0.375 TYP			0.015 TYP		
e	0.75 BSC			0.030 BSC		

NOTE

1. Controlling Dimension : Millimeter
2. Reference Document : JEDEC MO-207



1024K X 8 BIT SUPER LOW POWER CMOS SRAM

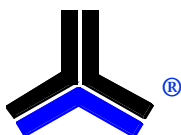
ORDERING INFORMATION

Alliance	Organization	VCC Range	Package	Operating Temp	Speed ns
AS6C8008-55ZIN	1024K x 8	2.7 - 5.5V	44pin TSOP II	Industrial ~ -40 C - 85 C	55
AS6C8008-55BIN	1024K x 8	2.7 - 5.5V	48ball TFBGA	Industrial ~ -40 C - 85 C	55

PART NUMBERING SYSTEM

AS6C	8008	-55	Z/B	I	N	XX
AS6C = Low Power SRAM prefix	Device Number 80 = 8Meg 08 = x 8 bit	Access Time 55 = 55ns	Package Option Z - 44pin TSOP B = 48ball TFBGA	I = Industrial Temp -40°C~ 85°C	Indicates Pb and Halogen Free	Packing Type None : Tray TR : Reel

**1024K X 8 BIT SUPER LOW POWER CMOS SRAM**



Alliance Memory, Inc.
12815 NE 124th st. STE#D,
Kirkland, WA 98034
Tel: 425-898-4456
Fax: 425-896-8628
www.alliancememory.com

Copyright © Alliance Memory
All Rights Reserved

© Copyright 2007 Alliance Memory, Inc. All rights reserved. Our three-point logo, our name and Intelliwatt are trademarks or registered trademarks of Alliance. All other brand and product names may be the trademarks of their respective companies. Alliance reserves the right to make changes to this document and its products at any time without notice. Alliance assumes no responsibility for any errors that may appear in this document. The data contained herein represents Alliance's best data and/or estimates at the time of issuance. Alliance reserves the right to change or correct this data at anytime, without notice. If the product described herein is under development, significant changes to these specifications are possible. The information in this product data sheet is intended to be general descriptive information for potential customers and users, and is not intended to operate as, or provide, any guarantee or warranty to any user or customer. Alliance does not assume any responsibility or liability arising out of the application or use of any product described herein, and disclaims any express or implied warranties related to the sale and/or use of Alliance products including liability or warranties related to fitness for a particular purpose, merchantability, or infringement of any intellectual property rights, except as expressly agreed to in Alliance's Terms and Conditions of Sale (which are available from Alliance). All sales of Alliance products are made exclusively according to Alliance's Terms and Conditions of Sale. The purchase of products from Alliance does not convey a license under any patent rights, copyrights; mask works rights, trademarks, or any other intellectual property rights of Alliance or third parties. Alliance does not authorize its products for use as critical components in life-supporting systems where a malfunction or failure may reasonably be expected to result in significant injury to the user, and the inclusion of Alliance products in such life-supporting systems implies that the manufacturer assumes all risk of such use and agrees to indemnify Alliance against all claims arising from such use.
