2X20W Stereo / 1X40W Mono Filter-less Digital Audio Amplifier With 2Vrms Line Driver

Features

- 16/18/20/24-bit input with I^2S, Left-alignment and Right-alignment data format
- PSNR & DR(A-weighting)
  Loudspeaker: 102dB (DR) @ 24V
- Multiple sampling frequencies (Fs)
  32kHz / 44.1kHz / 48kHz and
  64kHz / 88.2kHz / 96kHz and
  128kHz/176.4kHz/192kHz
- System clock = 64x, 128x, 256x, 384x, 512x, 768x, 1024x Fs
  256x~1024x Fs for 32kHz / 44.1kHz / 48kHz
  128x~512x Fs for 64kHz / 88.2kHz / 96kHz
  64x~256x Fs for 128kHz /176.4kHz/192kHz
- Supply voltage
  3.0~3.3V for digital circuit
  8V~26V for loudspeaker driver
- Loudspeaker output power for Stereo
  10W x 2ch into 8Ω @ 10% THD+N@13V
  15W x 2ch into 8Ω @ 10% THD+N@16V
- Sounds processing including:
  Volume control (+24dB~-103dB, 0.125dB/step)
  Dynamic range control
  Power clipping
  Channel mixing
  User programmed noise gate with hysteresis window
  DC-blocking high-pass filter
- Anti-pop design
- I^2C control interface with selectable device address
- Internal PLL
- Dynamic temperature control
- Short circuit and over-temperature protection
- LV Under-voltage shutdown and HV Under-voltage detection
- DC detection function
- Clock detection function
- Filter-less solution
- MCLK-less application

Applications

- TV audio
- Boom-box, CD and DVD receiver, docking system
- Powered speaker
- Wireless audio

Description

AD87010 is an integrated audio system solution, embedding digital audio processing, power stage amplifier, and a stereo 2Vrms line driver.

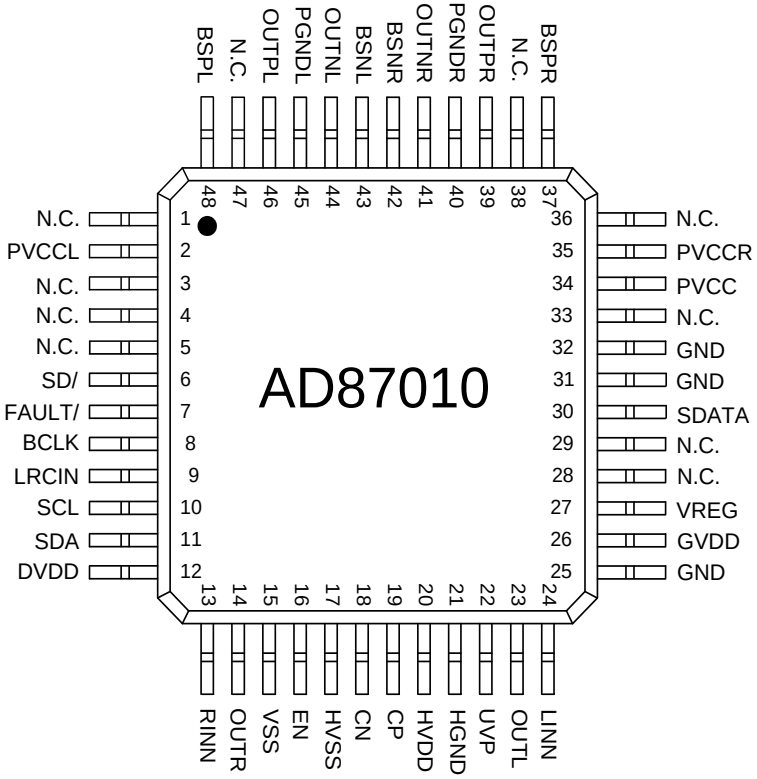
AD87010 is a digital audio amplifier capable of driving a pair of 8Ω,20W or a single 4Ω,40W speaker, both which operate with play music at a 24V supply.

Using I^2C digital control interface, the user can control AD87010's input format selection, mute and volume control functions. AD87010 has many built-in protection circuits to safeguard AD87010 from connection errors.

Ordering Information

Product ID	Package	Packing / MPQ	Comments
AD87010-LG48NRY	E-LQFP-48L (7x7 mm)	2.5K Units / Small Box (250 Units / Tray, 10 Trays / Small Box	Green

Pin Assignment (Top View)



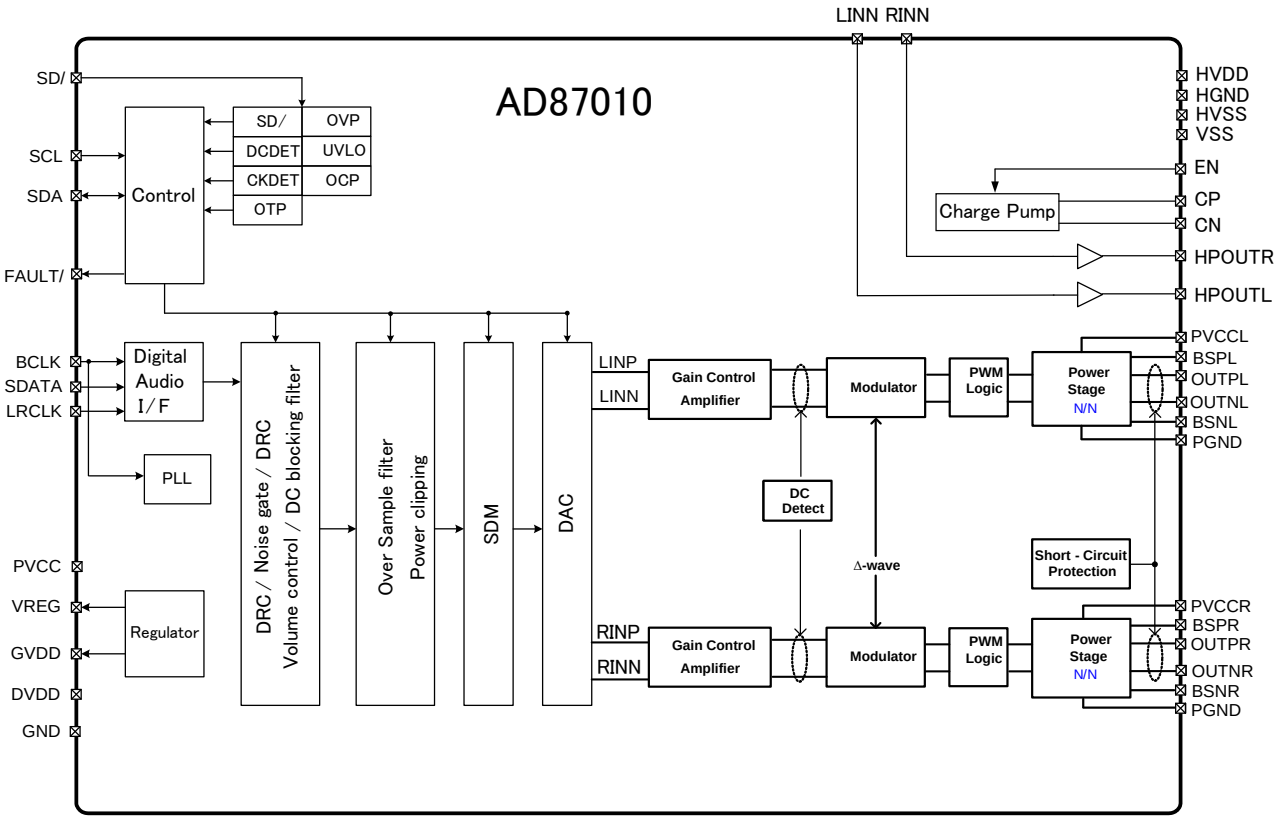
Pin Description

PIN	NAME	TYPE	DESCRIPTION	CHARACTERISTICS
1	N.C.		No connected.	
2	PVCCL	P	High voltage power supply for left-channel.	Right channel and left channel power supply inputs are connect internally.
3	N.C.		No connected.	
4	N.C.		No connected.	
5	N.C.		No connected.	
6	SD/	I	Shut down, low active.	
7	FAULT/	I/O	FAULT pin is a dual function pin. One is I^2C address setting during power up. The other one is error status report (low active), It sets by register of A_SEL_FAULT at address 0x02 B[7] to enable it.	Schmitt trigger TTL input buffer
8	BCLK	I	Bit clock input (64Fs).	Schmitt trigger TTL input buffer
9	LRCIN	I	Left/Right clock input (Fs).	Schmitt trigger TTL input buffer

10	SCL	I	I^2C serial clock input.	Schmitt trigger TTL input buffer
11	SDA	I/O	I^2C bi-directional serial data.	Schmitt trigger TTL input buffer
12	DVDD	P	Digital Power.	
13	RINN	I	Right input for line driver.	
14	OUTR	O	Right output for line driver.	
15	VSS	P	Ground for line driver.	
16	EN	I	Enable for line driver.	
17	HVSS	P	Supply voltage for line driver.	
18	CN	IO	Charge pump flying capacitor negative connection for line driver.	
19	CP	IO	Charge pump flying capacitor positive connection for line driver.	
20	HVDD	P	Supply voltage for line driver.	
21	HGND	P	Ground for line driver.	
22	UVP	I	Under voltage protection for line driver.	
23	OUTL	O	Left output for Line driver.	
24	LINN	I	Left input for Line driver.	
25	GND	P	Ground.	
26	GVDD	O	5V Regulator voltage output. This pin must not be used to drive external devices.	
27	VREG	O	1.8V Regulator voltage output.	
28	N.C.		No connected.	
29	N.C.		No connected.	
30	SDATA	I	Serial audio data input.	Schmitt trigger TTL input buffer
31	GND	P	Ground.	
32	GND	P	Ground.	
33	N.C.		No connected.	
34	PVCC	P	High-voltage power supply for internal GVDD regulator.	
35	PVCCR	P	High-voltage power supply for right-channel.	Right channel and left channel power supply inputs are connect internally.
36	N.C.		No connected.	
37	BSPR	P	Bootstrap I/O for right channel, positive high side FET.	
38	N.C.		No connected.	

39	OUTPR	O	Class-D H-bridge positive output for right channel.	
40	PGNDR	P	Power ground for the H-bridges.	
41	OUTNR	O	Class-D H-bridge negative output for right channel.	
42	BSNR	P	Bootstrap I/O for right channel, negative high side FET.	
43	BSNL	P	Bootstrap I/O for left channel, negative high side FET.	
44	OUTNL	O	Class-D H-bridge negative output for left channel.	
45	PGNDL	P	Power ground for the H-bridges.	
46	OUTPL	O	Class-D H-bridge positive output for left channel.	
47	N.C.		No connected.	
48	BSPL	P	Bootstrap I/O for left channel, positive high side FET.	

Functional Block Diagram



Available Package

Package Type	Device No.	θ_{ja}(℃/W)	θ_{jt} (℃/W)	Ψ_{jb} (℃/W)	Exposed Thermal Pad
E-LQFP-48L (7X7)	AD87010	22.9	34.9	1.64	(Note1)

Note 1.1: The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is suggested.

Note 1.2: θ_{ja} is measured on a room temperature (T_A=25℃), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The measurement is tested using the JEDEC51-5 thermal measurement standard.

Note 1.3: θ_{jt} represents the heat resistance for the heat flow between the chip and the package's top surface. (The junction-to-top thermal resistance is obtained by simulating a cold plate test on the top of the package).

Note 1.4: Ψ_{jb} represents the heat resistance for the heat flow between the chip and the exposed pad center. (The junction-to-top characterization parameter is extracted from the simulation data to obtainθ_{ja}).

Absolute Maximum Ratings

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device.

Symbol	Parameter	Min	Max	Units
DVDD	Supply for Digital Circuit	-0.3	3.6	V
HVDD	Supply for Line Driver	-0.3	3.6	V
PVCC	Supply for Internal Regulator	-0.3	30	V
PVCCL/R	Supply for Class-D Driver Stage	-0.3	30	V
V_i	Input Voltage	-0.3	3.6	V
T_{stg}	Storage Temperature	-65	150	^oC
T_J	Junction Operating Temperature	-40	150	^oC
R_L	BTL: PVCC ＞ 13V	4.8		Ω
	BTL: PVCC ≦ 13V	3.2		
	PBTL	3.2		
ESD	Human Body Model		±2K	V
	Machine Model		±200	

Recommended Operating Conditions

Symbol	Parameter	Typ.	Units
DVDD	Supply for Digital Circuit	3.15~3.45	V
HVDD	Supply for Line Driver	3.15~3.45	V
PVCC	Supply for Internal Regulator	8~26	V
PVCCL/R	Supply for Class-D Driver Stage	8~26	V
T_J	Junction Operating Temperature	-40~125	^oC
T_A	Ambient Operating Temperature	-40~85	^oC

Marking Information

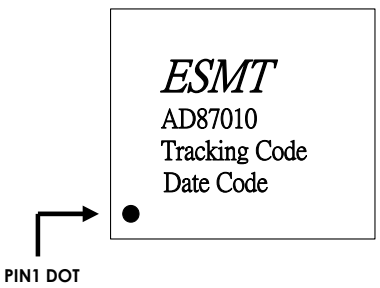
AD87010

Line 1 : LOGO

Line 2 : Product no.

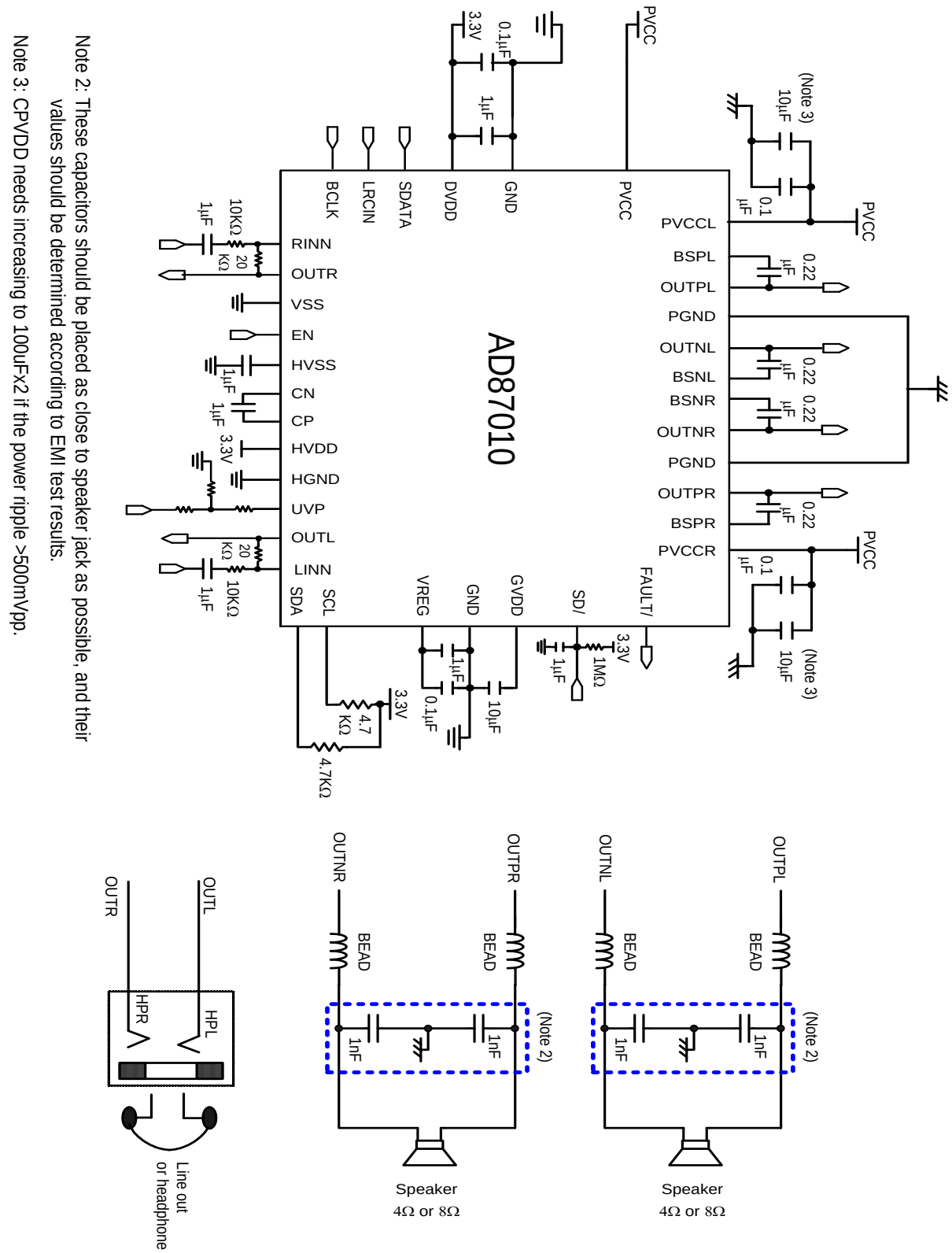
Line 3 : Tracking Code

Line 4 : Date Code



E-LQFP-48L

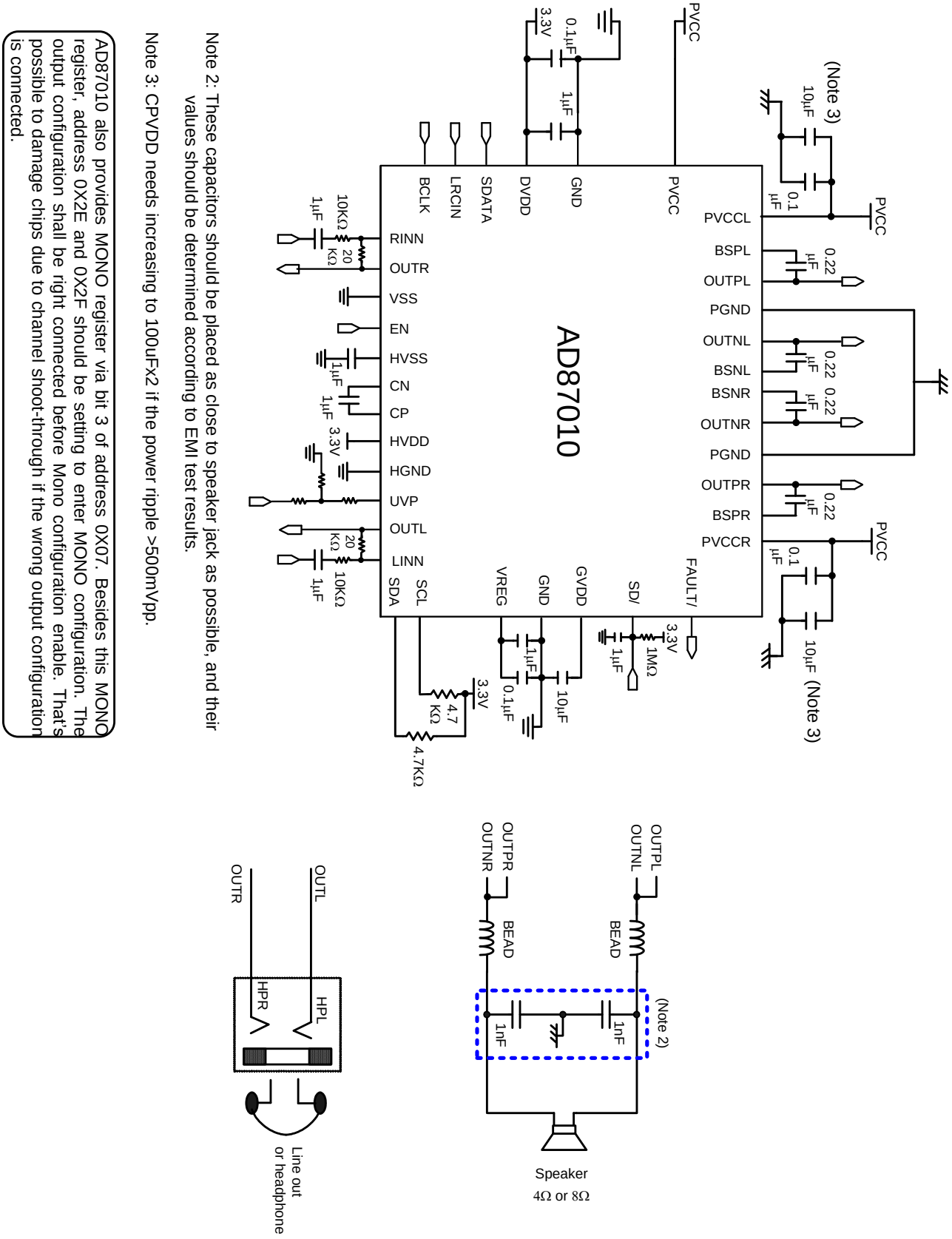
Application Circuit Example for Stereo



Note 2: These capacitors should be placed as close to speaker jack as possible, and their values should be determined according to EMI test results.

Note 3: CPVDD needs increasing to 100uFx2 if the power ripple >500mVpp.

Application Circuit Example for Mono



Note 2: These capacitors should be placed as close to speaker jack as possible, and their values should be determined according to EMI test results.

Note 3: CPVDD needs increasing to 100uFx2 if the power ripple >500mVpp.

AD87010 also provides MONO register via bit 3 of address 0X07. Besides this MONO register, address 0X2E and 0X2F should be setting to enter MONO configuration. The output configuration shall be right connected before Mono configuration enable. That's possible to damage chips due to channel shoot-through if the wrong output configuration is connected.

General Electrical Characteristics

Condition: T_A=25 °C (unless otherwise specified).

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{PD(PVCC)}$	PVCC Supply Current during Power Down	PVCC=24V		24	100	uA
$I_{PD(DVDD)}$	DVDD Supply Current during Shutdown	DVDD=3.3V			10	uA
$I_{PD(HVCC)}$	HVDD Supply Current during Shutdown	HVDD=3.3V			5	uA
$I_{Q(PVCC,24V)}$	PVCC Supply Current during standby	PVCC=24V		21		mA
$I_{Q(PVCC,12V)}$		PVCC=12V		17		mA
$I_{Q(DVDD)}$	Quiescent current for DVDD			70		mA
$I_{Q(HVDD)}$	Quiescent current for HVDD			7	15	mA
T_{SENSOR}	Junction Temperature for Driver Shutdown			160		°C
	Temperature Hysteresis for Recovery from Shutdown			35		°C
$DVDDUV_H$	Under Voltage Disabled (For DVDD)			2.9		V
$DVDDUV_L$	Under Voltage Enabled (For DVDD)			2.6		V
$PVCCUV_H$	Under Voltage Disabled (For PVCC)			10.4		V
$PVCCUV_L$	Under Voltage Enabled (For PVCC)			9.7		V
Rds-on	Static Drain-to-Source On-state Resistor, NMOS	PVCC=24V, Id=500mA		225		mΩ
GVDD	5V Regulator Voltage Output.			5		V
VREG	1.8V Regulator Voltage Output.			1.8		V
I_{SC}	L(R) Channel Over-Current Protection (Note 4)			8		A
V_{IH}	High-Level Input Voltage	DVDD=3.3V	1.7			V
V_{IL}	Low-Level Input Voltage	DVDD=3.3V			0.8	V
V_{OH}	High-Level Output Voltage	DVDD=3.3V	2.4			V
V_{OL}	Low-Level Output Voltage	DVDD=3.3V			0.4	V
C_I	Input Capacitance			6.4		pF
f_{PWM}	PWM Frequency		235	315	395	KHz

Note 4: Loudspeaker over-current protection is only effective when loudspeaker drivers are properly connected with external LC filters. Please refer to the application circuit example for recommended LC filter configuration.

Electrical Characteristics and Specifications for Loudspeaker (Stereo)

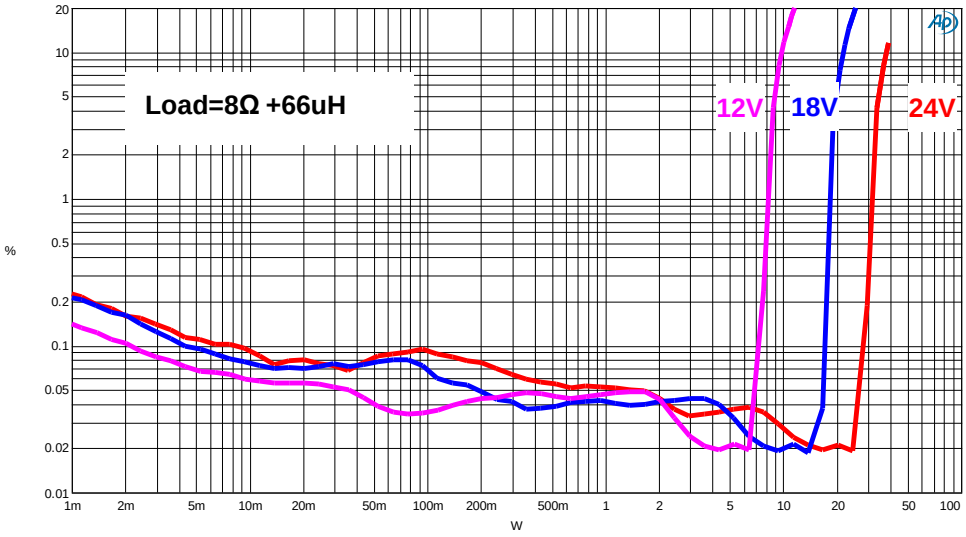
Condition: T_A=25 °C, DVDD=3.3V, PVCCL=PVCCR=24V, F_S=48kHz, Load=8Ω ; Input is 1kHz sine wave. Volume is 0dB unless otherwise specified.

Symbol	Parameter	Condition	Input Level	Min	Typ	Max	Units
P_O	Output Power (Note 5)	THD+N=0.02%, f=1kHz, PVCC=24V			20		W
		THD+N=10%, f=1kHz, PVCC=12V, R_L=4Ω			16		W
		THD+N=10%, f=1kHz, PVCC=12V, R_L=8Ω			9.7		W
THD+N	Total Harmonic Distortion + Noise	P_O=10W			0.027		%
		P_O=5W			0.04		%
Vn	Noise	R_L=8Ω ,A-Weighted Filter			117		uV
		R_L=8Ω ,A-Weighted Filter, PVCC=12V			76		uV
SNR	Signal to Noise Ratio (Note 6)	Maximum output at THD+N=1%, f=1kHz,			102		dB
DR	Dynamic Range (Note 6)	-60dB of input level			109		dB
PSRR	Power Supply Rejection Ratio	V_{RIPPLE}=200mVpp at 1kHz			66		dB
X-talk	Channel Separation (non-shield choke)	P_O=1W at 1kHz			85		dB

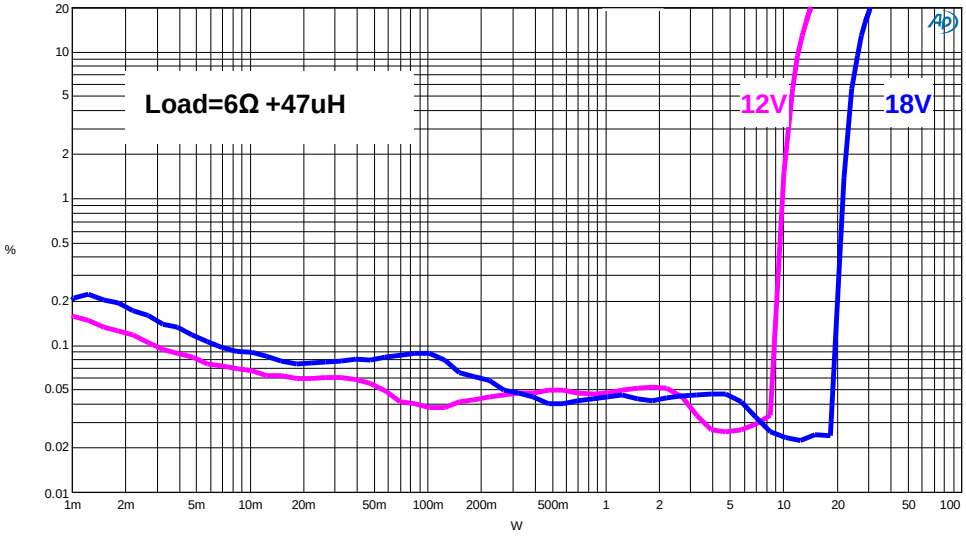
Note 5: Thermal dissipation is limited by package type and PCB design, the external heat-sink or system cooling method should be adopted for RMS power output.

Note 6: Measured with A-weighting filter.

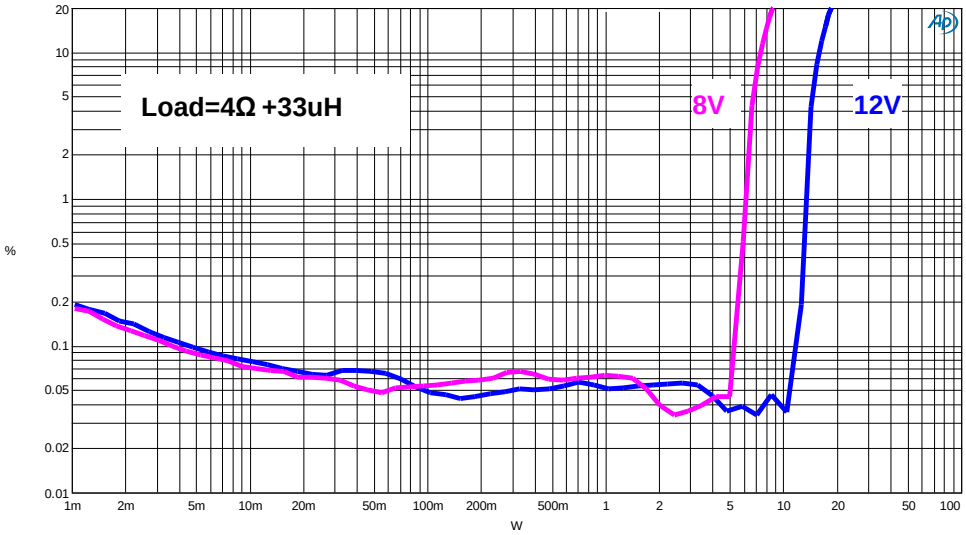
THD + N (%) v.s. Output power (8Ω load)



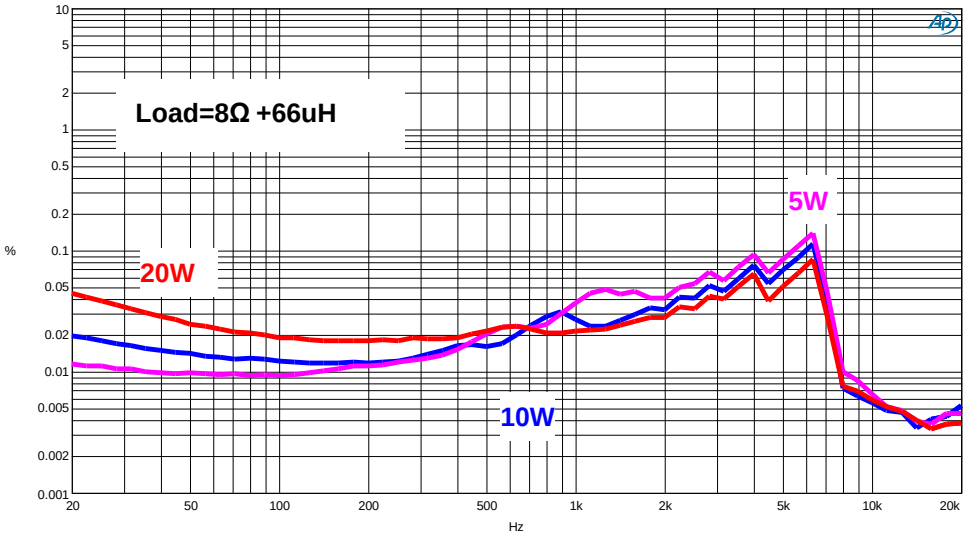
THD + N (%) v.s. Output power (6Ω load)



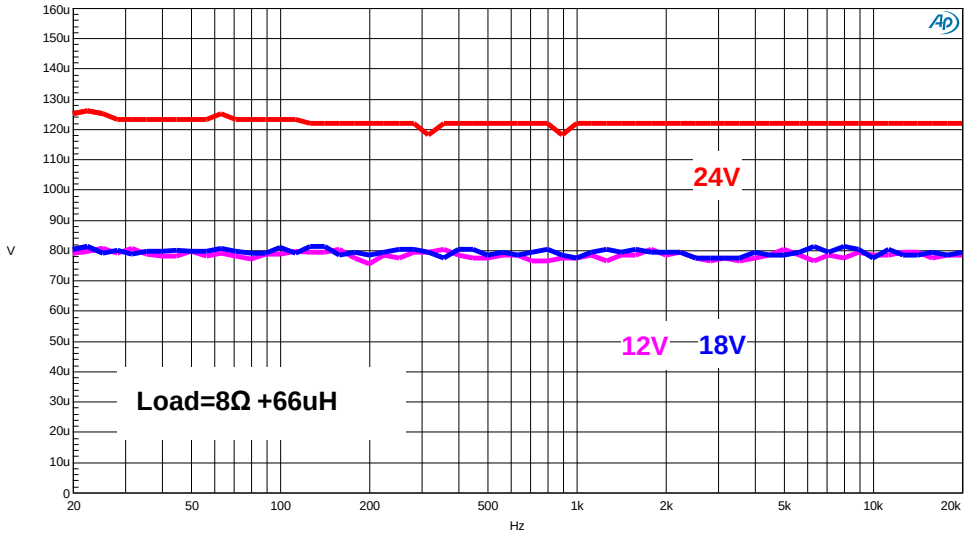
THD + N (%) v.s. Output power (4Ω load)



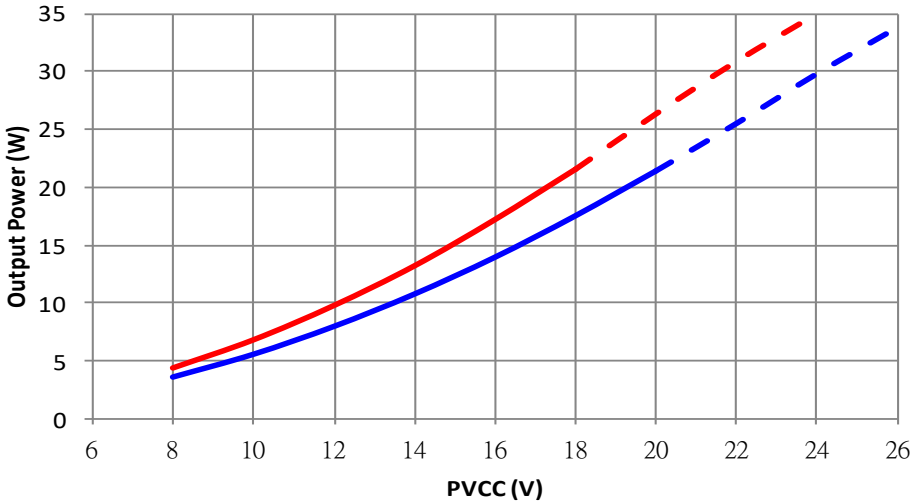
THD + N (%) v.s. Frequency (24V 8Ω load)



Noise (8Ω load)

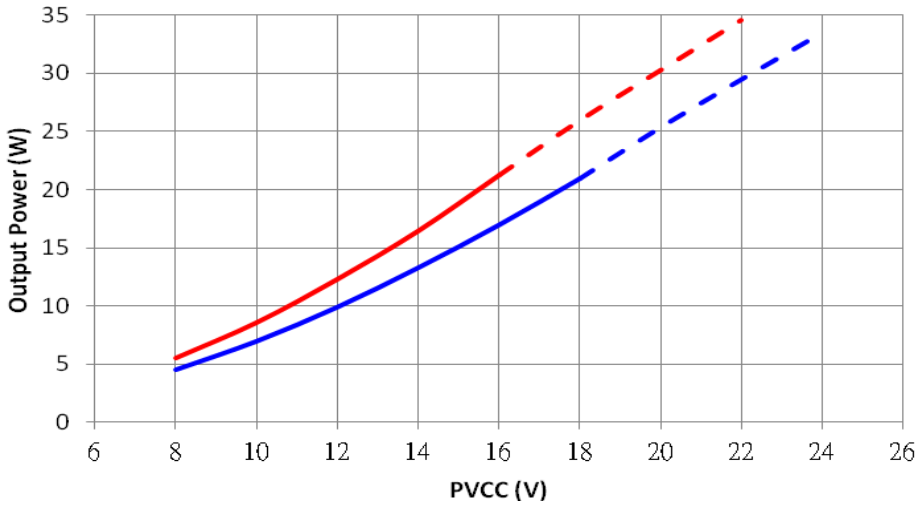


AD87010_8ohm stereo



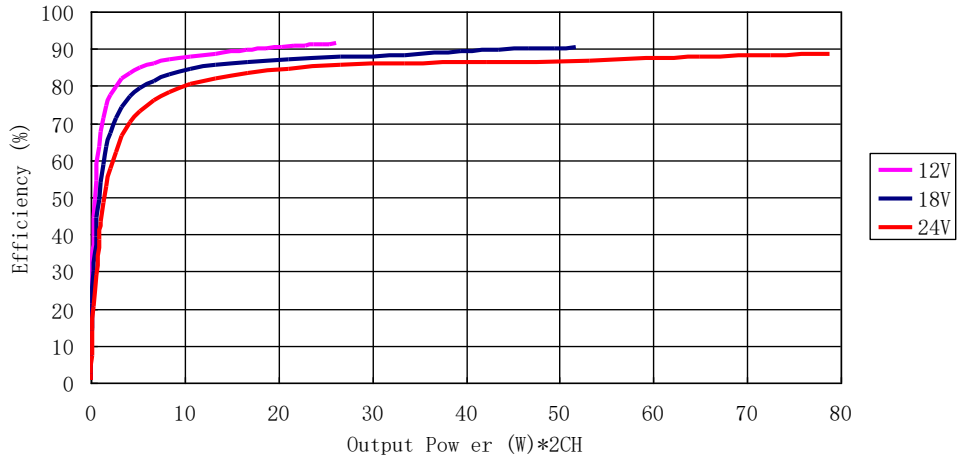
Note: Dashed Line represent thermally limited regions.

AD87010_6ohm stereo

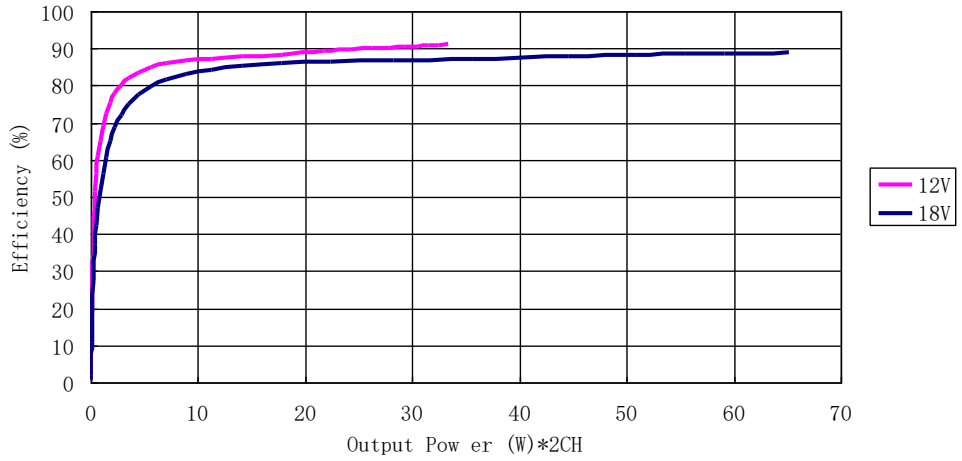


Note: Dashed Line represent thermally limited regions.

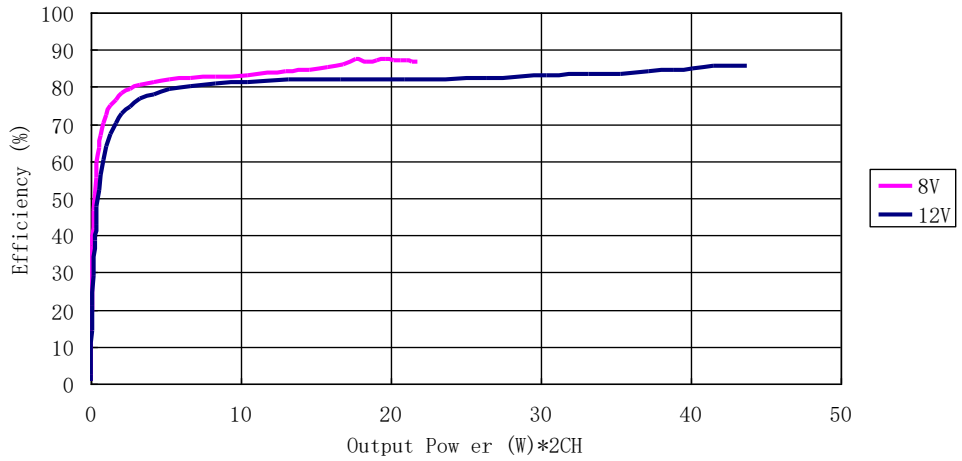
Efficiency (Stereo 8Ω load) / 2ch



Efficiency (Stereo 6Ω load) / 2ch



Efficiency (Stereo 4Ω load) / 2ch



Electrical Characteristics and Specifications for Loudspeaker (Mono)

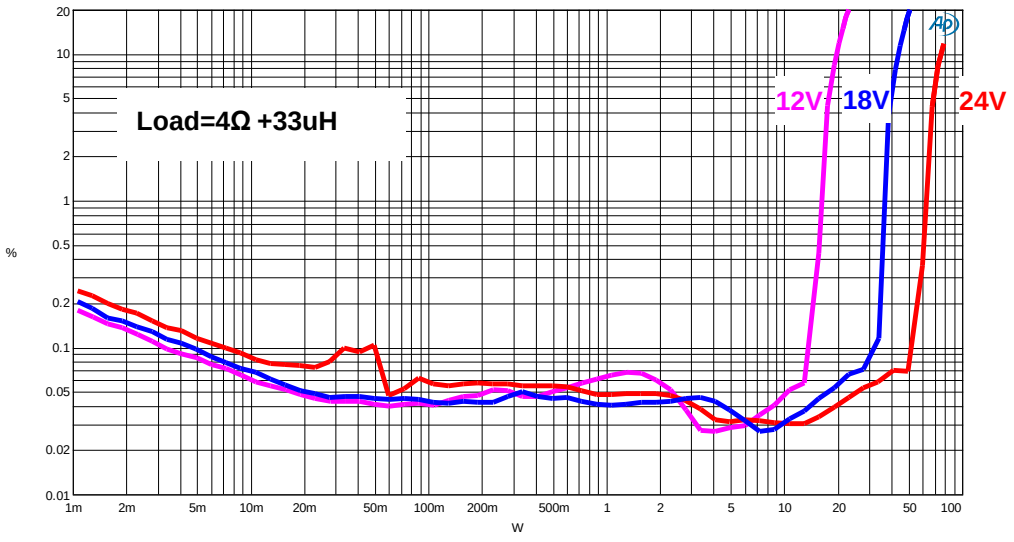
Condition: T_A=25 °C, DVDD=3.3V, PVCCL=PVCCR=24V, F_S=48kHz, Load=4Ω ; Input is 1kHz sine wave. Volume is 0dB unless otherwise specified.

Symbol	Parameter	Condition	Input Level	Min	Typ	Max	Units
P_O	Output Power (Note 5)	THD+N=0.08%, f=1kHz, PVCC=24V			40		W
		THD+N=10%, f=1kHz, PVCC=12V			19.5		W
THD+N	Total Harmonic Distortion + Noise	P_O=20W			0.045		%
Vn	Noise	R_L=4Ω ,A-Weighted Filter			102		uV
		R_L=4Ω ,A-Weighted Filter PVCC=12V			82		uV
SNR	Signal to Noise Ratio (Note 6)	Maximum output at THD+N=1%, f=1kHz,			103		dB
DR	Dynamic Range (Note 6)	-60dB of input level			110		dB
PSRR	Power Supply Rejection Ratio	V_{RIPPLE}=200mVpp at 1kHz			66		dB

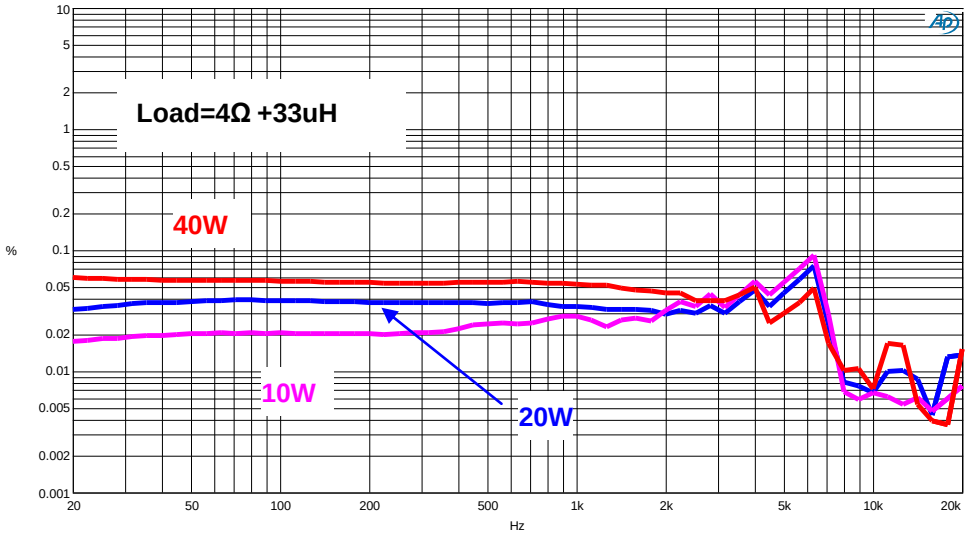
Note 5: Thermal dissipation is limited by package type and PCB design, the external heat-sink or system cooling method should be adopted for RMS power output.

Note 6: Measured with A-weighting filter.

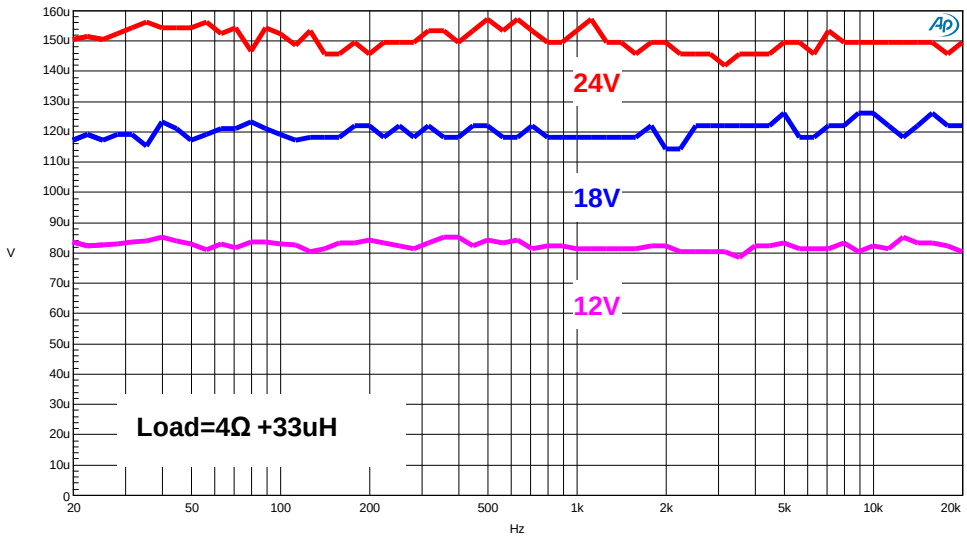
THD + N (%) v.s. Output power (Mono 4Ω load)



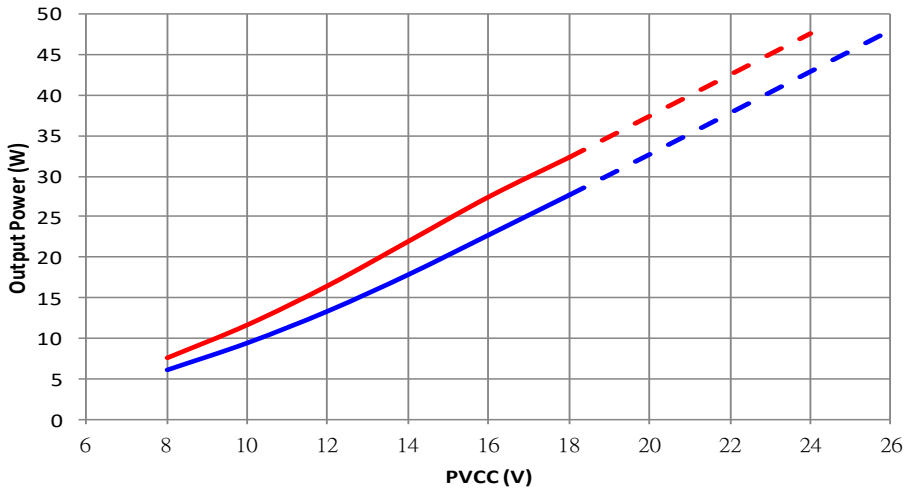
THD + N (%) v.s. Frequency (24V Mono 4Ω load)



Noise (Mono 4Ω load)

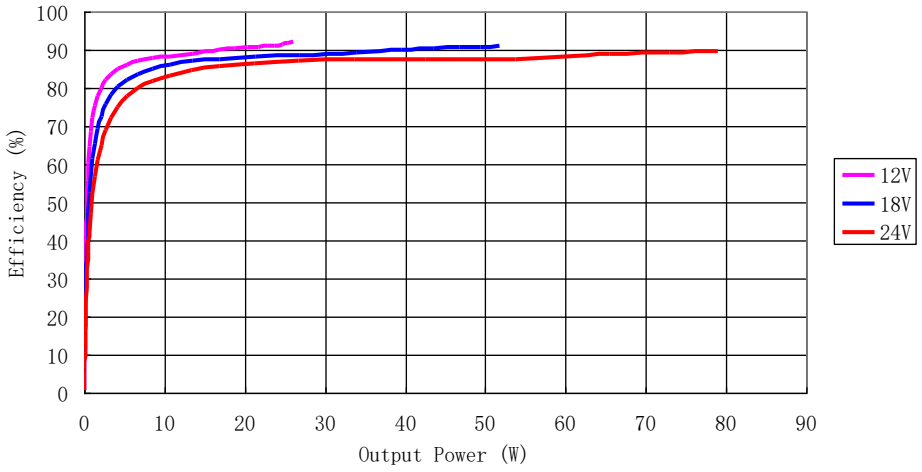


AD87010_4ohm Mono



Note: Dashed Line represent thermally limited regions.

Efficiency (Mono 4Ω load)



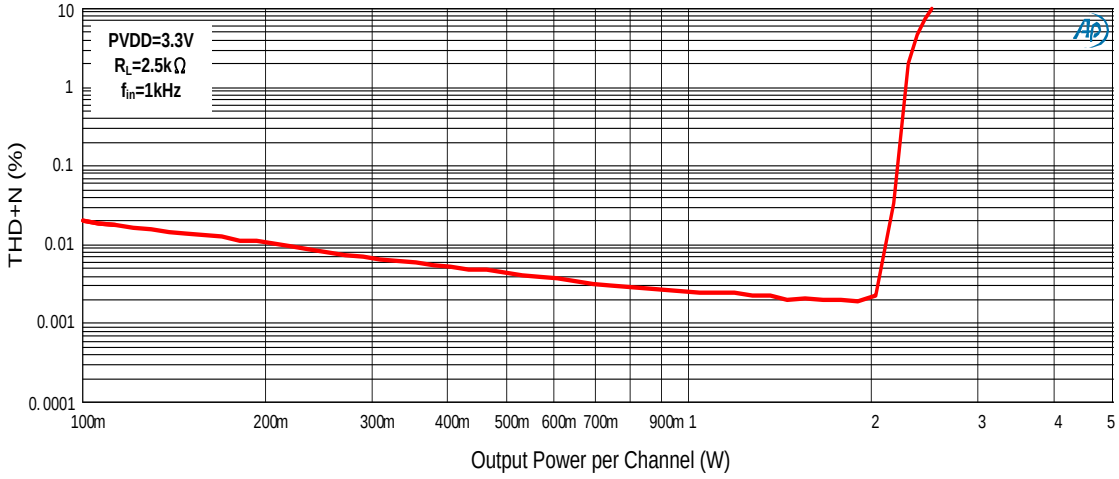
Electrical Characteristics and Specifications for Line Driver

- **Line driver**

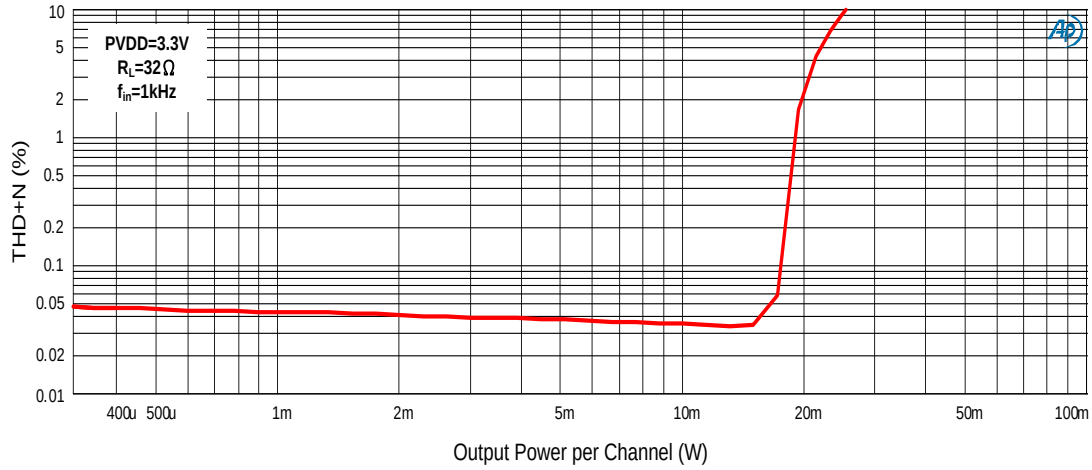
HVDD=3.3V, T_A=25℃, R_L=2.5kΩ, C_{FLY}=C_{PVSS}=1μF, C_{IN}=1μF, R_I=10kΩ, R_F=20kΩ (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_O	Output Voltage (Outputs In Phase)	THD+N=1%, HVDD=3.3V, f_{IN}=1kHz		2.2		Vrms
THD+N	Total Harmonic Distortion Plus Noise	V_O=2Vrms, f_{IN}=1kHz		0.002		%
Crosstalk	Channel Separation	V_O=2Vrms, f_{IN}=1kHz		-106		dB
V_N	Output Noise	R_I=10k, R_F=10k		11	15	μVrms
V_{SR}	Slew Rate			8		V/μs
SNR	Signal to Noise Ratio	V_O=2Vrms, R_I=10k, R_F=10k, A-weighted		107		dB
G_{BW}	Unit-Gain Bandwidth			8		MHz
A_{VO}	Open-Loop Gain		80			dB
V_{OS}	Output Offset Voltage	HVDD=3V to 3.6V, Input Grounded	-5		5	mV
PSRR	Power Supply Rejection Ratio	HVDD=3V to 3.6V, V_{rr}=200mVrms, f_{IN}=1kHz		-80	-60	dB
R_I	Input Resistor Range		1	10	47	kΩ
R_F	Feedback Resistor Range		4.7	20	100	kΩ
f_{CP}	Charge-Pump Frequency		400	500	600	kHz
	Maximum capacitive Load			220		pF
V_{UVP}	External Under Voltage Detection			1.25		V
I_{HYS}	External Under Voltage Detection Hysteresis Current			5		μA
$T_{start-up}$	Start-up Time			0.5		ms

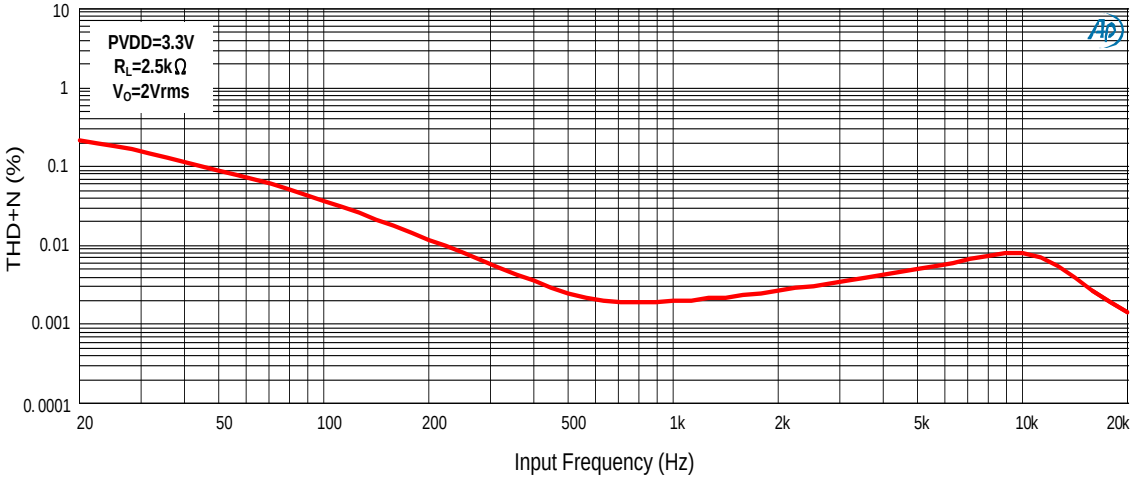
Total Harmonic Distortion + Noise (THD+N) vs. Output Power (R_L=2.5kΩ)



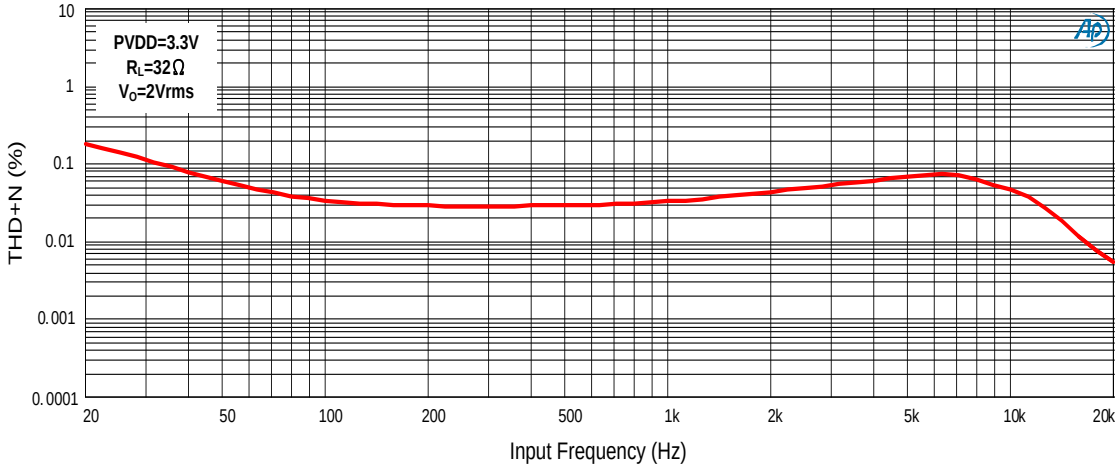
Total Harmonic Distortion + Noise (THD+N) vs. Output Power (R_L=32Ω)



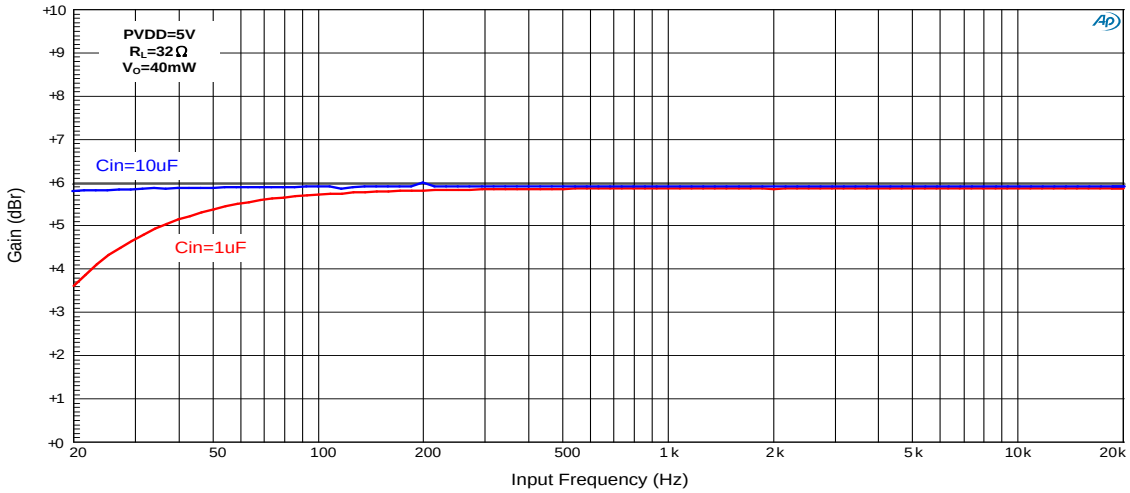
Total Harmonic Distortion + Noise (THD+N) vs. Signal Frequency (R_L=2.5kΩ)



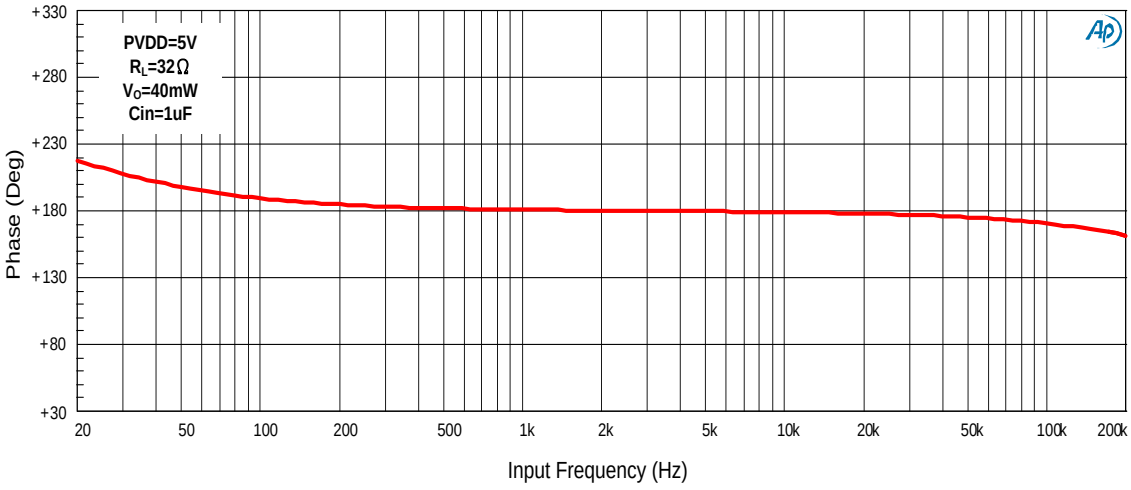
Total Harmonic Distortion + Noise (THD+N) vs. Signal Frequency (R_L=32Ω)



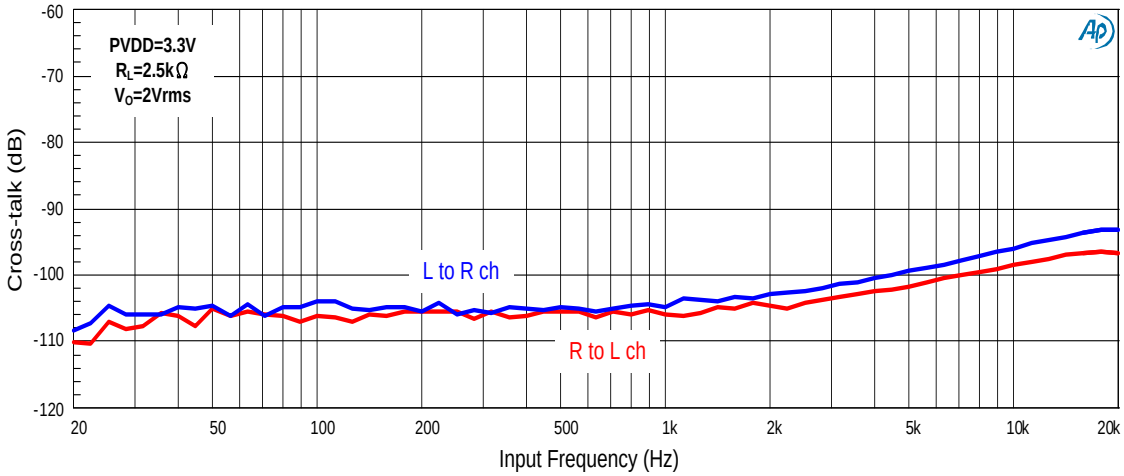
Gain vs. Signal Frequency



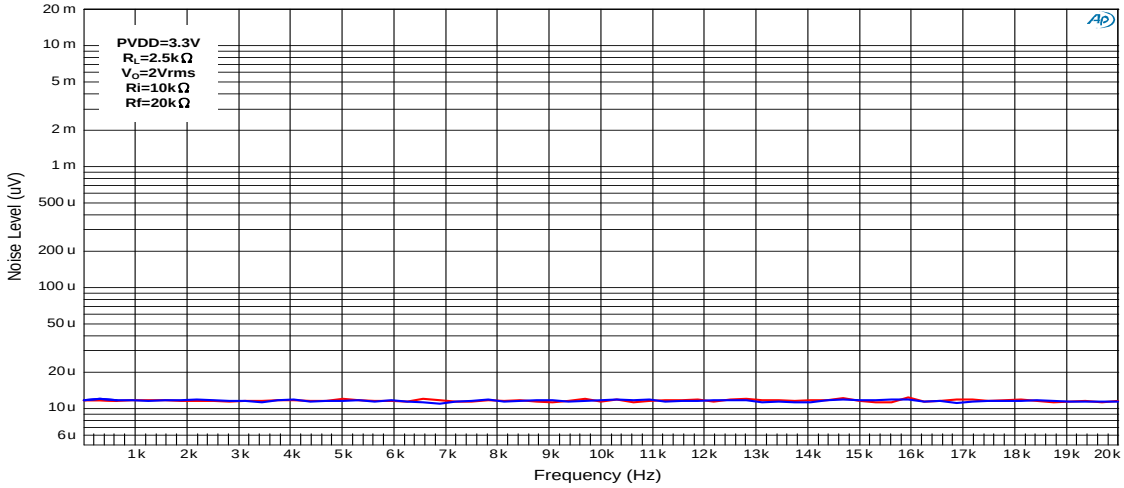
Phase vs. Signal Frequency



Cross-talk

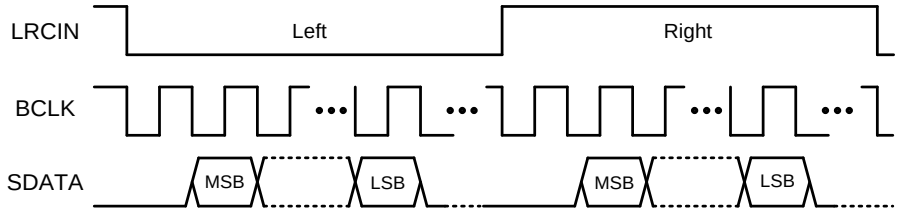

PVDD=3.3V
RL=2.5kΩ
VO=2Vrms
L to R ch
R to L ch
Cross-talk (dB)
-60
-70
-80
-90
-100
-110
-120
20
50
100
200
500
1k
2k
5k
10k
20k
Input Frequency (Hz)

Noise Level

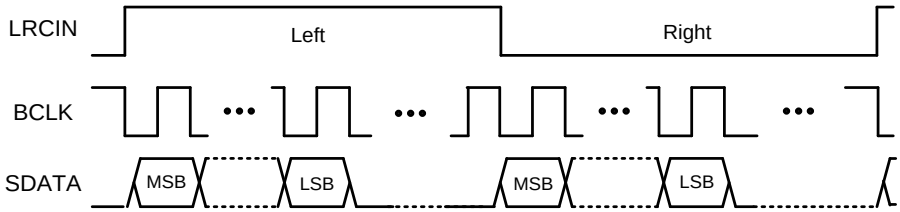

PVDD=3.3V
RL=2.5kΩ
VO=2Vrms
Ri=10kΩ
Rf=20kΩ
Noise Level (uV)
20 m
10 m
5 m
2 m
1 m
500 u
200 u
100 u
50 u
20u
10u
6u
1k
2k
3k
4k
5k
6k
7k
8k
9k
10k
11k
12k
13k
14k
15k
16k
17k
18k
19k
20k
Frequency (Hz)

Interface Configuration

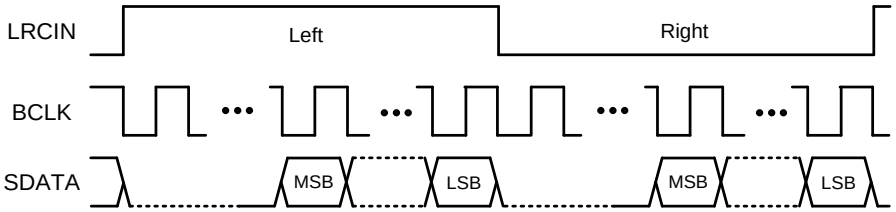
- I^2S



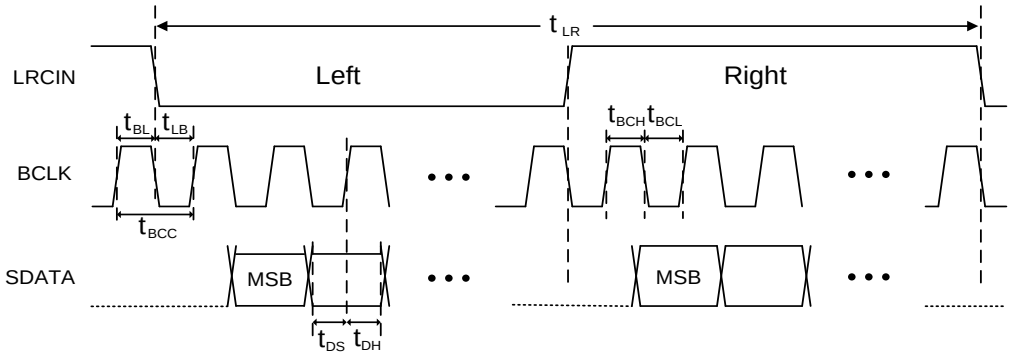
- Left-Alignment



- Right-Alignment

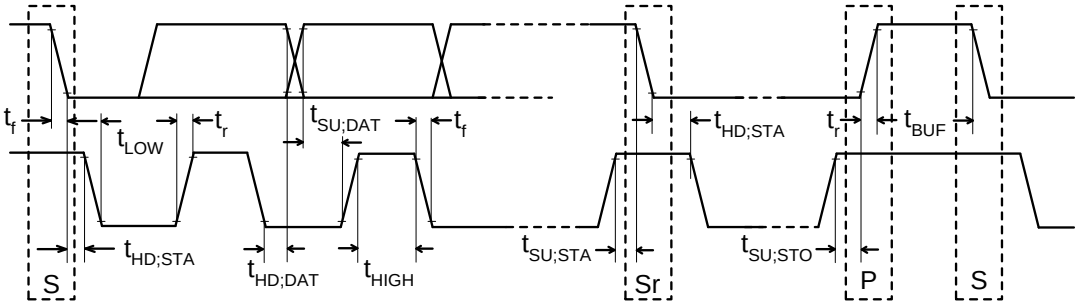


- Timing Relationship (Using I^2S format as an example)



Symbol	Parameter	Min	Typ	Max	Units
t_{LR}	LRCIN Period ($1/F_S$)	5.2		31.25	us
t_{BL}	BCLK Rising Edge to LRCIN Edge	50			ns
t_{LB}	LRCIN Edge to BCLK Rising Edge	50			ns
t_{BCC}	BCLK Period ($1/64F_S$)	162.76		488.3	ns
t_{BCH}	BCLK Pulse Width High	40.69		244	ns
t_{BCL}	BCLK Pulse Width Low	40.69		244	ns
t_{DS}	SDATA Set-Up Time	50			ns
t_{DH}	SDATA Hold Time	50			ns

- I^2C Timing

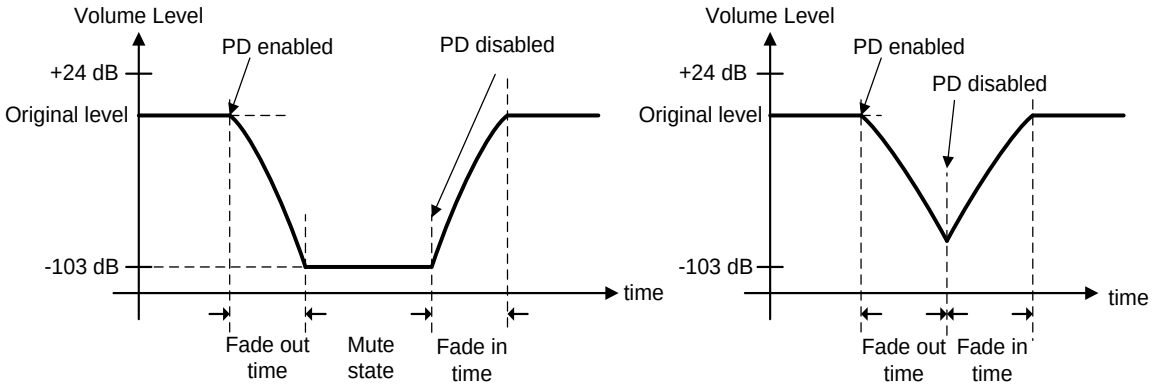


Parameter	Symbol	Standard Mode		Fast Mode		Unit
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time for repeated START condition	$t_{HD,STA}$	4.0	---	0.6	---	us
LOW period of the SCL clock	t_{LOW}	4.7	---	1.3	---	us
HIGH period of the SCL clock	t_{HIGH}	4.0	---	0.6	---	us
Setup time for repeated START condition	$t_{SU;STA}$	4.7	---	0.6	---	us
Hold time for I^2C bus data	$t_{HD;DAT}$	0	3.45	0	0.9	us
Setup time for I_2C bus data	$t_{SU;DAT}$	250	---	100	---	ns
Rise time of both SDA and SDL signals	t_r	---	1000	20+0.1Cb	300	ns
Fall time of both SDA and SDL signals	t_f	---	300	20+0.1Cb	300	ns
Setup time for STOP condition	$t_{SU;STO}$	4.0	---	0.6	---	us
Bus free time between STOP and the next START condition	t_{BUF}	4.7	---	1.3	---	us
Capacitive load for each bus line	C_b		400		400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	$0.1V_{DD}$	---	$0.1V_{DD}$	---	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	$0.2V_{DD}$	---	$0.2V_{DD}$	---	V

Operation Description

- Shut down control

AD87010 has a built-in volume fade-in/fade-out design for SD/Mute function. The relative SD timing diagrams for loudspeakers are shown below.



$$(10^{\frac{target(dB)}{20}} - 10^{\frac{original(dB)}{20}}) x 512 x (1/96K)$$

The volume level will be decreased to -∞dB in several LRCIN cycles. Once the fade-out procedure is finished, AD87010 will turn off the power stages, clock signals (for digital circuits) and current (for analog circuits). After PD pin is pulled low, AD87010 requires T_{fade} to finish the forementioned work before entering power down state. Users can not program AD87010 during power down state. Also, all settings in the registers will remain intact unless DVDD is removed.

If the PD signal is removed during the fade-out procedure (above, right figure), AD87010 will still execute the fade-in procedure. In addition, AD87010 will establish the analog circuits' bias current and send the clock signals to digital circuits. Afterwards, AD87010 will return to its normal status.

- Internal PLL

  AD87010 has a built-in PLL with multiple MCLK/FS ratio, which is selected by I^2C control interface. The MCLK/FS ratio will be fixed at 1024x, 512x, or 256x with a sample frequency of 48kHz, 96kHz, or 192kHz respectively.

- Anti-pop design

  AD87010 will generate appropriate control signals to suppress pop sounds during initial power on/off, power down/up, mute, and volume level changes.

- I^2C chip select

  $\overline{FAULT}$ is an input pin during power start-up. It can be pulled high (15-kΩ pull up) or low (15-kΩ pull down) for I^2C address selection. Low indicates an I^2C address of 0x30, and high an address of 0x34.

- Self-protection circuits

  AD87010 has built-in protection circuits including thermal, short-circuit and under-voltage detection circuits.

  (i) When the internal junction temperature is higher than 160℃, power stages will be turned off and AD87010 will return to normal operation once the temperature drops to 135℃. The temperature values may vary around 10%.

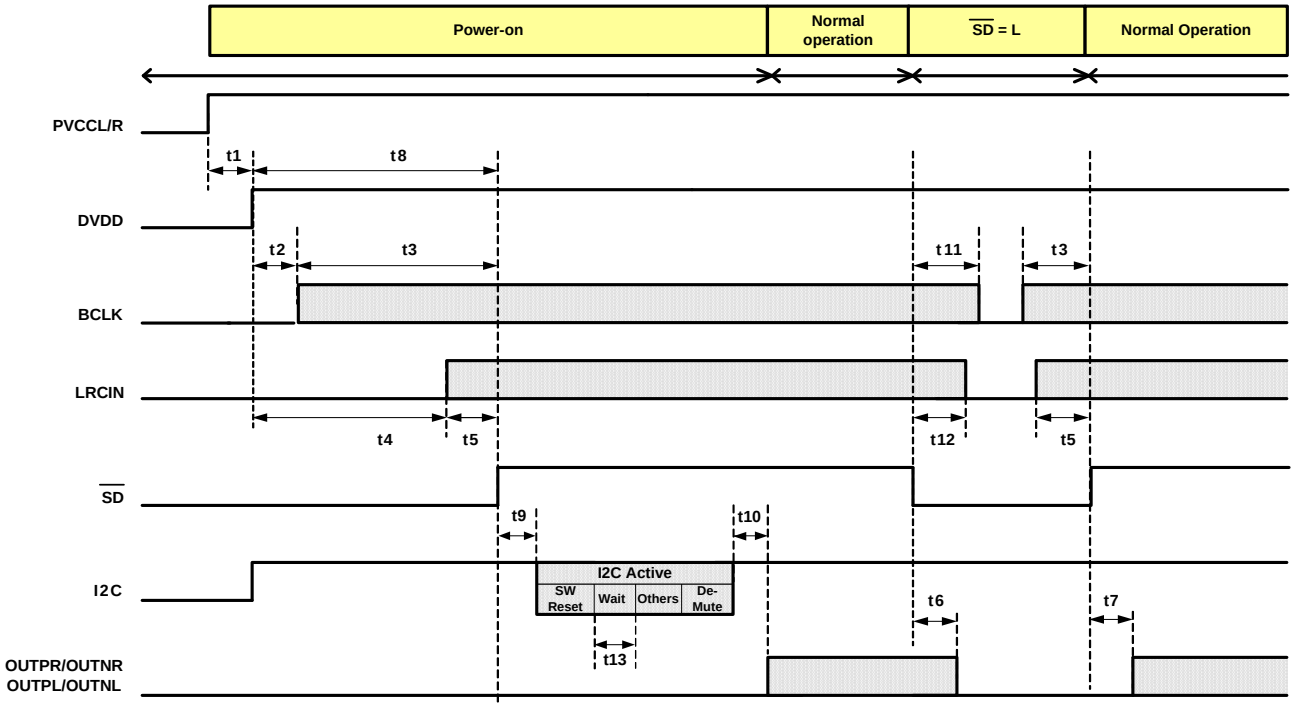
  (ii) The short-circuit protection circuit protects the output stage when the wires connected to loudspeakers are shorted to each other or GND/VDD. For normal 24V operations, the current flowing through the power stage will be less than 8A for stereo configuration. Otherwise, the short-circuit detectors may pull the $\overline{FAULT}$ pin to DGND, disabling the output stages. When the over-temperature or short-circuit condition occurs, the open-drain $\overline{FAULT}$ pin will be pulled low and latched into ERROR state. Once the short-circuit condition is removed, AD87010 will exit ERROR state when one of the following conditions is met: (1) $\overline{SD}$ pin is pulled low, (3) Master mute is enabled through the I^2C interface.

  (iii) Once the DVDD voltage is lower than 2.6V, AD87010 will turn off its loudspeaker power stages and cease the operation of digital processing circuits. When DVDD becomes larger than 2.9V, AD87010 will return to normal operation.

  (iv) If the master clock inputted into BCLK pin stops during the period for 500 ns or more, AD87010 detect the stop of BCLK. In this state, amplifier outputs are forced to Weak Low. If master clock is inputted normally again, $\overline{FAULT}$ pin is set to high.

- Power on sequence

Hereunder is AD87010's power on sequence for FS=48kHz application. Give a de-mute command via I^2C when the whole system is stable.



Note:

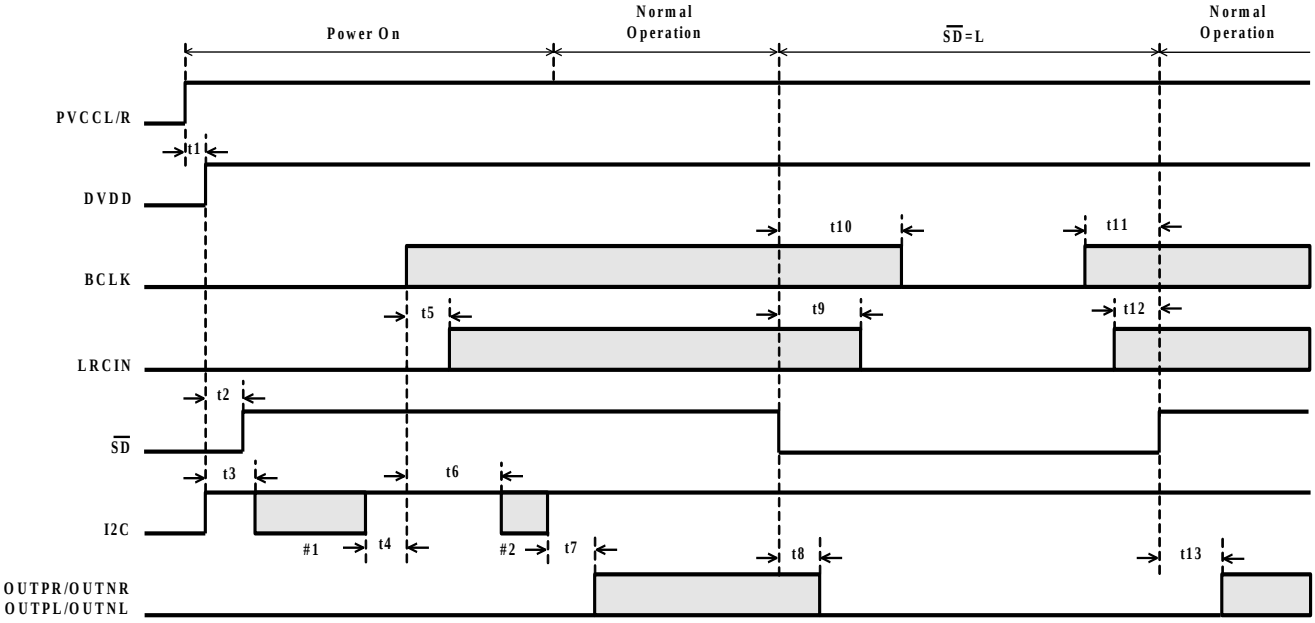
Please be noted below sequence shall be follow up with "I2C Active" processing,

(1) Set S/W reset bit (0X02 B[4]) = 0 → (2) Delay 5ms → (3) Set S/W reset bit (0X02 B[4]) = 1 → (4) Delay 20ms → (5) Set all channels = mute (setting address 0X02 B[3] = 1) → (6) Set other registers (except setting address 0X02 B[3,4]) → (7) Set all channels = de-mute (setting address 0X02 B[3] = 0)

Symbol	Condition	Min	Max	Units
t1		0	-	msec
t2		0	-	msec
t3		10	-	msec
t4		0	-	msec
t5		10	-	msec
t6		--	22(FADE_SPEED=0) 176(FADE_SPEED=1)	msec
t7		--	150	msec
t8		10	-	msec
t9		150	-	msec
t10		-	0.1	msec
t11		25	-	msec

t12		25	-	msec
t13		20		msec

FS=96KHz or 192KHz application, below mentioned power on sequence shall be follow up with. Give a de-mute command via I^2C when the whole system is stable.



#1: Steps

1) Set S/W reset bit (0X02 B[4]) = 0
2) Delay 5ms
3) Set S/W reset bit (0X02 B[4]) = 1
4) Delay 20ms
5) Set all channels = mute (0X02 B[3] = 1)
6) Set I2S format as Fs = 96KHz or 192KHz (0X01 B[5:4] = 01 or 10)
7) Set other registers (except 0X01 B[5:4] and 0X02 B[4:3])

#2: Steps

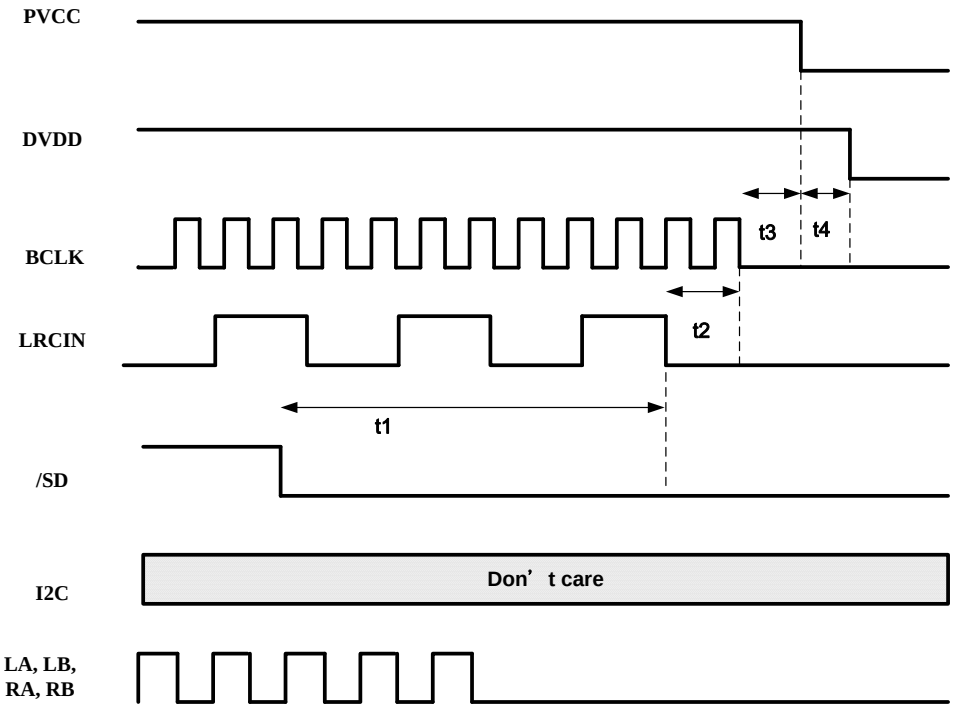
1) Set all channels = de-mute (0x02 B[3] = 0)

#3: If reg.0x16 B[3:2]=00, max. is 30ms
If reg.0x16 B[3:2]=11, max. is 240ms

Symbol	Min	Max	Units	Symbol	Min	Max	Units
t1	0	-	msec	t10	35	-	msec
t2	25	-	msec	t11	10	-	msec
t3	35	-	msec	t12	10	-	msec
t4	20	-	msec	t13	150	-	msec
t5	0	-	msec				
t6	150	-	msec				
t7	-	0.1	msec				
t8	-	#3	msec				
t9	35	-	msec				

- Power off sequence

Hereunder is AD87010's power off sequence.



Symbol	Condition	Min	Max	Units
t1		35(Note 7)	-	msec
t2		0	-	msec
t3		1(Note 8)	-	msec
t4		1(Note 8)	-	msec

Note7: t1 min 35ms refer to FADE_SPEED register=00(address:0X16,bit3~2).

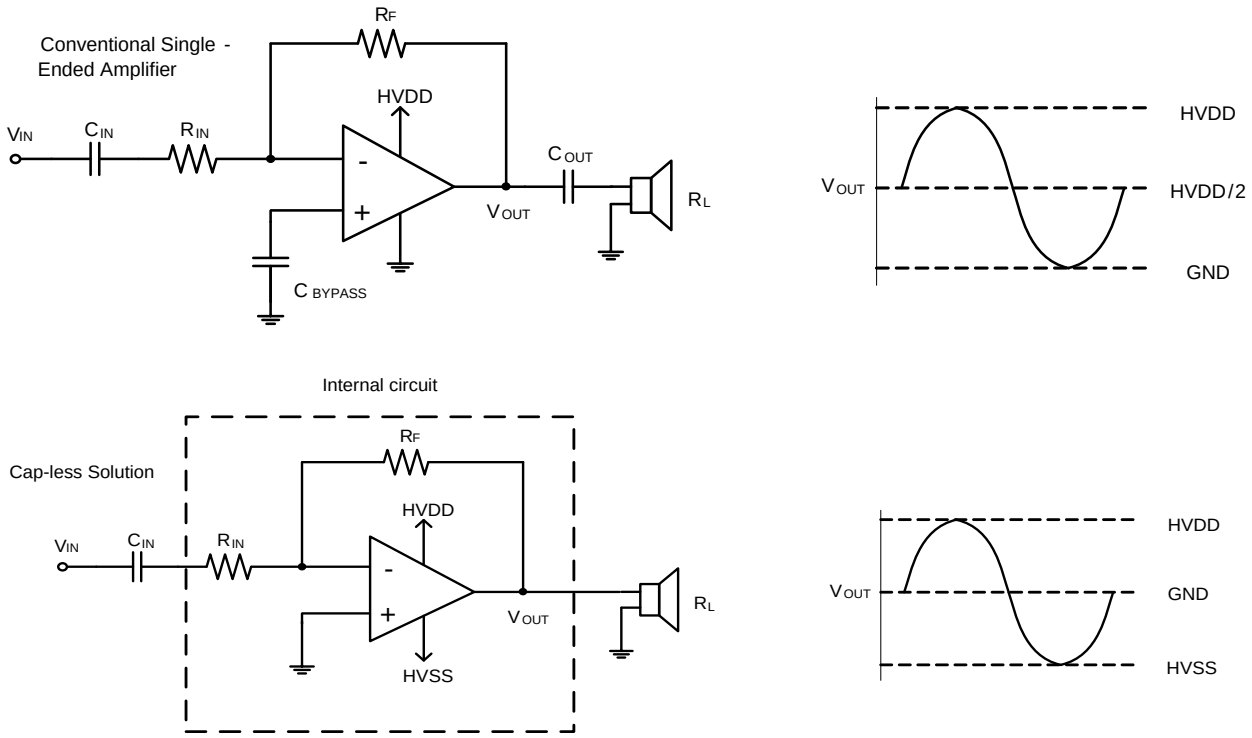
If the FADE_SPEED=11, T1 should change to 280ms.

Note 8: Don't care it if the PVCC or DVDD power supports continuously during the system off.

- Line Driver Amplifiers Operation

A conventional inverting line-driver amplifier always requires an output dc-blocking capacitor and a bypass capacitor. DC blocking capacitors are large in size and cost a lot. It also restricts the output low frequency response. POP will occur if the charge and discharge processes on output capacitors are not carefully take cared. Besides, it needs to wait for a long time to charge V_{OUT} from 0V to HVDD/2.

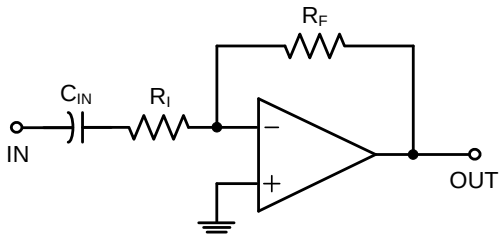
For a cap-less line driver, a negative supply voltage (HVSS) is produced by the integrated charge-pump, and feeds to line driver's negative supply instead of ground. The positive input can directly connect to ground without a C_{BYPASS}, and V_{OUT} is biased at ground which can eliminate the output dc-blocking capacitors. The output voltage swing is doubled compared to conventional amplifiers.



- Gain Setting Resistors (R_I and R_F)

The line driver's gain is determined by R_I and R_F. The configuration of the amplifier is inverting type, The gain equation is listed as follows:

Inverting configuration: $A_V = -\frac{R_F}{R_I}$

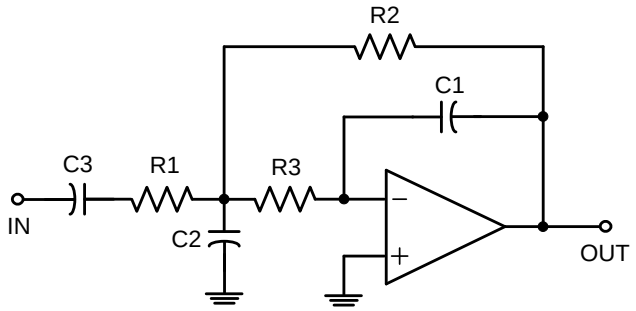


The values of R_I and R_F must be chosen with consideration of stability, frequency response and noise. The recommended value of R_I is in the range from 1kΩ to 47kΩ, and R_F is from 4.7kΩ to 100kΩ for. The gain is in the range from -1V/V to -10V/V for inverting configuration. The following table shows the recommended resistor values for different configurations.

R_I (kΩ)	R_F (kΩ)	Inverting Input Gain (V/V)
22	22	-1
15	30	-2
33	68	-2.1
10	100	-10

- Second-Order Filter Configuration

Line Driver can be used like a standard OPAMP. Several filter topologies can be implemented by using line driver, both single-ended and differential input configuration. For inverting input configuration, the overall gain is $-\frac{R2}{R1}$, the high-pass filter's cutoff frequency is $\frac{1}{2\pi R1C3}$, the low-pass filter's cutoff frequency is $\frac{1}{2\pi\sqrt{R2R3C1C2}}$, The following table show the detail component values.



Gain (V/V)	High Pass (Hz)	Low Pass (kHz)	C1 (pF)	C2 (pF)	C3 (μF)	R1 (kΩ)	R2 (kΩ)	R3 (kΩ)
-1	1.6	40	100	680	10	10	10	24
-1.5	1.3	40	68	680	15	8.2	12	30
-2	1.6	60	33	150	6.8	15	30	47
-2	1.6	30	47	470	6.8	15	30	43
-3.33	1.2	30	33	470	10	13	43	43
-10	1.5	30	22	1000	22	4.7	47	27

- External Under-Voltage Protection for Line Driver

The external under-voltage protection is used to mute the line-driver before any input voltage change to generate a POP. The threshold of UVP pin is designed to 1.25V. By using a resistor divider, users can decide the UVP level and hysteresis level. The levels can be obtained by following equations:

$$V_{UVP} = (1.25V - 6\mu A \times Rc) \times (Ra + Rb) / Rb$$
$$Hysteresis = 5\mu A \times Rc \times (Ra + Rb) / Rb$$

With the condition Rc >> (Ra // Rb).

For example, to obtain V_{UVP}=2.67V, Hysteresis=0.37V, Ra=1.5kΩ, Rb=1kΩ, Rc=30kΩ.

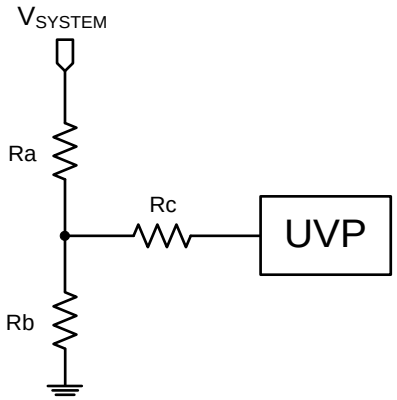


Figure. Application circuit of UVP pin

- Enable Function for Line Driver

The enable function is used to reduce power consumption while the device is not in use. When a logic low is applied to this pin, the overall circuits are turned off. Line driver output and HVSS are pulled to ground. When a logic high is applied to enable pin, the HVSS is started to build-up and line driver output signal is released after about 0.5ms typically.

- Input Blocking Capacitors (C_{IN})

An input blocking capacitor is required to block the dc voltage of the audio source and allows the input to bias at a proper dc level for optimum operation. The input capacitor and input resistor (R_I) form a high-pass filter with the corner frequency determined as following equation:

$$f_C = \frac{1}{2\pi R_I C_{IN}}$$

I²C-Bus Transfer Protocol

- Introduction

  AD87010 employs I²C-bus transfer protocol. Two wires, serial data and serial clock carry information between the devices connected to the bus. Each device is recognized by a unique 7-bit address and can operate as either a transmitter or a receiver. The master device initiates a data transfer and provides the serial clock on the bus. AD87010 is always an I²C slave device.

- Protocol

  - START and STOP condition

    START is identified by a high to low transition of the SDA signal.. A START condition must precede any command for data transfer. A STOP is identified by a low to high transition of the SDA signal. A STOP condition terminates communication between AD87010 and the master device on the bus. In both START and STOP, the SCL is stable in the high state.

  - Data validity

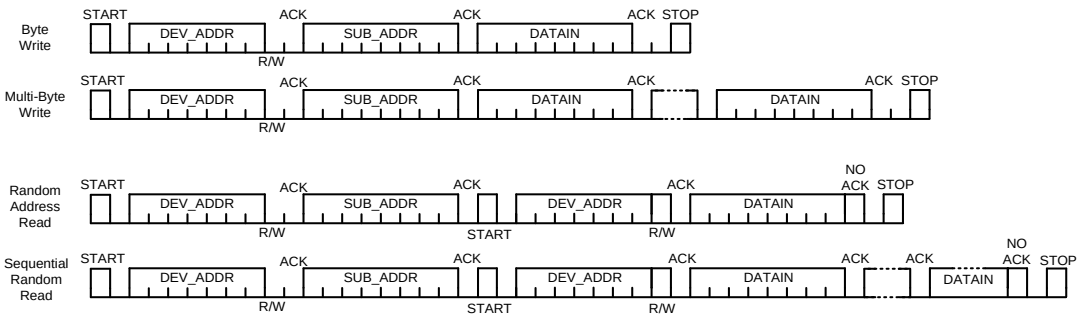
    The SDA signal must be stable during the high period of the clock. The high or low change of SDA only occurs when SCL signal is low. AD87010 samples the SDA signal at the rising edge of SCL signal.

  - Device addressing

    The master generates 7-bit address to recognize slave devices. When AD87010 receives 7-bit address matched with 0110000 or 0110100 ($\overline{\text{FAULT}}$ pin state during power up), AD87010 will acknowledge at the 9th bit (the 8th bit is for R/W bit). The bytes following the device identification address are for AD87010 internal sub-addresses.

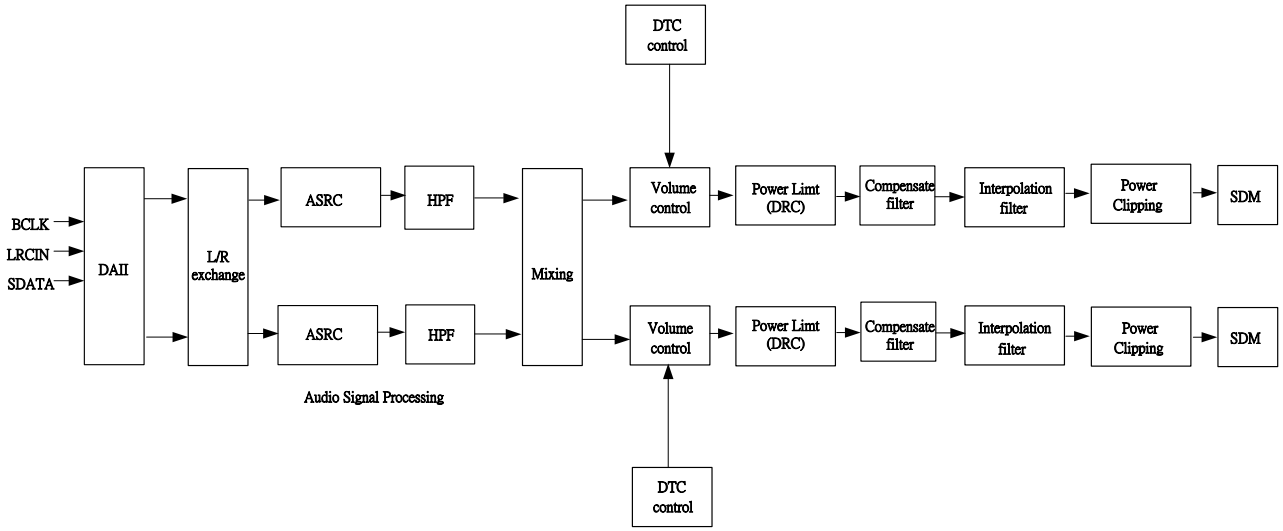
  - Data transferring

    Each byte of SDA signaling must consist of 8 consecutive bits, and the byte is followed by an acknowledge bit. Data is transferred with MSB first, as shown in the figure below. In both write and read operations, AD87010 supports both single-byte and multi-byte transfers. Refer to the figure below for detailed data-transferring protocol.



Register Table

The audio signal processing data flow is shown as the following figure. Users can control these function by programming appropriate setting to register table. In this section, the register table is summarized first. The definition of each register follows in the next section.



Address	Register	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
0X00	SCTL1	IF[2]	IF[1]	IF[0]	LREXC	Reserved			NGE
0X01	SCTL 2	BCLK_SEL	Reserved	FS[1]	FS[0]	PMF[3]	PMF[2]	PMF[1]	PMF[0]
0X02	SCTL 3	A_SEL_FAULT	HPB	LV_UVSEL	SW_RSTB	MUTE	CM1	CM2	Reserved
0X03	MVOL	MV[7]	MV[6]	MV[5]	MV[4]	MV[3]	MV[2]	MV[1]	MV[0]
0X04	C1VOL	C1V[7]	C1V[6]	C1V[5]	C1V[4]	C1V[3]	C1V[2]	C1V[1]	C1V[0]
0X05	C2VOL	C2V[7]	C2V[6]	C2V[5]	C2V[4]	C2V[3]	C2V[2]	C2V[1]	C2V[0]
0X06	HVUV	DIS_HVUV	DIS_LVUV_FADE	DIS_OV_FADE	Reserved		HVUVSEL[2]	HVUVSEL[1]	HVUVSEL[0]
0X07	SCTL 4	C1MX_EN	C2MX_EN	PC1_EN	PL1_EN	MONO_EN	PC2_EN	PL2_EN	Reserved
0X08	LAR	LA[3]	LA[2]	LA[1]	LA[0]	LR[3]	LR[2]	LR[1]	LR[0]
0X09	TEST	Prohibited							
0X0A	Reserved	Reserved							
0X0B	Reserved	Reserved							
0X0C	STATUS	Prohibited							
0X0D	ACFG	Prohibited							
0X0E	TM_CTRL	Prohibited							
0X0F	PWM_CTRL	Prohibited							
0X11	ATT	ATT[7]	ATT[6]	ATT[6]	ATT[4]	ATT[3]	ATT[2]	ATT[1]	ATT[0]
0X11	ATM	ATM[7]	ATM[6]	ATM[5]	ATM[4]	ATM[3]	ATM[2]	ATM[1]	ATM[0]
0X12	ATB	ATB[7]	ATB[6]	ATB[5]	ATB [4]	ATB [3]	ATB [2]	ATB [1]	ATB [0]
0X13	PCT	PCT[7]	PCT[6]	PCT[5]	PCT[4]	PCT[3]	PCT[2]	PCT[1]	PCT[0]

0X14	PCM	PCM[7]	PCM[6]	PCM[5]	PCM[4]	PCM[3]	PCM[2]	PCM[1]	PCM[0]
0X15	PCB	PCB[7]	PCB[6]	PCB[5]	PCB [4]	PCB [3]	PCB [2]	PCB [1]	PCB [0]
0X16	SCTL5	NG_CNT_SEL[1]	NG_CNT_SEL[0]	Reserved	DIS_ZD _FADE	FADE_SPEED [1]	FADE_SPEED [0]	NG_GAIN[1]	NG_GAIN[0]
0X17	VFT	MV_FT[1]	MV_FT[0]	C1V_FT[1]	C1V_FT[0]	C2V_FT[1]	C2V_FT[0]	Reserved	
0X18	DTC	DTC_EN	DTC_TH[1]	DTC_TH[0]	DTC_RATE[1]	DTC_RATE[0]	Reserved		
0X19	Reserved	Reserved							
0X1A	NGALT	NGALT[7]	NGALT[6]	NGALT[5]	NGALT[4]	NGALT[3]	NGALT[2]	NGALT[1]	NGALT[0]
0X1B	NGALM	NGALM[7]	NGALM[6]	NGALM[5]	NGALM[4]	NGALM[3]	NGALM[2]	NGALM[1]	NGALM[0]
0X1C	NGALB	NGALB[7]	NGALB [6]	NGALB [5]	NGALB [4]	NGALB [3]	NGALB [2]	NGALB [1]	NGALB [0]
0X1D	NGRLT	NGRLT[7]	NGRLT[6]	NGRLT[5]	NGRLT[4]	NGRLT[3]	NGRLT[2]	NGRLT[1]	NGRLT[0]
0X1E	NGRLM	NGRLM[7]	NGRLM[6]	NGRLM[5]	NGRLM[4]	NGRLM[3]	NGRLM[2]	NGRLM[1]	NGRLM[0]
0X1F	NGRLB	NGRLB[7]	NGRLB [6]	NGRLB[5]	NGRLB[4]	NGRLB [3]	NGRLB [2]	NGRLB [1]	NGRLB [0]
0X20	DRC_ECT	DRC_ECT[7]	DRC_ECT[6]	DRC_ECT[5]	DRC_ECT[4]	DRC_ECT[3]	DRC_ECT[2]	DRC_ECT[1]	DRC_ECT[0]
0X21	DRC_ECB	DRC_ECB[7]	DRC_ECB[6]	DRC_ECB[5]	DRC_ECB[4]	DRC_ECB[3]	DRC_ECB[2]	DRC_ECB[1]	DRC_ECB[0]
0X22	RTT	RTT[7]	RTT[6]	RTT[5]	RTT[4]	RTT[3]	RTT[2]	RTT[1]	RTT[0]
0X23	RTM	RTM[7]	RTM[6]	RTM[5]	RTM[4]	RTM[3]	RTM[2]	RTM[1]	RTM[0]
0X24	RTB	RTB[7]	RTB[6]	RTB[5]	RTB [4]	RTB [3]	RTB [2]	RTB [1]	RTB [0]
0X25	DEVICE ID	Device code				Version code			
0X26	RAM1_ CFADDR	Prohibited							
0X27	RAM1_ A1CF1	Prohibited							
0X28	RAM1_ A1CF2	Prohibited							
0X29	RAM1_ A1CF3	Prohibited							
0X2A	RAM1_ CFRW	Prohibited							
0X2B	HI-RES	Reserved				FIR2_EN	ANTI_LC_EN	ANTI_ALIAS_EN	Reserved
0X2C	MBIST	Prohibited							
0X2D	ERROR	UVBAR	OCSOUT	HITOUT	UVOUT	DC_ERR_N	CK_ERR_N	OVP	Reserved
0X2E	MK_H	MK_HBYTE[7]	MK_HBYTE[6]	MK_HBYTE[5]	MK_HBYTE[4]	MK_HBYTE[3]	MK_HBYTE[2]	MK_HBYTE[1]	MK_HBYTE[0]
0X2F	MK_L	MK_LBYTE[7]	MK_LBYTE[6]	MK_LBYTE[5]	MK_LBYTE[4]	MK_LBYTE[3]	MK_LBYTE[2]	MK_LBYTE[1]	MK_LBYTE[0]

Detail Description for Register

In this section, please note that the highlighted columns are the default value of these tables. If no highlighted, it is because the default setting of this bit is determined by external pin.

- Address 0X00 : State control 1

  AD87010 support multiple serial data input formats including I^2S, Left-alignment and Right-alignment. These formats is chosen by user via bit7~bit5 of address 0.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:5]	IF[2:0]	Input Format	000	I^2S 16-24 bits
			001	Left-alignment 16-24 bits
			010	Right-alignment 16 bits
			011	Right-alignment 18 bits
			100	Right-alignment 20 bits
			101	Right-alignment 24 bits
			other	Reversed
B[4]	LREXC	Left/Right (L/R) Channel Exchanged	0	No exchanged
			1	L/R exchanged
B[3]	X	Reserved		
B[2]	X	Reserved		
B[1]	X	Reserved		
B[0]	NGE	Noise Gate Enable	0	Disable
			1	Enable

- Address 0X01 : State control 2

AD87010 has built-in PLL, multiple MCLK/FS ratio is supported. Detail setting is shown as the above table.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	BCLK_SEL	BCLK System enable	0	Disable
			1	Enable
B[6]	X	Reserved		
B[5:4]	FS	Sampling Frequency	00	32/44.1/48kHz
			01	64/88.2/96kHz
			10	128/176.4/192kHz
			11	128/176.4/192kHz

Multiple MCLK/FS ratio setting table

BIT	NAME	DESCRIPTION	VALUE	B[5:4]=00	B[5:4]=01	B[5:4]=1x
B[3:0]	PMF[3:0]	MCLK/Fs setup when PLL is not bypassed	0000	1024x	512x	256x
			0001	Reset Default (64x)	Reset Default (64x)	Reset Default (64x)
			0010	128x	128x	128x
			0011	192x	192x	192x
			0100	256x	256x	256x
			0101	384x	384x	Reserved
			0110	512x	512x	
			0111	576x	Reserved	
			1000	768x		
			1001	1024x		

- Address 0X02 : State control 3

The $\overline{FAULT}$ of AD87010 is a dual function pin. It is treated as an I2C device address selection input when bit 7 is set as low. It will become as a FAULT output pin when bit 7 is set as high. To prevent the DC current from damaging the speaker, a high pass filter (3dB frequency=1Hz) is built into the AD87010. It can be enabled or disabled by bit 6 of address 0X02.

AD87010 has a mute function which includes master mute and individual channel mute modes. When the master mute mode is enabled, both left and right processing channels are muted. On the other hand, either channel can be muted by using the channel mute mode. When the mute function is enabled or disabled, the fade-out or fade-in process will be initiated.

AD87010 frequency response will become higher at high frequency area with PVCC lower 12V.Turning on the compensate filter will can adjust the frequency response more flat at high frequency area while PVCC lower 12V.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	A_SEL_FAULT	I2C address selection or FAULT output	0	I2C device address selection
			1	ERROR output
B[6]	HPB	DC Blocking HPF Bypass	0	Enable
			1	Disabled
B[5]	LV_UVSEL	LV Under Voltage Selection	0	2.6V
			1	2.2V
B[4]	SW_RSTB	Software reset	0	Reset
			1	Normal operating
B[3]	MUTE	Master Mute	0	Un-Mute
			1	Mute
B[2]	CM1	Channel 1 Mute	0	Un-Mute
			1	Mute
B[1]	CM2	Channel 2 Mute	0	Un-Mute
			1	Mute
B[0]	COMP_EN	Frequency Compensate filter	0	Disable
			1	Enable

- Address 0X03 : Master volume

AD87010 supports both master-volume and channel-volume control for the stereo processing channels. Both master volume control (Address 0X03) and channel volume (Address 0X04 and 0X05) settings range from +12dB ~ -102dB. Given master volume level, say, Level A (in dB unit) and channel volume level, say Level B (in dB unit), the total volume equals to Level A plus with Level B and its range is from +24dB ~ -102dB, i.e., -103dB ≦ Total Volume (Level A + Level B) ≦ +24dB.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	MV[7:0]	Master Volume	00000000	+12dB
			00000001	+11.5dB
			00000010	+11dB
			:	:
			00010111	0.5dB
			00011000	0dB
			00011001	-0.5dB
			:	:
			11100110	-103dB
			11100101	-∞dB
			:	:
			11111111	-∞dB

- Address 0X04 : Channel1 volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C1V[7:0]	Channel 1 Volume	00000000	+12dB
			00000001	+11.5dB
			:	:
			00010100	2dB
			:	:
			00011000	0dB
			00011001	-0.5dB
			:	:
			11100110	-103dB
			11100101	-∞dB
			:	:
			1111111	-∞dB

- Address 0X05 : Channel2 volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C2V[7:0]	Channel 2 Volume	00000000	+12dB
			00000001	+11.5dB
			:	:
			00010100	2dB
			:	:
			00011000	0dB
			00011001	-0.5dB
			:	:
			11100110	-103dB
			11100101	-∞dB
			:	:
			1111111	-∞dB

- Address 0X06 : Under voltage selection for high voltage supply

AD87010 provides HV under voltage detection which can be enable or disable via bit 7. The under-voltage detection level is programmable via bit2~ bit0. Once the output stage voltage drops below the default value (see table), AD87010 will fade out audio signals to turn off the speaker.

If user want to have an application with PVCC is lower than 10V, user can set HV under voltage disable or set lower under voltage level. AD87010 also provide OV fade function, user can select fade or not fade for OV via bit5.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	Dis_HVUV	Disable HV Under Voltage Circuit	0	Enable
			1	Disable
B[6]	DIS_LVUV_FADE	Disable LVUV Fade Selection	0	Fade
			1	No fade
B[5]	DIS_OV_FADE	Disable over voltage fade	0	Fade
			1	No fade
B[4:3]	X	Reserved		
B[2:0]	HVUVSEL[2:0]	HV Under Voltage Selection (Active)	000	4V
			001	8.2V
			010	9.7V
			011	13.2V
			100	15.5V
			101	19.5V
			Others	4V

- Address 0X07 : State control 4

AD87010 provides channel mix, power clipping, and dynamic range control (DRC) function. These functions can be enable or not as the following table.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	C1MX_EN	Channel1 Mixing Enable	0	Disable
			1	Enable
B[6]	C2MX_EN	Channel2 Mixing Enable	0	Disable
			1	Enable
B[5]	PC1_EN	CH1 Power Clipping enable	0	Disable
			1	Enable
B[4]	PL1_EN	CH1 Power limit enable	0	Disable
			1	Enable
B[3]	MONO_EN	MONO or Stereo configure	0	Stereo
			1	MONO
B[2]	PC2_EN	CH2 Power Clipping enable	0	Disable
			1	Enable
B[1]	PL2_EN	CH2 Power limit enable	0	Disable
			1	Enable
B[0]	X	Reserved		

AD87010 also provides MONO register via bit 3 of address 0X07. Besides this MONO register, address 0X2E and 0X2F should be setting to enter MONO configuration. The output configuration shall be right connected before Mono configuration enable. That's possible to damage chips due to channel shoot-through if the wrong output configuration is connected.

- Address 0X08 : Attack rate and Release rate for Dynamic Range Control (DRC)

The attack/release rates of AD87010 are defined as following table,

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:5]	LA[3:0]	DRC Attack Rate	0000	3 dB/ms
			0001	2.667 dB/ms
			0010	2.182 dB/ms
			0011	1.846 dB/ms
			0100	1.333 dB/ms
			0101	0.889 dB/ms
			0110	0.4528 dB/ms
			0111	0.2264 dB/ms
			1000	0.15 dB/ms
			1001	0.1121 dB/ms
			1010	0.0902 dB/ms
			1011	0.0752 dB/ms
			1100	0.0645 dB/ms
			1101	0.0563 dB/ms
			1110	0.0501 dB/ms
			1111	0.0451 dB/ms
B[3:0]	LR[3:0]	DRC Release Rate	0000	0.5106 dB/ms
			0001	0.1371 dB/ms
			0010	0.0743 dB/ms
			0011	0.0499 dB/ms
			0100	0.0360 dB/ms
			0101	0.0299 dB/ms
			0110	0.0264 dB/ms
			0111	0.0208 dB/ms
			1000	0.0198 dB/ms
			1001	0.0172 dB/ms
			1010	0.0147 dB/ms
			1011	0.0137 dB/ms
			1100	0.0134 dB/ms
			1101	0.0117 dB/ms
			1110	0.0112 dB/ms
			1111	0.0104 dB/ms

- Address 0X10 : Top 5 bits of attack threshold for Dynamic Range Control (DRC)

The AD87010 provides dynamic range control function. When the input RMS exceeds the programmable attack threshold value, the output power will be limited by this threshold power level via gradual gain reduction. Attack threshold is defined by 24-bit representation composed of registers controlled by I2C. The device addresses of DRC attack threshold are 0X10, 0X11, and 0X12.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	ATT[7:0]	Top 8 Bits of Attack Threshold	X	User programmed
			00100000	0dB

- Address 0X11 : Middle 8 bits of attack threshold

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	ATM[7:0]	Middle 8 Bits of Attack Threshold	X	User programmed
			00000000	0dB

- Address 0X12 : Bottom 8 bits of attack threshold

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	ATB[7:0]	Bottom 8 bits of attack threshold	X	User programmed
			00000000	0dB

- Address 0X13 : Top 8 bits of power clipping

The AD87010 provides power clipping function to avoid excessive signal that may destroy loud speaker. The power clipping level is defined by 24-bit representation composed of registers controlled by I2C. The device addresses of power clipping threshold are 0X13, 0X14, and 0X15.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	PCT[7:0]	Top 8 Bits of Power Clipping Level	X	User programmed
			00100000	0dB

- Address 0X14 : Middle 8 bits of power clipping

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	PCM[7:0]	Middle 8 Bits of Power Clipping Level	X	User programmed
			00000000	0dB

- Address 0X15 : Bottom 8 bits of power clipping level

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	PCB[7:0]	Bottom 8 Bits of Power Clipping Level	X	User programmed
			00000000	0dB

The following table shows the power clipping level's numerical representation.

Sample calculation for power clipping

Max amplitude	dB	Linear	Decimal	Hex (3.21 format)
Gain	0	1	2097152	200000
Gain*0.707	-3	0.707	1482680	169FB8
Gain*0.5	-6	0.5	1048576	100000
Gain*L	x	$L=10^{(x/20)}$	D=2097152xL	H=dec2hex(D)

Note: Gain is the closed loop gain of AD87010, the value is 30(±5%) with 8ohm load. If the max amplitude is larger than PVCC, max amplitude change to PVCC.

- Address 0X16 : State control 5

When receiving signal sample points less than noise gate attack level for the time more than noise gate count time, noise gate function will active. The noise gate count time can be programmed via bit [7:6].User can change noise gate gain via bit1~ bit0. When noise gate function occurs, input signal will multiply noise gate gain (x1/8, x1/4 x1/2, x0). User can select fade out or not via bit 4.

AD87010 provide 4 kinds of fade speed(1.25ms,2.5ms,5ms,10ms), user can select most suitable fade speed for their system.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]	NG_CNT_SEL	Noise gate count time selection	00	43ms @fs:48K
			01	86ms @fs:48K
			10	172ms @fs:48K
			11	344ms @fs:48K
B[4]	DIS_NG_FADE	Disable Noise Gate Fade	0	Fade
			1	No fade
B[3:2]	FADE_SPEED	Fade in/out speed selection	00	1.25ms
			01	2.5ms
			10	5ms
			11	10ms
B[1:0]	NG_GAIN	Noise Gate Detection Gain	00	x1/8
			01	x1/4
			10	x1/2
			11	Mute

- Address 0X17 : Volume fine tune

AD87010 supports both master-volume fine tune and channel-volume control fine tune modes. Both volume control settings range from 0dB ~ -0.375dB and 0.125dB per step. Note that the master volume fine tune is added to the individual channel volume fine tune as the total volume fine tune.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]	MV_FT	Master Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[5:4]	C1V_FT	Channel 1 Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[3:2]	C2V_FT	Channel 2 Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[1:0]	X	Reserved		

- Address 0X18 : Dynamic Temperature Control (DTC)

AD87010 supports dynamic temperature control. The table describes the setting of DTC.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	DTC_EN	DTC Enable	0	Disable
			1	Enable
B[6:5]	DTC_TH	DTC Threshold	00	110 °C
			01	120 °C
			10	130 °C
			11	140 °C
B[4:3]	DTC_RATE	DTC Attack and Release Rate	00	1dB/sec
			01	0.5dB/sec
			10	0.33dB/sec
			11	0.25dB/sec
B[2:0]	X	Reserved		

Release threshold is always 10 °C smaller than attack threshold.

For example:

DTC threshold (attack threshold) =130 °C, the release threshold = 120 °C.

DTC threshold (attack threshold) =120 °C, the release threshold = 110 °C.

If junction temperature (Tj) exceeds 130 °C, amplifier gain will be lowered to timing of 1dB/sec. If amplifier gain falls and junction temperature (Tj) turns into less than 130 °C and larger than 120 °C, the gain will not increase or decrease. If amplifier gain falls and junction temperature (Tj) turns into less than 120 °C, amplifier gain will be raised to timing of 1dB/sec.

- Address 0X1A : Top 8 bits of noise gate attack level

When both left and right signals have 2048 consecutive sample points less than the programmable noise gate attack level, the audio signal will multiply noise gate gain, which can be set at x1/8, x1/4, x1/2, or zero if the noise gate function is enabled. Noise gate attack level is defined by 24-bit representation composed of registers controlled by I2C. The device addresses of noise gate attack level are 0X1A, 0X1B, and 0X1C

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	NGALT[7:0]	Top 8 Bits of Noise Gate Attack Level	X	User programmed
			00000000	-110dB

- Address 0X1B : Middle 8 bits of noise gate attack level

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	NGALM[7:0]	Middle 8 Bits of Noise Gate Attack Level	X	User programmed
			00000000	-110dB

- Address 0X1C : Bottom 8 bits of noise gate attack level

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	NGALB[7:0]	Bottom 8 Bits of Noise Gate Attack Level	X	User programmed
			00011010	-110dB

- Address 0X1D : Top 8 bits of noise gate release level

After entering the noise gating status, the noise gain will be removed whenever AD87010 receives any input signal that is more than the noise gate release level. Noise gate release level is defined by 24-bit representation composed of registers controlled by I2C. The device addresses of noise gate release level are 0X1D, 0X1E, and 0X1F.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	NGRLT[7:0]	Top 8 Bits of Noise Gate Release Level	X	User programmed
			00000000	-100dB

- Address 0X1E : Middle 8 bits of noise gate release level

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	NGRLM[7:0]	Middle 8 Bits of Noise Gate Release Level	X	User programmed
			00000000	-100dB

- Address 0X1F : Bottom 8 bits of noise gate release level

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	NGRLB[7:0]	Bottom 8 Bits of Noise Gate Release Level	X	User programmed
			01010011	-100dB

The following table shows the noise gate attack and release threshold level's numerical representation.

Sample calculation for noise gate attack and release level

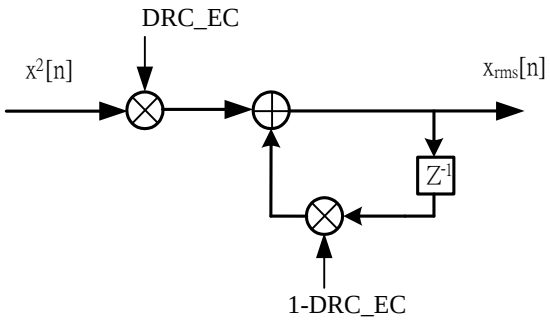
Input amplitude (dB)	Linear	Decimal	Hex (1.23 format)
0	1	8388607	7FFFFF
-100	10^{-5}	83	53
-110	$10^{-5.5}$	26	1A
X	$L=10^{(x/20)}$	D=8388607xL	H=dec2hex(D)

- Address 0X20 : Top 8 bits of DRC energy coefficient

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	DRC_ECT [7:0]	Top 8 Bits of DRC Energy Coefficient	X	User programmed
			00000000	1/2048

- Address 0X21 : Bottom 8 bits of DRC energy coefficient

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	DRC_ECB [7:0]	Bottom 8 Bits of DRC Energy Coefficient	X	User programmed
			00010000	1/2048



The above figure illustrates the digital processing of calculating RMS signal power. In this processing, a DRC energy coefficient is required, which can be programmed for different frequency range. Energy coefficient is defined by 16-bit representation composed of registers controlled by I2C. The device addresses of DRC energy coefficient are 0X20, and 0X21. The following table shows the DRC energy coefficient numerical representation.

Sample calculation for DRC energy coefficient

DRC energy coefficient	dB	Linear	Decimal	Hex {1,b0, DRC_ECT[6:0], DRC_ECB,8'b0} (1.23 format)
1	0	1	8388352	7FFF00
1/256	-48.2	1/256	32768	8000
1/2048	-66.2	1/2048	4096	1000
L	x	$L=10^{(x/20)}$	D=8388352xL	H=dec2hex(D)

- Address 0X22 : Top 8 bits of release threshold for Dynamic Range Control (DRC)

  After AD87010 has reached the attack threshold, its output power will be limited to that level. The output power level will be gradually adjusted to the programmable release threshold level. Release threshold is defined by 21-bit representation composed of registers controlled by I2C. The device addresses of release threshold are 0X22, 0X23, and 0X24.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	RTT[7:0]	Top 8 Bits of Release Threshold	X	User programmed
			00001000	-6dB

- Address 0X23 : Middle 8 bits of release threshold

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	RTM[7:0]	Middle 8 Bits of Release Threshold	X	User programmed
			00000000	-6dB

- Address 0X24 : Bottom 8 bits of release threshold

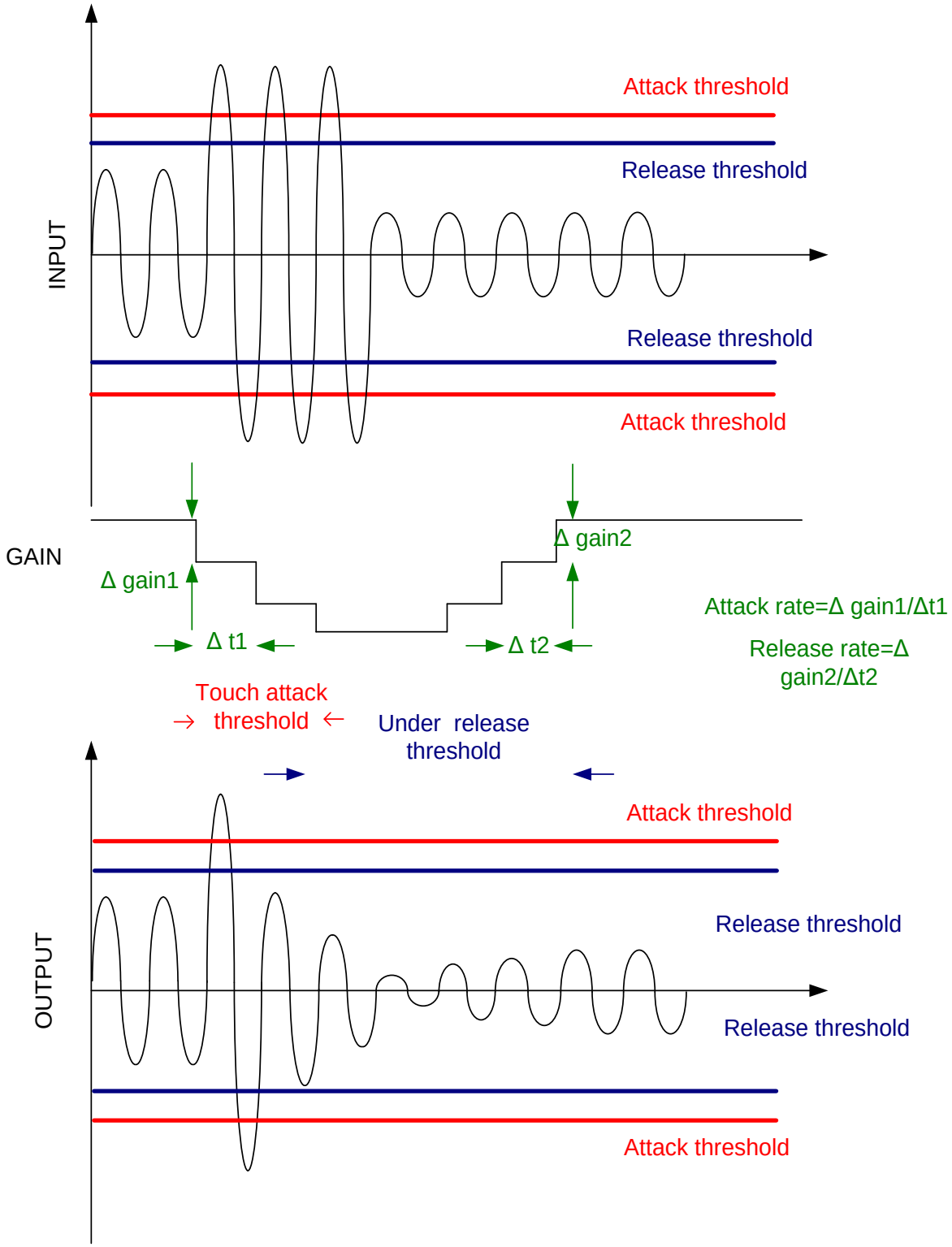
BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	RTB[7:0]	Bottom 8 Bits of Release Threshold	X	User programmed
			00000000	-6dB

The following table shows the attack and release threshold's numerical representation.

Sample calculation for attack and release threshold

Power	dB	Linear	Decimal	Hex (3.21 format)
(Gain^2)/R	0	1	2097152	200000
(Gain^2)/2R	-3	0.5	1048576	100000
(Gain^2)/4R	-6	0.25	131072	80000
((Gain^2)/R)*L	x	$L=10^{(x/10)}$	D=2097152xL	H=dec2hex(D)

To best illustrate the dynamic range control function, please refer to the following figure.



- Address 0X2D, Protection Status Register

The protection registers will show what kind of protection occurs.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	UVBAR	Under voltage occur	1	Normal
			0	Occurred
B[6]	OCSOUT	Over current occur	1	Normal
			0	Occurred
B[5]	HITOUT	Over temperature occur	1	Normal
			0	Occurred
B[4]	UVOUT	Under voltage occur	1	Normal
			0	Occurred
B[3]	DC_ERR_N	DC detection error	1	Normal
			0	Occurred
B[2]	CK_ERR_N	Clock detection error	1	Normal
			0	Occurred
B[1]	OVP	Over voltage occur	1	Normal
			0	Occurred
B[0]	X	Reversed		

- Address 0X2E : Mono Key High Byte

AD87010 provide a protection method to enter mono mode. Besides setting MONO_EN register high, it needs to set address 0X2E value to 0X30 and address 0X2F value to 0X06 for mono application. Otherwise, AD87010 will be stereo mode.

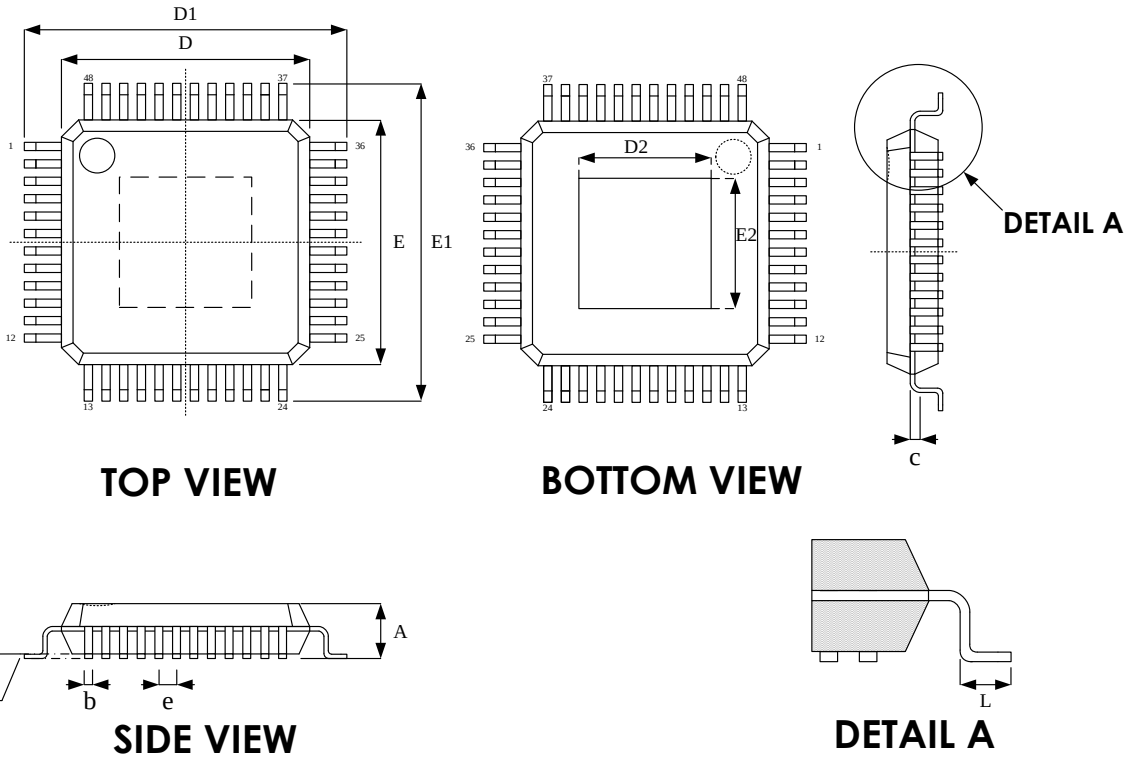
BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	MK_HBYTE[7:0]	Mono key high byte	0000_0000	Stereo
			X	Stereo
			0011_0000	MONO

- Address 0X2F : Mono Key Low Byte

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[:0]	MK_LBYTE[7:0	Mono key high byte	0000_0000	Stereo
			X	Stereo
			0000_0110	MONO

Package Dimensions

- **E-LQFP 48L (7x7mm)**



Symbol	Dimension in mm	
	Min	Max
A	--	1.60
A1	0.05	0.15
b	0.17	0.27
c	0.09	0.20
D	6.90	7.10
D1	8.90	9.10
E	6.90	7.10
E1	8.90	9.10
e	0.50 BSC	
L	0.45	0.75

Exposed pad

	Dimension in mm	
	Min	Max
D2	4.31	5.21
E2	4.31	5.21

Revision History

Revision	Date	Description
0.1	2017.05.05	Initial version.
0.2	2017.08.24	1. Remove DIS_LVUV_FADE 2. Dis_HVUV default value
0.3	2017.10.13	1. Add fPWM SPEC
1.0	2017.10.18	Remove “Preliminary”
1.1	2017.11.16	1. Power on sequence: PVDD→PVCC & /PD→/SD 2. Power off sequence: PVDD→PVCC & /PD→/SD 3. page 36: PVDD→PVCC, AD82010 → AD87010
1.2	2018.01.10	1. Add “Protection Status Register” Table. 2. Modify Register Table. (0x2D, Error) 3. Modify “Power on sequence” figure. 4. Modfiy “Absolute Maximum Ratings” Table. (Add ESD SPEC.)
1.3	2018.03.05	1. Modify “Power on sequence” figure. 2. Add Note 8. 3.Modify “Register Table” .(A_SEL_FAULT) 4.Modify “Pin Description”. (A_SEL_FAULT at address 0x0D -> 0x02) 5.Modify “Absolute Maximum Ratings” Table.(1.Remove Charged Device Mode. 2. Add Machine Mode)
1.4	2018.05.08	1.Modify “Sample calculation for power clipping “ Table (Decimal Value: 524288 change to 2097152) 2.Change T9 time 20ms to 150ms 3.Change T7 time 0.1ms to 150ms
1.5	2018.09.10	1. Add Application Circuit Example for Mono.
1.6	2019.02.20	Add “output power vs. PVCC” figure.
1.7	2019.10.01	Modify Address 0X01 data. Power on sequence.
1.8	2021.04.13	Modify Register Table at Address 0X06. Modify Address 0X06 data.
1.9	2021.05.24	Modify Power on Sequence.

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