2X25W Stereo / 1X50W Mono Filter-less Digital Audio Amplifier

Features

- 16/18/20/24/32-bits input with I^2S, Left-alignment, Right-alignment and TDM data format
- 32 bits audio data path
- I^2S output with selectable Audio DSP point and gain control
- PSNR & DR (A-weighting)
  105dB (PSNR), 112dB (DR) @ 24V
- Multiple sampling frequencies (Fs)
  32kHz / 44.1kHz / 48kHz and
  64kHz / 88.2kHz / 96kHz
- System clock = 64x, 128x, 256x, 384x, 512x, 768x, 1024x Fs
  256x~1024x Fs for 32kHz / 44.1kHz / 48kHz
  128x~512x Fs for 64kHz / 88.2kHz / 96kHz
- Supply voltage
  PVCC: 4.5V~26V
  DVDD: 3.3V
  DVDDIO: 1.8V or 3.3V
- Loudspeaker output power for Stereo
  10W x 2ch into 8Ω @ 10% THD+N @ 13V
  15W x 2ch into 8Ω @ 10% THD+N @ 16V
  8.5W x 2ch into 8Ω @ 1% THD+N @ 12V
  20W x 2ch into 8Ω @ 1% THD+N @ 18V
  25W x 2ch into 8Ω@ 0.04% THD+N @ 24V
- Sounds processing including:
  Volume control (+24dB~-103dB, 0.125dB/step)
  Dynamic range control
  Power clipping
  Channel mixing
  User programmed noise gate with hysteresis window
  DC-blocking high-pass filter
  Pre-scale/Post-scale
  Compensate filter
- Anti-pop design
- I^2C control interface with selectable device address
- Internal PLL
- Dynamic temperature control
- Short circuit and over-temperature protection
- LV Under-voltage shutdown and HV Under-voltage detection
- DC detection function
- Clock detection function
- Filter-less solution (most cases with PVCC ≤14V)
- MCLK-less application

Applications

- TV audio
- Boom-box, CD and DVD receiver, docking system
- Powered speaker
- Wireless audio

Description

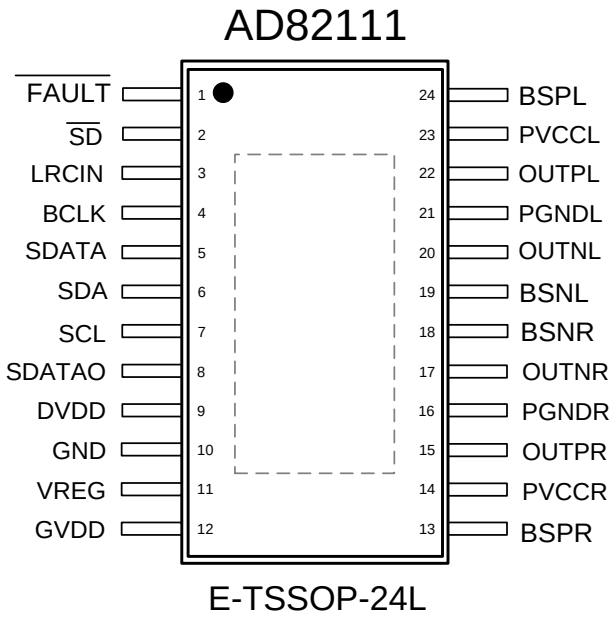
AD82111 is a digital audio amplifier capable of driving a pair of 8Ω,25W or a single 4Ω,50W speaker, both which operate with play music at a 24V supply .

Using I^2C digital control interface, the user can control AD82111's input format selection, mute and volume control functions. AD82111 has many built-in protection circuits to safeguard AD82111 from connection errors.

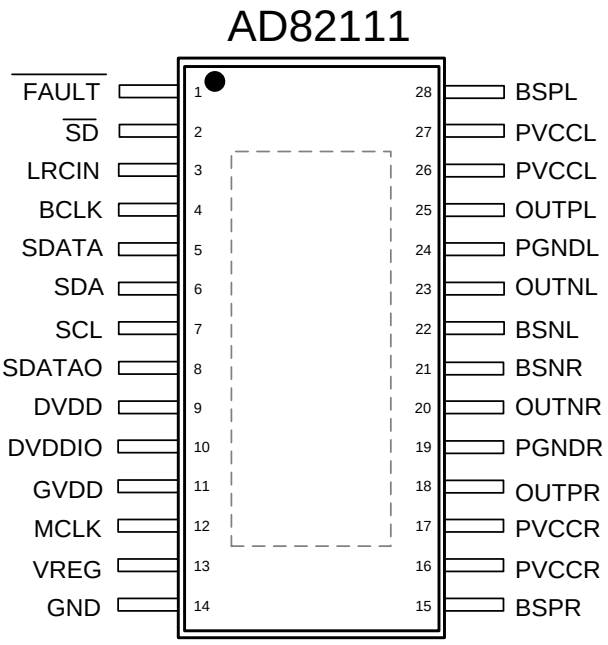
Ordering Information

Product ID	Package	Packing / MPQ	Comments
AD82111-QG24NRR	E-TSSOP 24L	2.5K Units / Reel 1 Reel / Small box	Green
AD82111-QG28NRR	E-TSSOP 28L	2.5K Units / Reel 1 Reel / Small Box	Green

Pin Assignment (Top View)



E-TSSOP-24L



E-TSSOP-28L

Pin Description (E-TSSOP 24L)

Pin	NAME	TYPE	DESCRIPTION	CHARACTERISTICS
1	$\overline{\text{FAULT}}$	DI/O	$\overline{\text{FAULT}}$ pin is a dual function pin. One is I^2C address setting during power up initial. After power up, it can be and indicator for error status report (low active) by setting register of A_SEL_FAULT at address 0x02 B[7] to enable it.	Schmitt trigger TTL input buffer
2	$\overline{\text{SD}}$	AI	Shut down, low active. Place the amplifier in Shutdown.	
3	LRCIN	DI	Left/Right clock input (Fs).	Schmitt trigger TTL input buffer

4	BCLK	DI	Bit clock input (64Fs).	Schmitt trigger TTL input buffer
5	SDATA	DI	Serial audio data input.	Schmitt trigger TTL input buffer
6	SDA	DI/O	I^2C bi-directional serial data.	Schmitt trigger TTL input buffer
7	SCL	DI	I^2C serial clock input.	Schmitt trigger TTL input buffer
8	SDATAO	DO	Serial audio data output.	Schmitt trigger TTL input buffer
9	DVDD	P	Digital Power.	
10	GND	P	Ground.	
11	VREG	P	1.8V Regulator voltage output, this pin must not be used to drive external devices.	
12	GVDD	P	5V Regulator voltage output. This pin must not be used to drive external devices.	
13	BSPR	P	Bootstrap capacitor connect pin for the OUTPR, it is used to create a power supply for the high-side gate drive for OUTPR.	
14	PVCCR	P	High-voltage power supply for right-channel. Right channel and left channel power supply inputs are connected internally.	
15	OUTPR	P	Positive output for right channel.	
16	PGNDR	P	Power ground for the H-bridges.	
17	OUTNR	O	Negative output for right channel.	
18	BSNR	P	Bootstrap capacitor connect pin for the OUTNR, it is used to create a power supply for the high-side gate drive for OUTNR.	
19	BSNL	P	Bootstrap capacitor connect pin for the OUTNL, it is used to create a power supply for the high-side gate drive for OUTNL.	
20	OUTNL	O	Negative output for left channel.	
21	PGNDL	P	Power ground for the H-bridges.	
22	OUTPL	O	Positive output for left channel.	
23	PVCCL	P	High-voltage power supply for left-channel. Right channel and	

			left channel power supply inputs are connected internally.	
24	BSPL	P	Bootstrap capacitor connect pin for the OUTPL, it is used to create a power supply for the high-side gate drive for OUTPL.	
Thermal land	Connect to the system ground.			

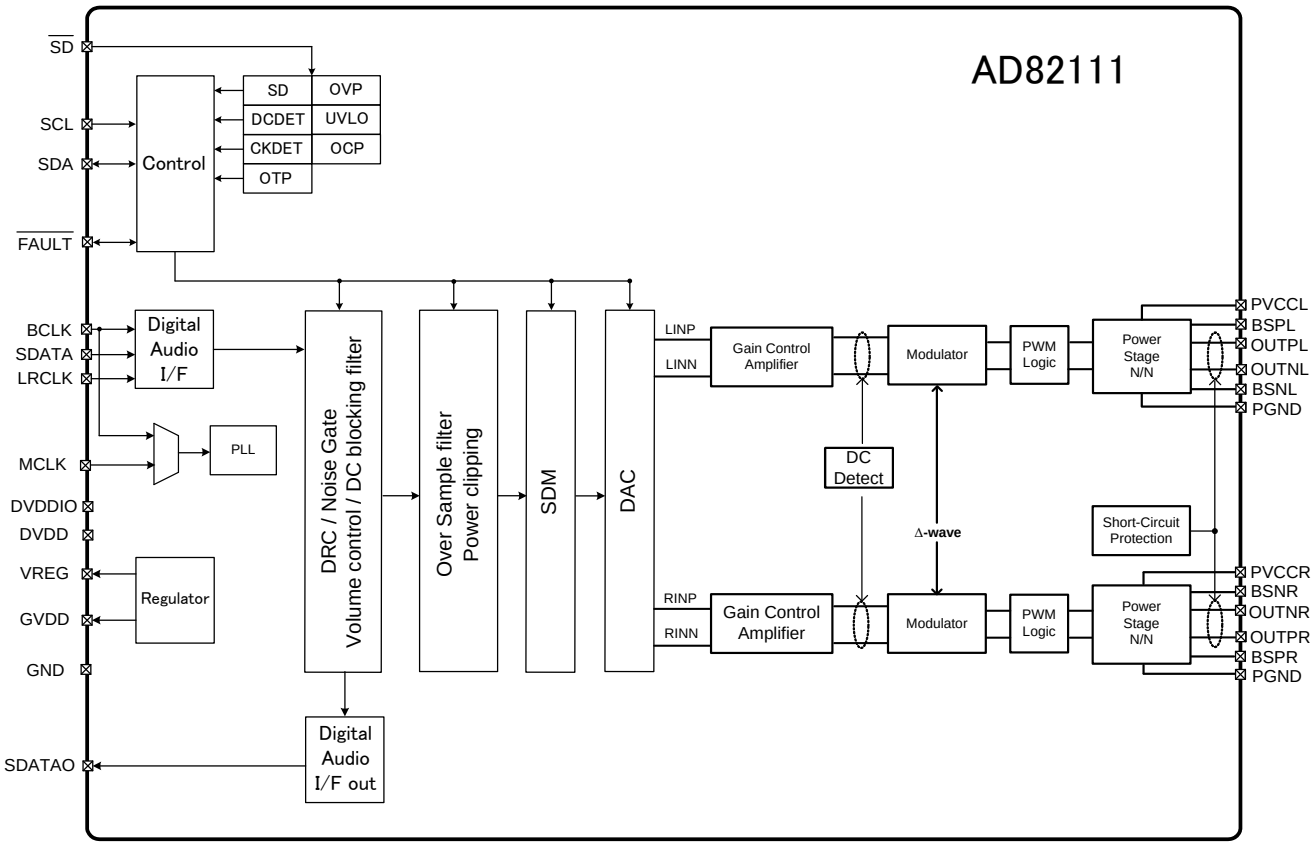
Pin Description (E-TSSOP 28L)

Pin	NAME	TYPE	DESCRIPTION	CHARACTERISTICS
1	$\overline{\text{FAULT}}$	DI/O	$\overline{\text{FAULT}}$ pin is a dual function pin. One is I^2C address setting during power up initial. After power up, it can be and indicator for error status report (low active) by setting register of A_SEL_FAULT at address 0x02 B[7] to enable it.	Schmitt trigger TTL input buffer
2	$\overline{\text{SD}}$	AI	Shut down, low active. Place the amplifier in Shutdown.	
3	LRCIN	DI	Left/Right clock input (Fs).	Schmitt trigger TTL input buffer
4	BCLK	DI	Bit clock input (64Fs).	Schmitt trigger TTL input buffer
5	SDATA	DI	Serial audio data input.	Schmitt trigger TTL input buffer
6	SDA	DI/O	I^2C bi-directional serial data.	Schmitt trigger TTL input buffer
7	SCL	DI	I^2C serial clock input.	Schmitt trigger TTL input buffer
8	SDATAO	DO	Serial audio data output.	
9	DVDD	P	Digital Power.	
10	DVDDIO	P	I/O Power.	
11	GVDD	P	5V Regulator voltage output. This pin must not be used to drive external devices.	
12	MCLK	DI	Master clock input.	Schmitt trigger TTL input buffer, internal pull Low with a 100Kohm resistor.
13	VREG	P	1.8V Regulator voltage output, this pin must not be used to drive	

			external devices.	
14	GND	P	Ground.	
15	BSPR	P	Bootstrap capacitor connect pin for the OUTPR, it is used to create a power supply for the high-side gate drive for OUTPR	
16,17	PVCCR	P	High-voltage power supply for right-channel. Right channel and left channel power supply inputs are connected internally.	
18	OUTPR	O	Positive output for right channel.	
19	PGNDR	P	Power ground for the H-bridges.	
20	OUTNR	O	Negative output for right channel.	
21	BSNR	P	Bootstrap capacitor connect pin for the OUTNR, it is used to create a power supply for the high-side gate drive for OUTNR	
22	BSNL	P	Bootstrap capacitor connect pin for the OUTNL, it is used to create a power supply for the high-side gate drive for OUTNL.	
23	OUTNL	O	Negative output for left channel.	
24	PGNDL	P	Power ground for the H-bridges.	
25	OUTPL	O	Positive output for left channel.	
26,27	PVCCL	P	High-voltage power supply for left-channel. Right channel and left channel power supply inputs are connected internally.	
28	BSPL	P	Bootstrap capacitor connect pin for the OUTPL, it is used to create a power supply for the high-side gate drive for OUTPL.	
Thermal land			Connect to the system ground.	

Note 1: AI = Analog input; AO = Analog output; AI/O = Analog Bi-directional (input and output); DI = Digital Input; DO = Digital Output; DI/O = Digital Bi-directional (input and output); P = Power or Ground

Functional Block Diagram



Available Package

Package Type	Device No.	θ ja(℃/W)	Ψ jt(℃/W)	θ jt(℃/W)	Exposed Thermal Pad
E-TSSOP 24L	AD82111	30.9	0.5	29.6	Yes (Note2)
E-TSSOP 28L		29.1	0.3	29.6	

Note 2.1: The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is suggested.

Note 2.2: θ_{ja} is measured on a room temperature (T_A=25 ℃), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The measurement is tested using the JEDEC51-5 thermal measurement standard.

Note 2.3: θ_{jt} represents the heat resistance for the heat flow between the chip and the package's top surface.

Note 2.4: Ψ_{jt} represents the heat resistance for the heat flow between the chip and the package's top surface center.

Absolute Maximum Ratings

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device.

Symbol	Parameter		Min	Max	Units
DVDD	Supply for Digital Circuit		-0.3	3.6	V
DVDDIO	Supply for Digital I/O Circuit		-0.3	3.6	V
PVCCL/R	Supply for Driver Stage		-0.3	30	V
V_i	Input Voltage		-0.3	3.6	V
T_{stg}	Storage Temperature		-65	150	°C
T_J	Junction Operating Temperature		-40	150	°C
R_L	Minimum Load Resistance	BTL: 4.5V≦PVDD≦16V	3.2		Ω
		BTL: 16V＜PVDD≦24V	4.8		Ω
		PBTL: 4.5V≦PVDD≦16V	1.6		Ω
		PBTL: 16V＜PVDD≦24V	2.4		Ω
ESD	Human Body Model			±2K	V
	Charged Device Model			±750	
P_d	Power Dissipation at T_A=25℃			4.66	W

Recommended Operating Conditions

Symbol	Parameter	Typ.	Units
DVDD	Supply for Digital Circuit	3.0~3.6	V
DVDDIO	Supply for Digital I/O Circuit for 1.8V	1.65~1.95	V
	Supply for Digital I/O Circuit for 3.3V	3.0~3.6	
PVCCL/R	Supply for Driver Stage	4.5~26	V
T_J	Junction Operating Temperature	-40~125	°C
T_A	Ambient Operating Temperature	-40~85	°C

Marking Information

AD82111

Line 1 : LOGO

Line 2 : Product no.

Line 3 : Tracking Code

E-TSSOP-24L / E-TSSOP-28L

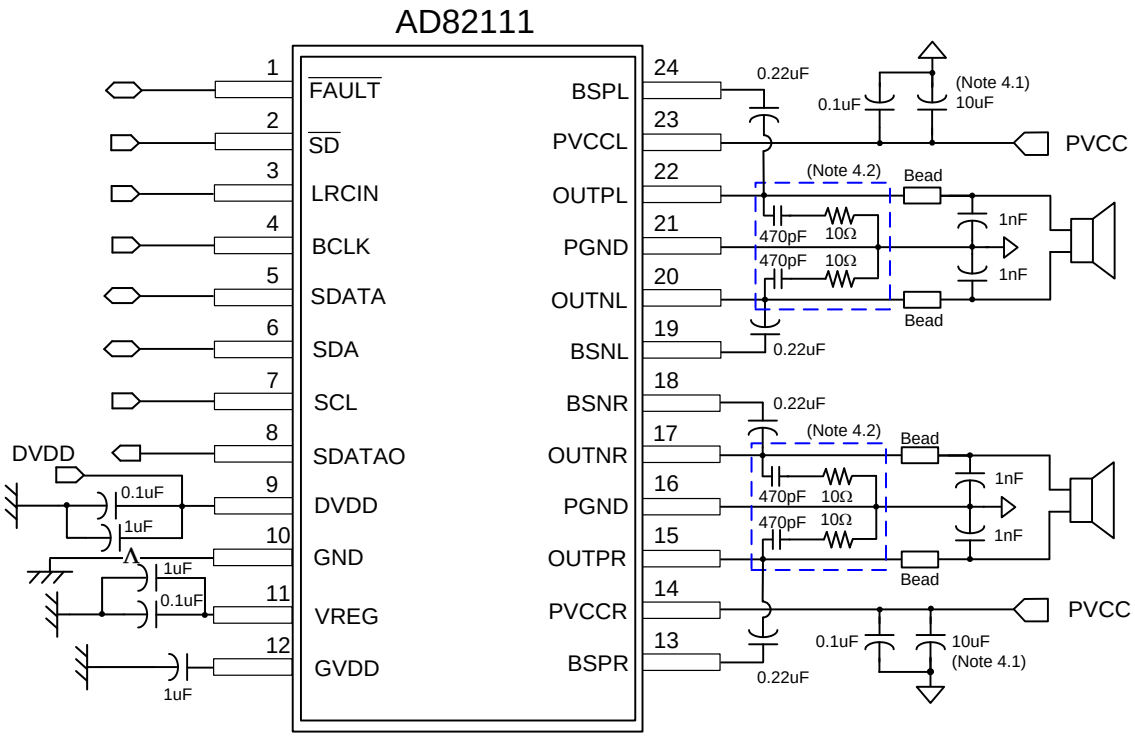
General Electrical Characteristics

Condition: T_A=25 °C (unless otherwise specified).

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{SD(PVCC)}$	PVCC Supply Current during Shutdown	PVCC=24V		21		uA
$I_{SD(DVDD+DVDDIO)}$	DVDD+DVDDIO Supply Current during Shutdown	DVDD=3.3V & DVDDIO=3.3V	0.1	1	2	mA
$I_{Q(PVCC)}$	PVCC Supply Current During Standby (PWM 50% / 50% duty after de-mute)	PVCC=24V		17		mA
		PVCC=12V		15		mA
$I_{Q(DVDD+DVDDIO)}$	Quiescent current for DVDD+DVDDIO	DVDD=3.3V & DVDDIO=3.3V	2	9	18	mA
T_{SENSOR}	Junction Temperature for Driver Shutdown			160		°C
	Temperature Hysteresis for Recovery from Shutdown			35		°C
$DVDDUV_H$	Under Voltage Disabled (For DVDD)			2.9		V
$DVDDUV_L$	Under Voltage Enabled (For DVDD)			2.6		V
$PVCCUV_H$	Under Voltage Disabled (For PVCC)			10.4		V
$PVCCUV_L$	Under Voltage Enabled (For PVCC)			9.7		V
Rds-on	Static Drain-to-Source On-state Resistor, NMOS	PVCC=24V, Id=500mA		150		mΩ
GVDD	5V Regulator voltage output.			5		V
VREG	1.8V Regulator voltage output.			1.8		V
I_{SC}	L(R) Channel Over-Current Protection (Note 3)			8		A
V_{IH}	High-Level Input Voltage	DVDDIO=3.3V	2.0			V
V_{IL}	Low-Level Input Voltage	DVDDIO=3.3V			0.8	V
V_{IH}	High-Level Input Voltage	DVDDIO=1.8V	1.26			V
V_{IL}	Low-Level Input Voltage	DVDDIO=1.8V			0.54	V
V_{OH}	High-Level Output Voltage	DVDDIO=3.3V	2.64			V
V_{OL}	Low-Level Output Voltage	DVDDIO=3.3V			0.73	V
V_{OH}	High-Level Output Voltage	DVDDIO=1.8V	1.44			V
V_{OL}	Low-Level Output Voltage	DVDDIO=1.8V			0.4	V
C_I	Input Capacitance			6.4		pF
f_{PWM}	PWM Frequency	FSW=0		300		KHz
		FSW=1		600		

Note 3: Loudspeaker over-current protection is only effective when loudspeaker drivers are properly connected with external LC filters. Please refer to the application circuit example for recommended LC filter configuration.

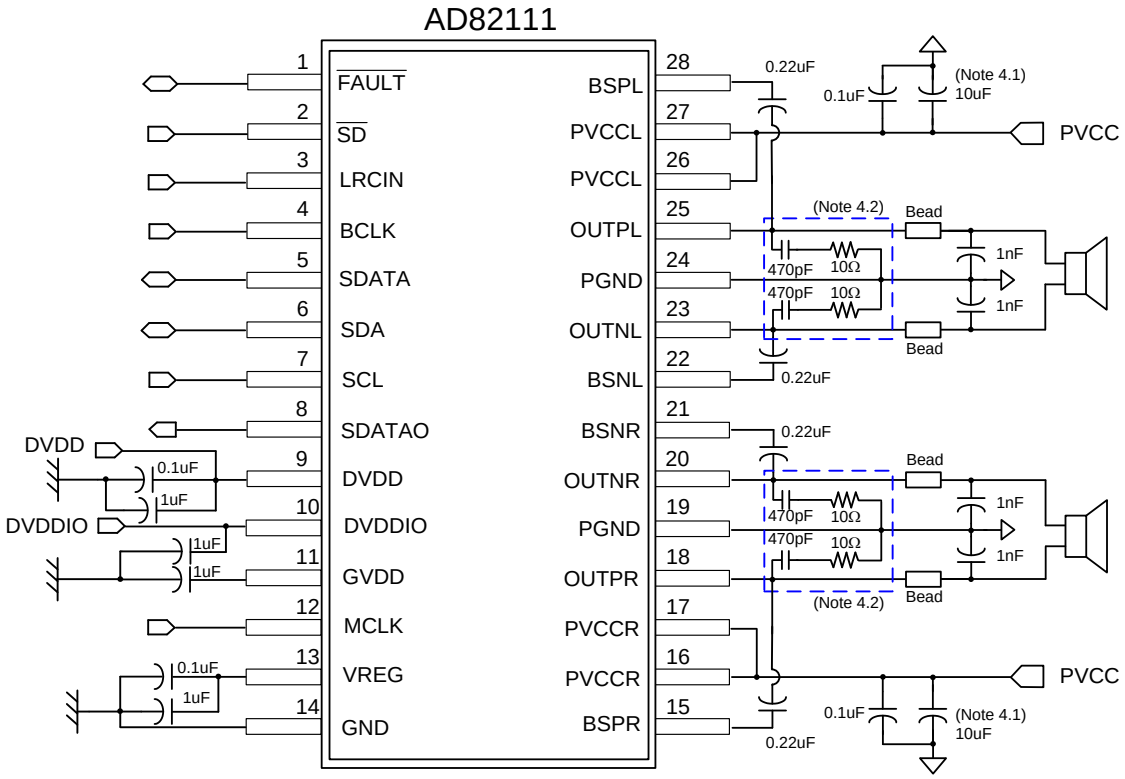
Application Circuit Example for E-TSSOP 24L Stereo



Note 4.1: PVCC needs increasing to 100uFx2 if the power ripple > 500mVpp.

Note 4.2: Option for EMI.

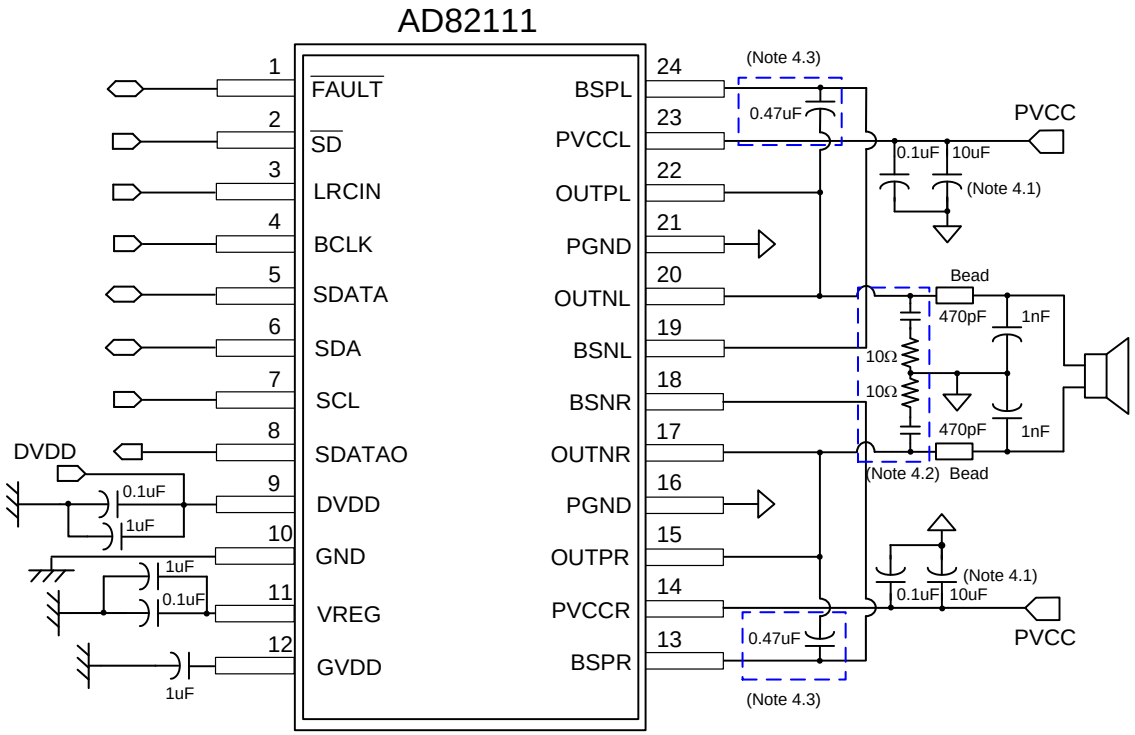
Application Circuit Example for E-TSSOP 28L Stereo



Note 4.1: PVCC needs increasing to 100uFx2 if the power ripple > 500mVpp.

Note 4.2: Option for EMI.

Application Circuit Example for E-TSSOP 24L Mono

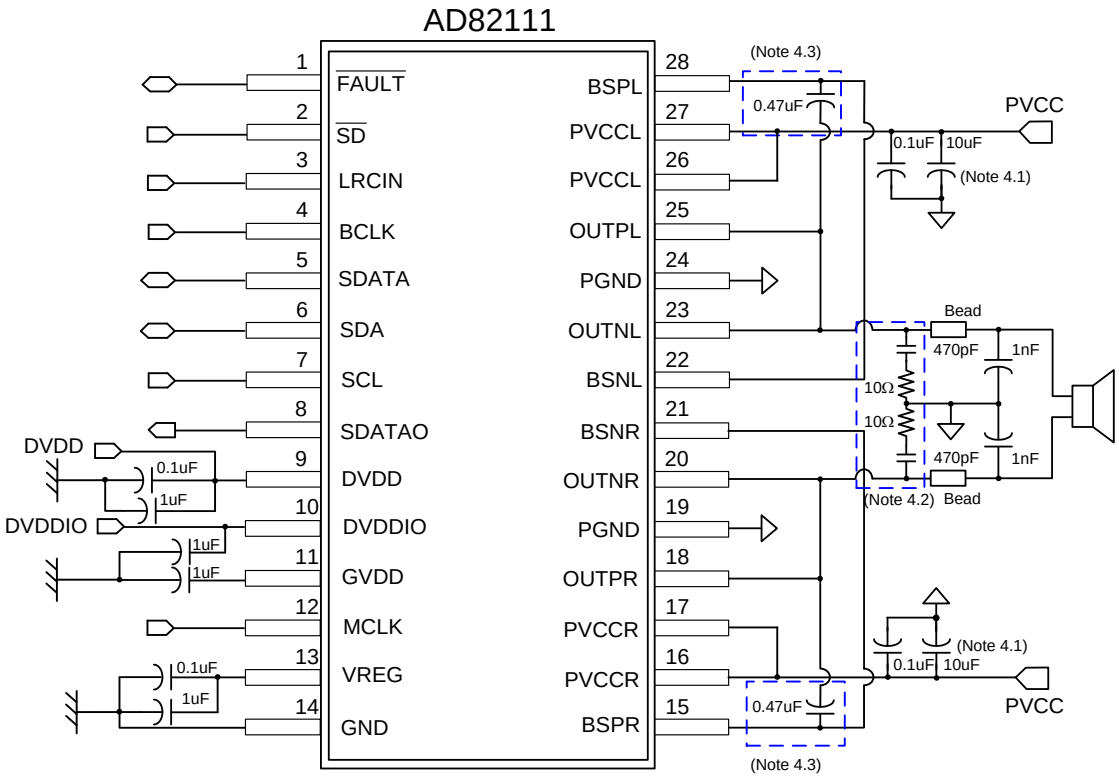


Note 4.1: PVCC needs increasing to 100uFx2 if the power ripple > 500mVpp.

Note 4.2: Option for EMI.

Note 4.3: C_{BST} need increasing to 1uF if the R_{Load} = 2Ω.

Application Circuit Example for E-TSSOP 28L Mono



Note 4.1: PVCC needs increasing to 100uFx2 if the power ripple > 500mVpp.

Note 4.2: Option for EMI.

Note 4.3: C_{BST} need increasing to 1uF if the R_{Load} = 2Ω.

Electrical Characteristics and Specifications for Loudspeaker (Stereo)

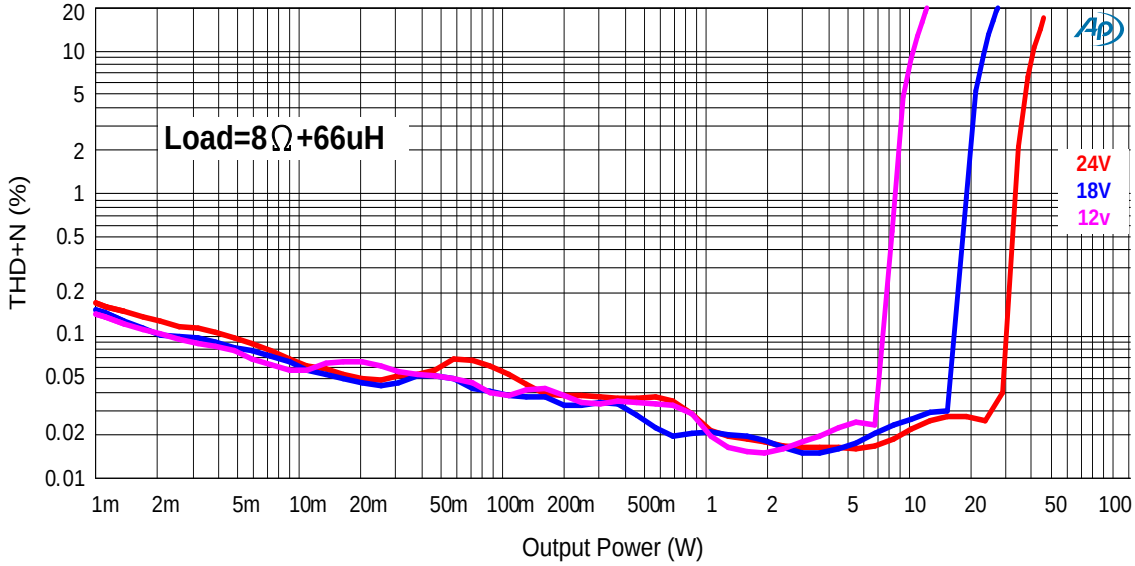
Condition: T_A=25 °C, DVDD=3.3V, PVCCL=PVCCR=24V, F_S=48kHz, Load=8Ω ; Input is 1kHz sine wave. Volume is 0dB unless otherwise specified.

Symbol	Parameter	Condition	Input Level	Min	Typ	Max	Units
P_O	Output Power (Note 6)	THD+N=0.03%, f=1kHz, PVCC=24V			25		W
		THD+N=10%, f=1kHz, PVCC=12V, R_L=4Ω			18.4		W
		THD+N=10%, f=1kHz, PVCC=12V, R_L=8Ω			10.2		W
THD+N	Total Harmonic Distortion + Noise	P_O=10W, f=1kHz			0.025		%
		P_O=5W, f=1kHz			0.017		%
Vn	Noise	R_L=8Ω, A-Weighted Filter			110		uV
SNR	Signal to Noise Ratio (Note 5)	Maximum output at THD+N=1%, f=1kHz, PVCC=12			98		dB
		Maximum output at THD+N=1%, f=1kHz, PVCC=24			103		
DR	Dynamic Range (Note 5)		-60dB		110		dB
PSRR	Power Supply Rejection Ratio	V_{RIPPLE}=200mVpp noise injected at 1kHz			70		dB
X-talk	Channel Separation	P_O=1W at 1kHz			88		dB

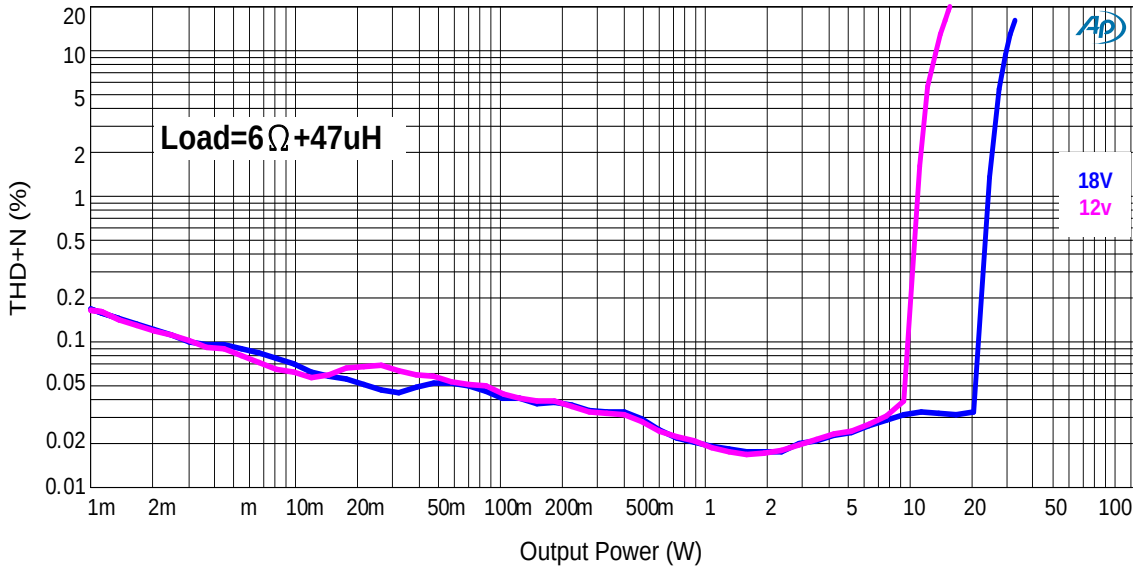
Note 5: Measured with A-weighting filter.

Note 6: Thermal dissipation is limited by package type and PCB design, the external heat-sink or system cooling method should be adopted for RMS power output.

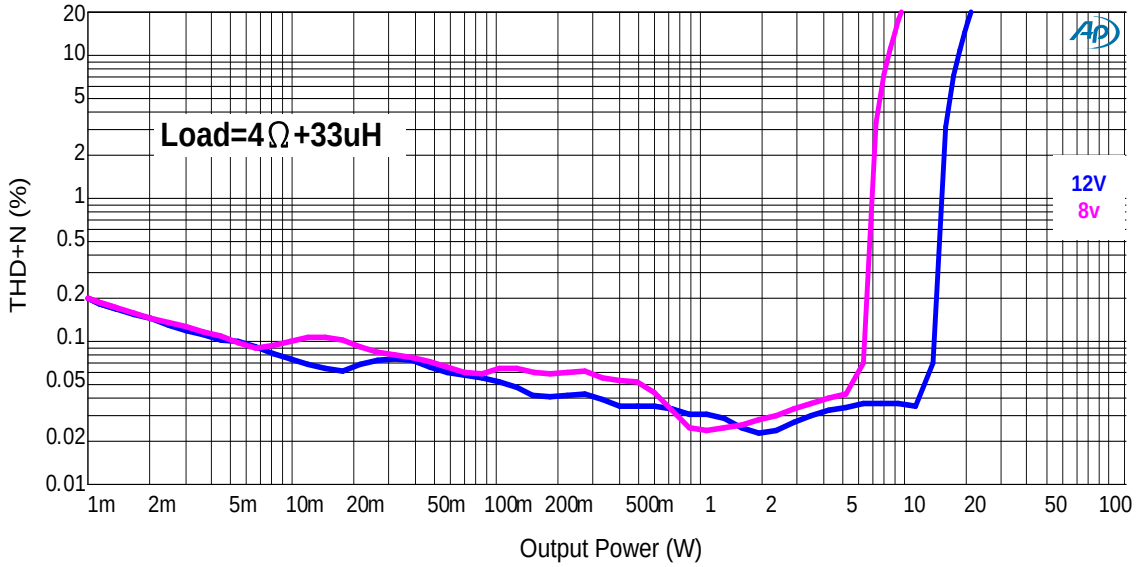
THD + N (%) vs. Output power (8Ω load)



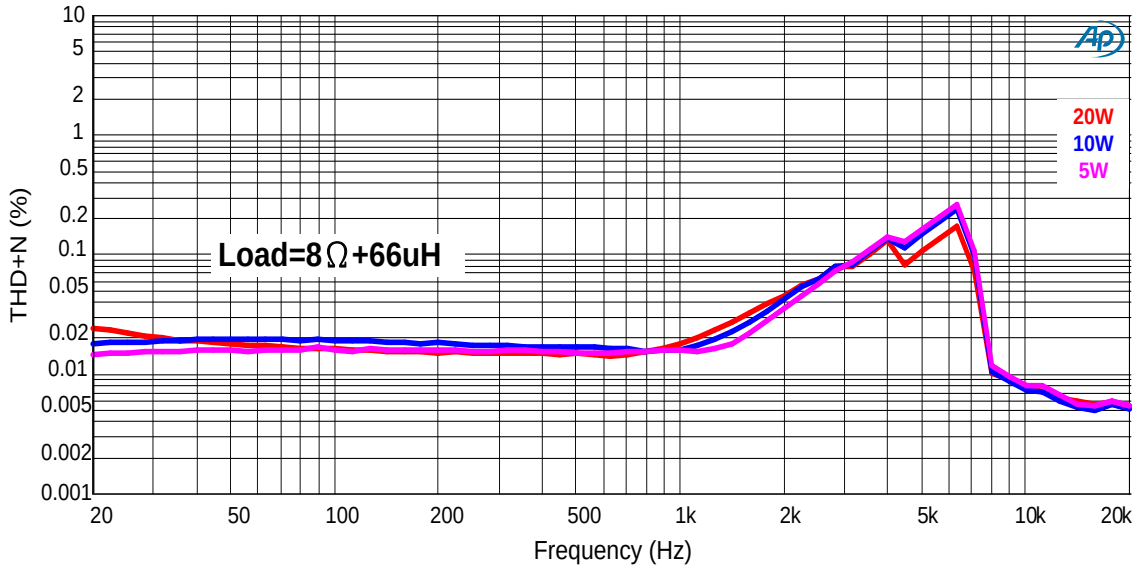
THD + N (%) vs. Output power (6Ωload)



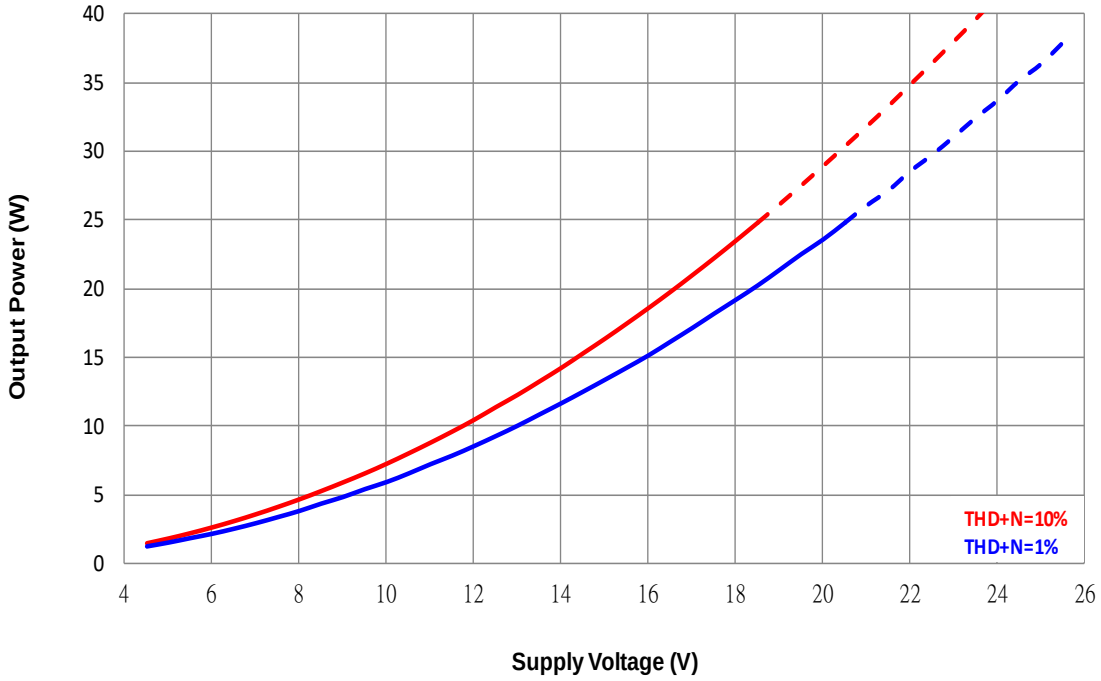
THD + N (%) vs. Output power (4Ωload)



THD + N (%) vs. Frequency (24V 8Ωload)

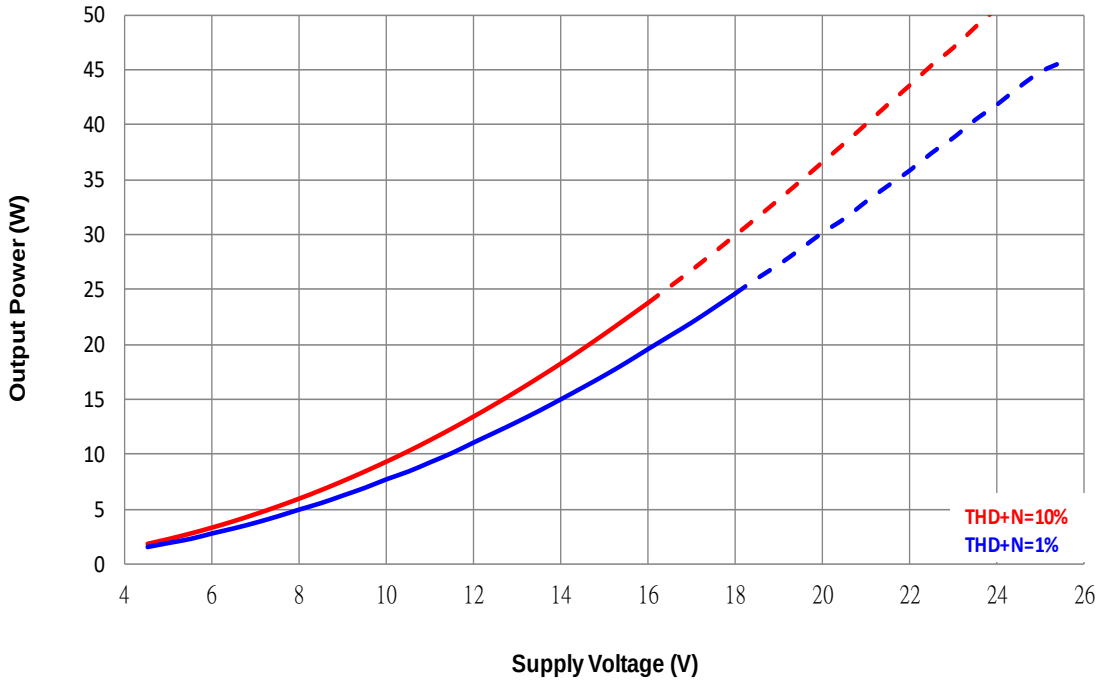


AD82111_8ohm stereo (f_{PWM}=300kHz)



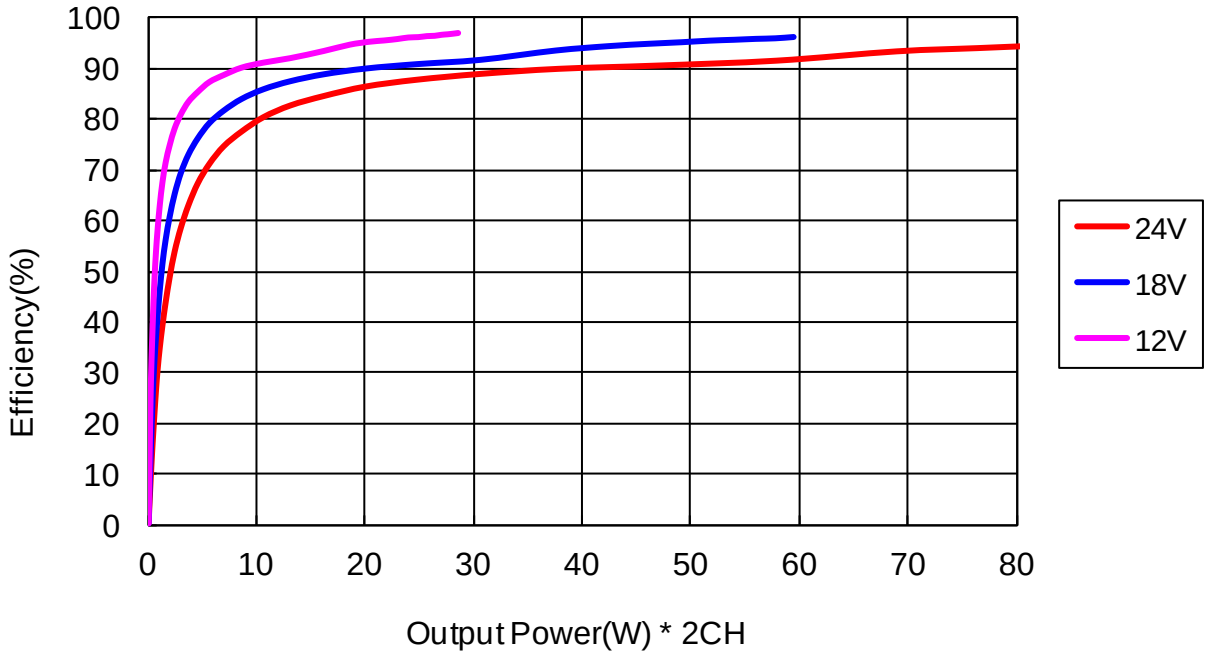
Note: Dashed Line represent thermally limited regions for the continuous output power.

AD82111_6ohm stereo (f_{PWM}=300kHz)

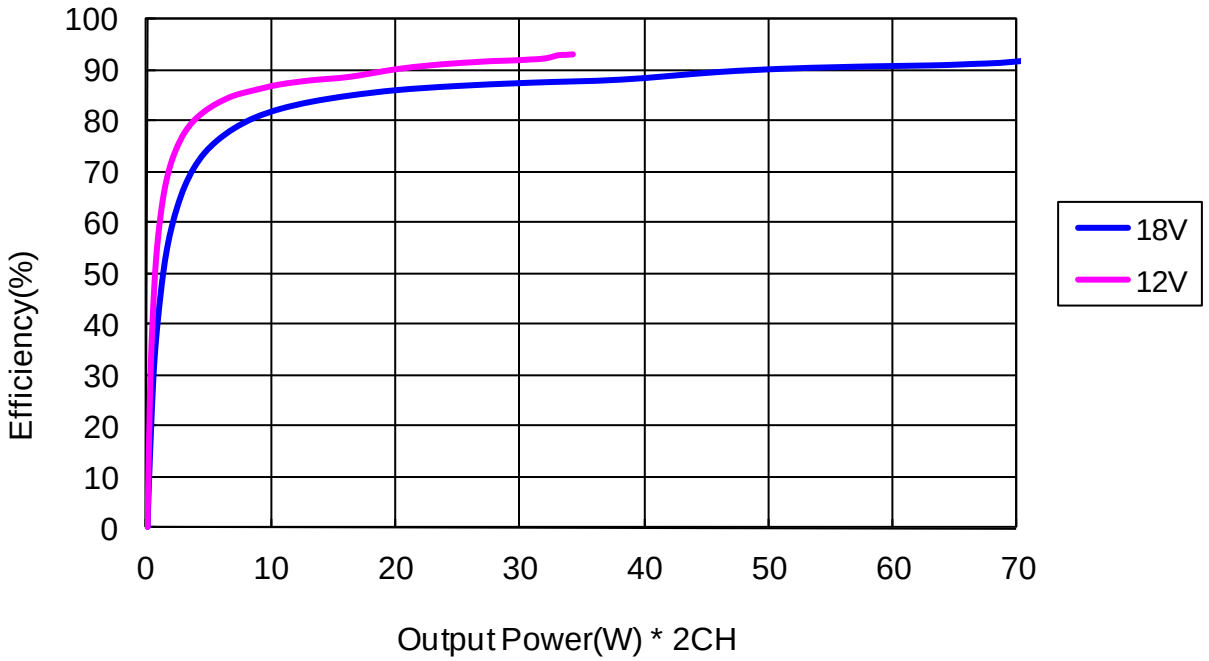


Note: Dashed Line represent thermally limited regions for the continuous output power.

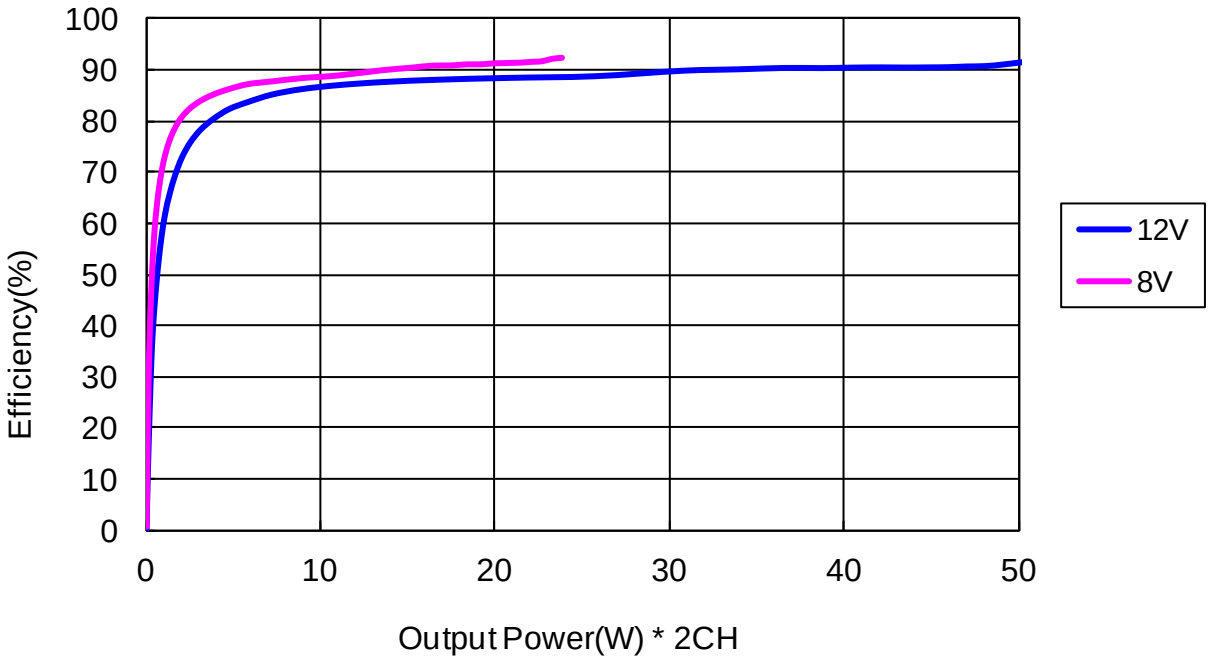
Efficiency (Stereo 8Ωload) / 2ch



Efficiency (Stereo 6Ωload) / 2ch



Efficiency (Stereo 4Ωload) / 2ch



Electrical Characteristics and Specifications for Loudspeaker (Mono)

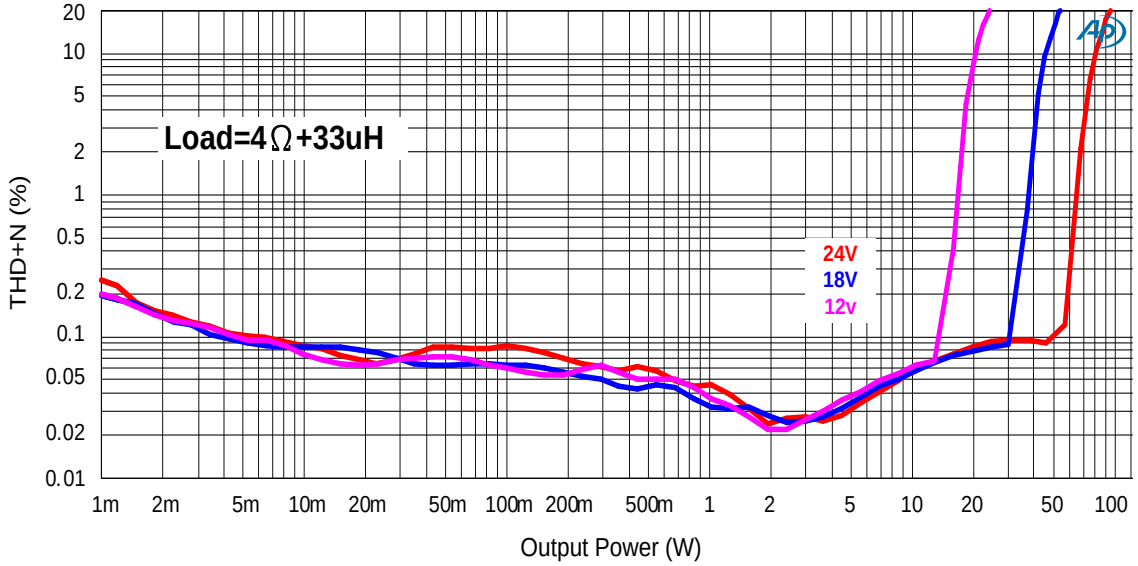
Condition: T_A=25 °C, DVDD=3.3V, PVCCL=PVCCR=24V, F_S=48kHz, Load=4Ω ; Input is 1kHz sine wave. Volume is 0dB unless otherwise specified.

Symbol	Parameter	Condition	Input Level	Min	Typ	Max	Units
P_O	Output Power (Note 6)	THD+N=0.1%, f=1kHz, PVCC=24V			50		W
		THD+N=10%, f=1kHz, PVCC=12V			20.5		W
THD+N	Total Harmonic Distortion + Noise	P_O=20W, f=1kHz			0.085		%
Vn	Noise	R_L=4Ω,A-Weighted Filter			100		uV
SNR	Signal to Noise Ratio (Note 5)	Maximum output at THD+N=1%, f=1kHz,			104		dB
DR	Dynamic Range (Note 5)	-60dB of input level			110		dB

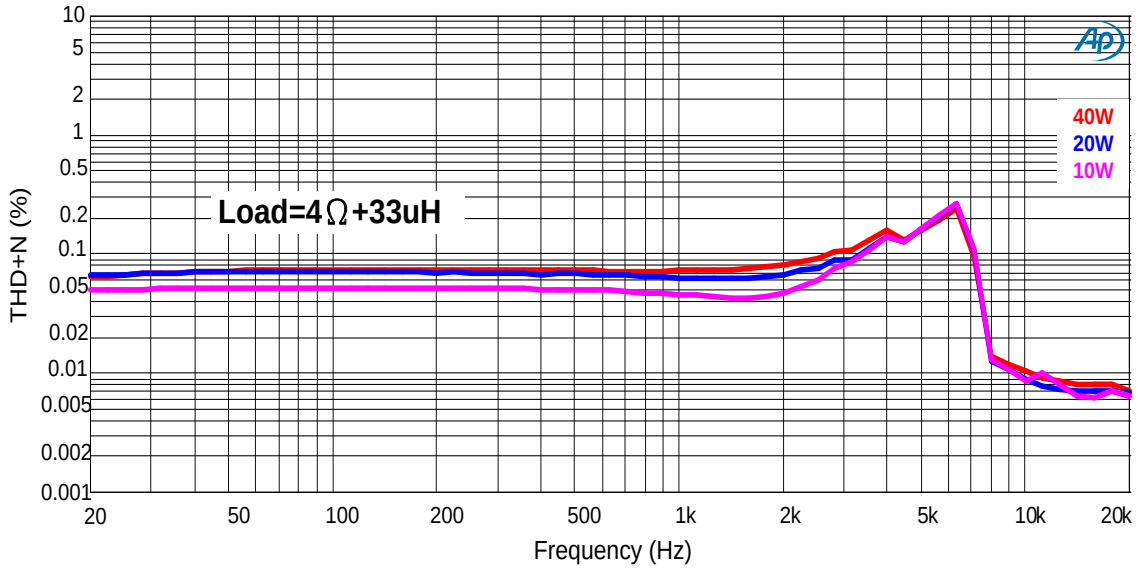
Note 5: Measured with A-weighting filter.

Note 6: Thermal dissipation is limited by package type and PCB design, the external heat-sink or system cooling method should be adopted for RMS power output.

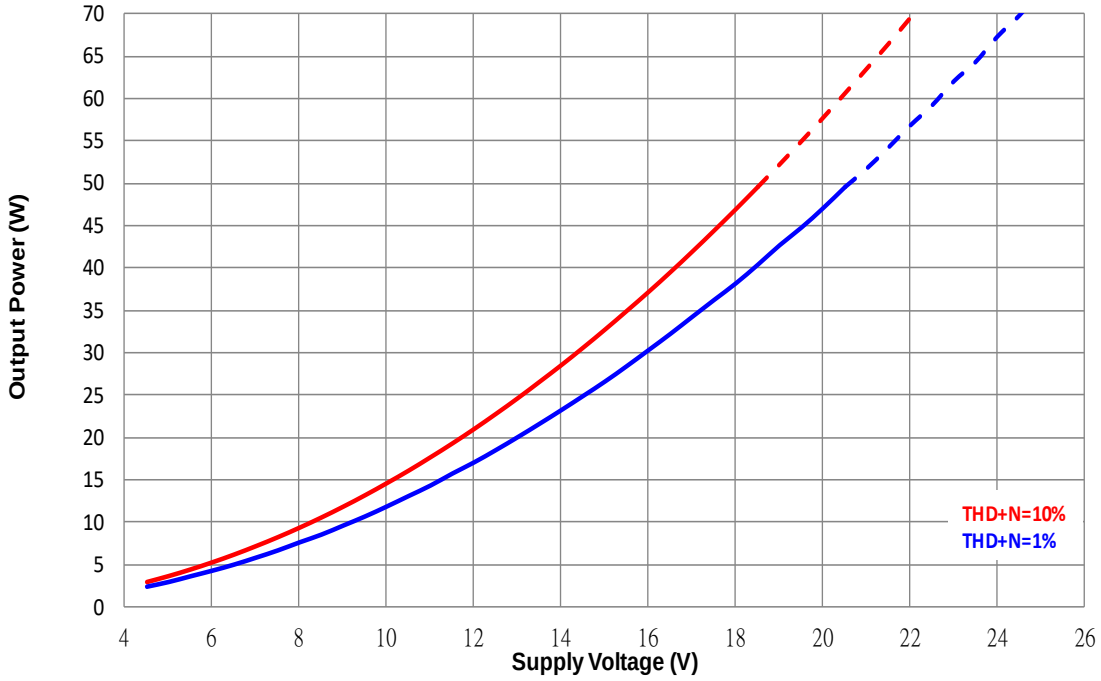
THD + N (%) vs. Output power (Mono 4Ωload)



THD + N (%) vs. Frequency (24V Mono 4Ωload)

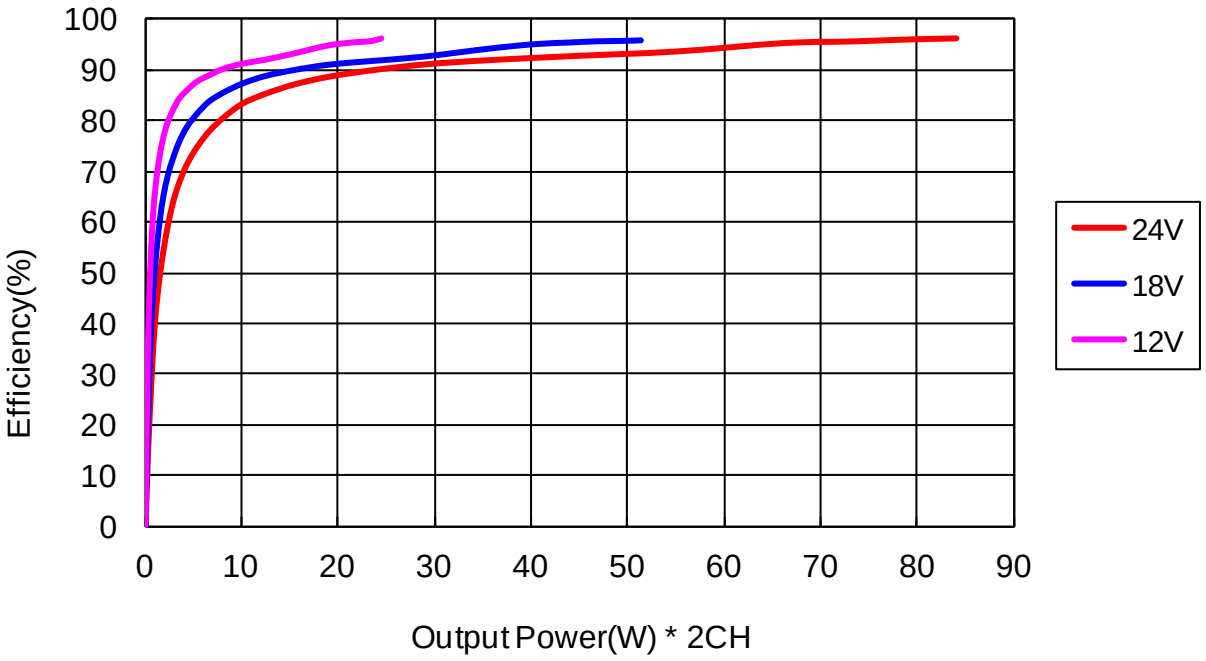


AD82111_4ohm Mono (f_{PWM}=300kHz)



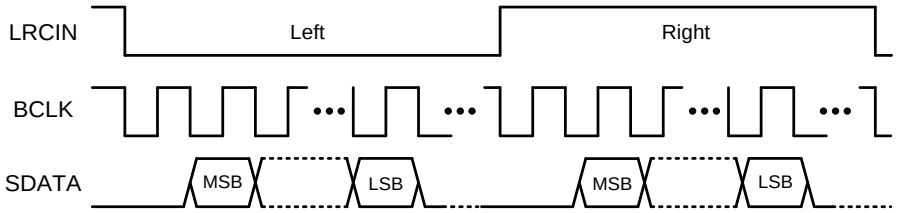
Note: Dashed Line represent thermally limited regions for the continuous output power.

Efficiency (Mono 4Ωload)

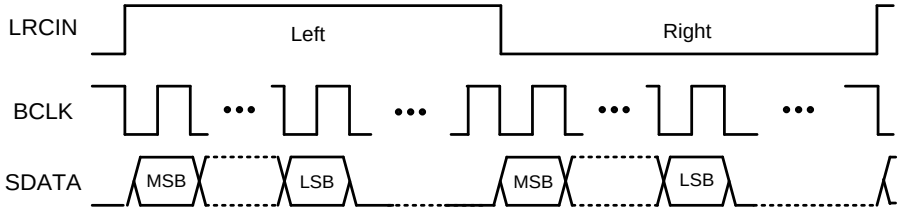


Interface Configuration

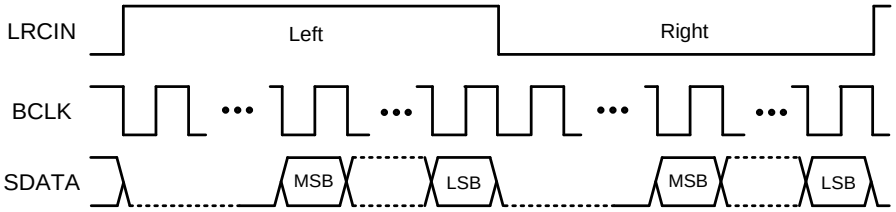
- I^2S



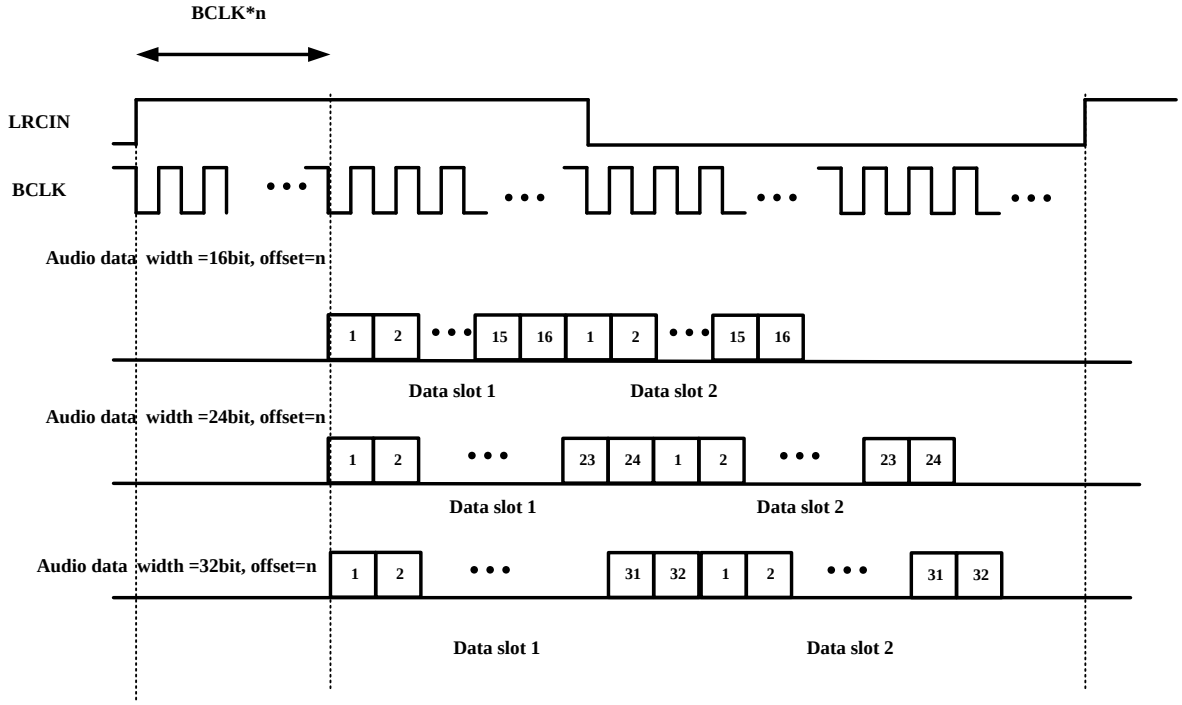
- Left-Alignment



- Right-Alignment



- TDM



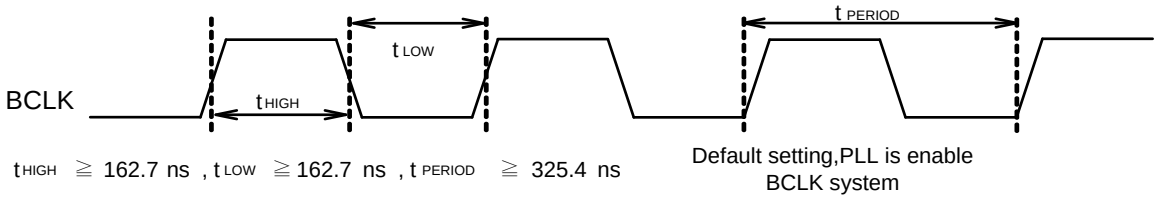
AD82111 device Audio Data Formats, Bit Depths, Clock Rates, and channel numbers

Format	Data Bits	Maximum LRCIN Frequency (KHz)	BCLK Rate (FS)	Channel numbers
I^2S/LJ/RJ	32	48, 96	64x	2
TDM	32, 16	48, 96	64x, 128x, 256x for 32 data bits 128x, 256x for 16 data bits	2,4,8 channels for 32 data bits 8,16 channels for 16 data bits

AD82111 device Audio Data Formats, Bit Depths, Clock Rates, and channel numbers (MCLK system)

Format	Data Bits	Maximum LRCIN Frequency (KHz)	MCLK Rate (FS)	BCLK Rate (FS)	Channel numbers
I^2S/LJ/RJ	32, 24, 20, 16	48, 96	64~1024x for 48K FS 64~512x for 96K FS	32x, 48x, 64x	2
TDM	32, 24, 20, 16	48	64~1024x	32x, 64x, 128x, 256x for 32 data bits 24x, 48x, 96x, 192x for 24 data bits 20x, 40x, 80x, 160x for 20 data bits 16x, 32x, 64x, 128x, 256x for 16 data bits	1,2,4,8 channels for 32/24/20 data bits 1,2,4,8,16 channels for 16 data bits
		96	64~512x		

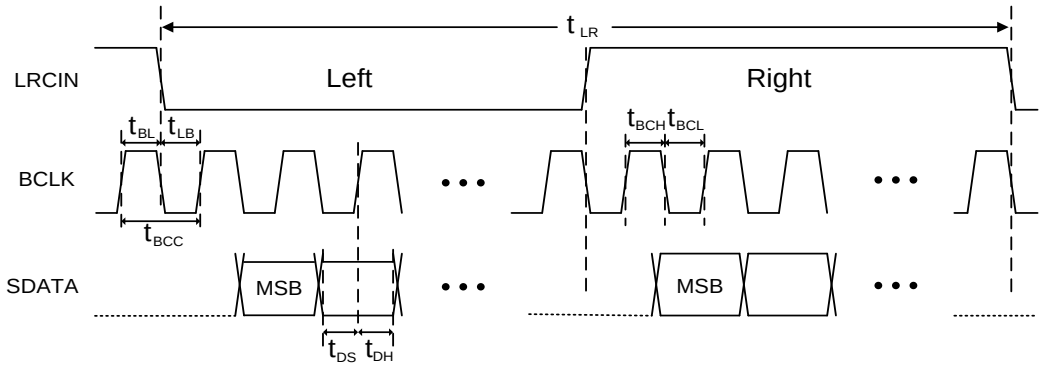
- System Clock Timing



t_{HIGH} ≧ 162.7 ns , t_{LOW} ≧ 162.7 ns , t_{PERIOD} ≧ 325.4 ns

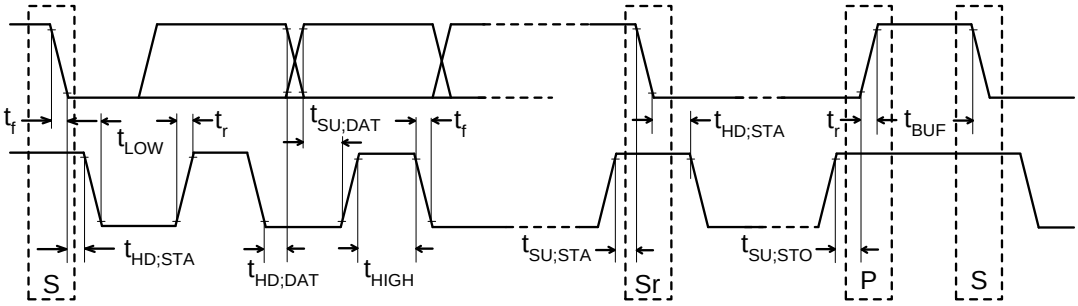
Default setting,PLL is enable
BCLK system

- Timing Relationship (Using I^2S format as an example)



Symbol	Parameter	Min	Typ	Max	Units
t_{LR}	LRCIN Period ($1/F_S$)	5.2		31.25	us
t_{BL}	BCLK Rising Edge to LRCIN Edge	50			ns
t_{LB}	LRCIN Edge to BCLK Rising Edge	50			ns
t_{BCC}	BCLK Period ($1/64F_S$)	162.76		488.3	ns
t_{BCH}	BCLK Pulse Width High	40.69		244	ns
t_{BCL}	BCLK Pulse Width Low	40.69		244	ns
t_{DS}	SDATA Set-Up Time	50			ns
t_{DH}	SDATA Hold Time	50			ns

- I^2C Timing

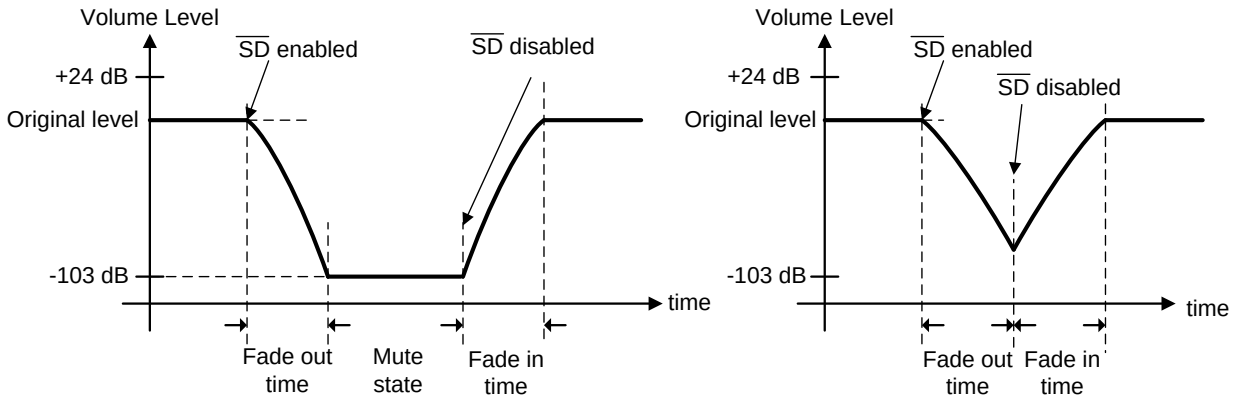


Parameter	Symbol	Standard Mode		Fast Mode		Unit
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time for repeated START condition	$t_{HD,STA}$	4.0	---	0.6	---	us
LOW period of the SCL clock	t_{LOW}	4.7	---	1.3	---	us
HIGH period of the SCL clock	t_{HIGH}	4.0	---	0.6	---	us
Setup time for repeated START condition	$t_{SU;STA}$	4.7	---	0.6	---	us
Hold time for I^2C bus data	$t_{HD;DAT}$	0	3.45	0	0.9	us
Setup time for I^2C bus data	$t_{SU;DAT}$	250	---	100	---	ns
Rise time of both SDA and SDL signals	t_r	---	1000	20+0.1Cb	300	ns
Fall time of both SDA and SDL signals	t_f	---	300	20+0.1Cb	300	ns
Setup time for STOP condition	$t_{SU;STO}$	4.0	---	0.6	---	us
Bus free time between STOP and the next START condition	t_{BUF}	4.7	---	1.3	---	us
Capacitive load for each bus line	C_b		400		400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	$0.1V_{DD}$	---	$0.1V_{DD}$	---	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	$0.2V_{DD}$	---	$0.2V_{DD}$	---	V

Operation Description

- Shut down control

AD82111 has a built-in volume fade-in / fade-out design for SD / Mute function. The relative SD timing diagrams for loudspeakers are shown below.



$$(10^{\frac{target(dB)}{20}} - 10^{\frac{original(dB)}{20}}) x 128 x (1/96K)$$

(Note: Address 0x16 B[3:2] = 00)

The volume level will be decreased to -∞dB in several LRCIN cycles. Once the fade-out procedure is finished, AD82111 will turn off the power stages, clock signals (for digital circuits) and current (for analog circuits). After $\overline{SD}$ pin is pulled low, AD82111 requires T_{fade} to finish the aforementioned work before entering power down state. Users can not program AD82111 during power down state. Also, all settings in the registers will remain intact unless DVDD is removed.

If the $\overline{SD}$ signal is removed during the fade-out procedure (above, right figure), AD82111 will still execute the fade-in procedure. In addition, AD82111 will establish the analog circuits' bias current and send the clock signals to digital circuits. Afterwards, AD82111 will return to its normal status.

- Internal PLL

AD82111 has a built-in PLL with multiple MCLK/FS ratio or BCLK/FS ratio to create the higher rate clocks required by the DSP. It is selected via register 0x01.

- Anti-pop design

AD82111 will generate appropriate control signals to suppress pop sounds during initial power on/off, power down/up, mute, and volume level changes.

- I^2C chip select

  $\overline{FAULT}$ is an input pin during power start-up. It can be pulled high (15-kΩ pull up) or low (15-kΩ pull down) for I^2C address selection. Low indicates an I^2C address of 0x30, and high an address of 0x34.

- Dynamic temperature control

  To avoid thermal shut down, AD82111 provides dynamic temperature control. When the junction temperature increases and exceeds the DTC attack threshold, AD82111 will lower the audio output by decreasing the volume. Once the junction temperature decreases and is below the DTC release threshold, AD82111 recovers to current volume setting.

- Clock detection

  AD82111 has clock error handling that uses the built-in oscillator clock to quickly detect changes / errors. Once the system detects the clock change / error, it will turn off the output and then force the oscillator clock as the reference clock of PLL. If the clocks are stable, the system will detect automatically and the system will revert to normal operation. During this process, AD82111 will fade in to the current volume setting.

- Self-protection circuits

  AD82111 has built-in protection circuits including thermal, short-circuit and under-voltage detection circuits.

  (i) When the internal junction temperature is higher than 160℃, power stages will be turned off and AD82111 will return to normal operation once the temperature drops to 125℃. The temperature values may vary around 10%.

  (ii) The short-circuit protection circuit protects the output stage when the wires connected to loudspeakers are shorted to each other or PGND/PVCC. For normal 24V operations, the current flowing through the power stage will be less than 8A for stereo configuration. Otherwise, the short-circuit detectors may pull the $\overline{FAULT}$ pin to GND, disabling the output stages. When the over-temperature or short-circuit condition occurs, the open-drain $\overline{FAULT}$ pin will be pulled low and latched into ERROR state. Once the short-circuit condition is removed, AD82111 will exit ERROR state when one of the following conditions is met: (1) $\overline{SD}$ pin is pulled low, (3) Master mute is enabled through the I^2C interface.

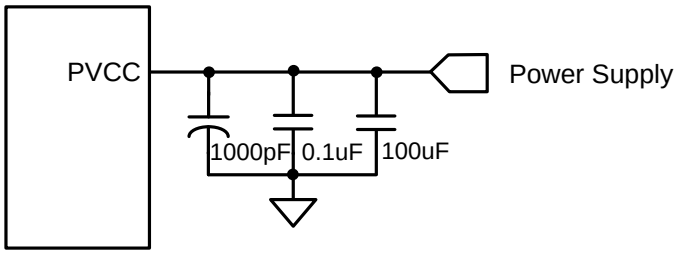
  (iii) Once the DVDD voltage is lower than 2.6V, AD82111 will turn off its loudspeaker power stages and cease the operation of digital processing circuits. When DVDD becomes larger than 2.9V, AD82111 will return to normal operation.

  (iv) If the clock inputted into BCLK pin stops during the period for 500ns or more, AD82111 detect the stop of BCLK. In this state, amplifier outputs are forced to Weak Low. While the clock is inputted normally again, $\overline{FAULT}$ pin is set to high.

Application information

- Power supply decoupling capacitor (Cs)

Because of the power loss on the trace between the device and decoupling capacitor, the decoupling capacitor should be placed close to PVCC and PGND to reduce any parasitic resistor or inductor. A low ESR ceramic capacitor, typically 1000pF, is suggested for high frequency noise rejection. For mid-frequency noise filtering, place a capacitor typically 0.1uF or 1uF as close as possible to the device PVCC leads works best. For low frequency noise filtering, a 100uF or greater capacitor (tantalum or electrolytic type) is suggested.



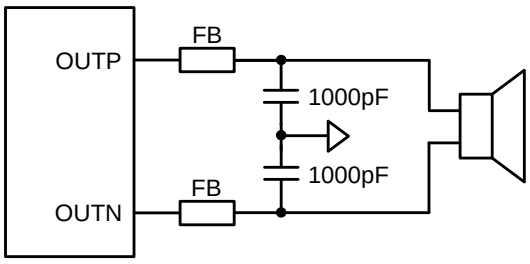
Recommended Power Supply Decoupling Capacitors.

- Boot-strap Capacitor

The output stage of the AD82111 uses a high-side NMOS driver. To generate the gate driver voltage for the high-side NMOS, a boot-strap capacitor for each output terminal acts as a floating power supply for the switching cycle. Use 0.22uF capacitors to connect the appropriate output pin to the boot-strap pin in stereo application and use 0.47uF boot-strap capacitor in mono application.

- Ferrite Bead selection

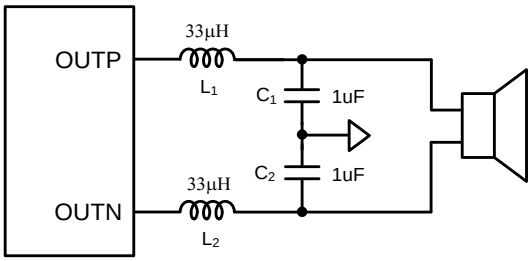
If the traces from the AD82111 to speaker are short, the ferrite bead filters can reduce the high frequency emissions to meet FCC requirements. A ferrite bead that has very low impedance at low frequency and high impedance at high frequency (above 1MHz) is recommended. The impedance of the ferrite bead can be used along with a small capacitor with a value around 1000pF to reduce the frequency spectrum of the signal to an acceptable level.



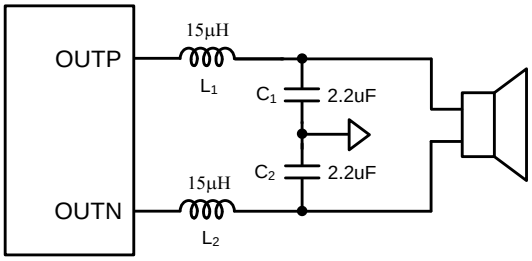
Typical output filter for Filter-less application

- Output LC Filter

If the traces from the AD82111 to speaker are not short, it is recommended to add the output LC filter to eliminate the high frequency emissions. Below figure shows the typical output filter for 8Ω & 4Ω speaker with a cut-off frequency of 27kHz.



Typical LC output filter for 8Ω speaker



Typical LC output filter for 4Ω speaker

- Inductor Selection

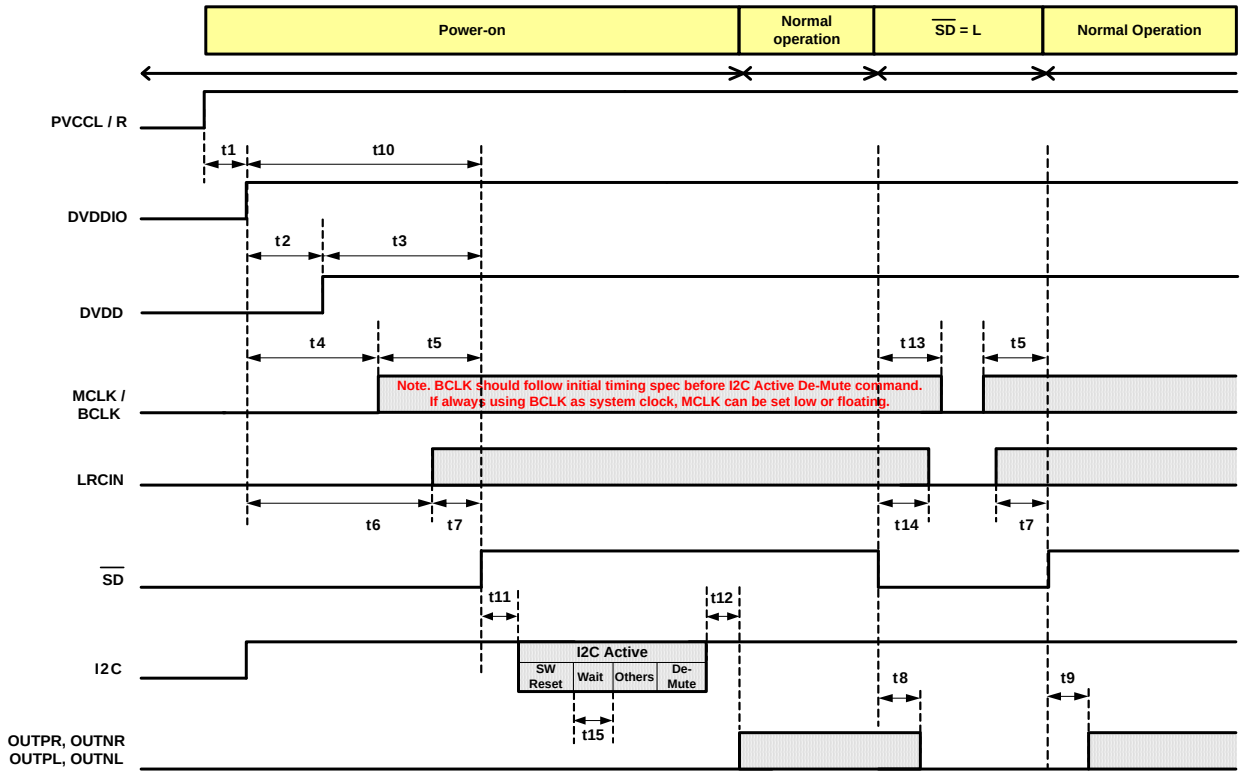
The inductance vs. current profile for the inductor used in the output LC filter of a class-D amplifier can significantly impact the total harmonic distortion (THD) performance. The inductors always have decreasing inductance with increasing operating current. The inductance falls off severely, which induce inductor distortion is higher during lower-impedance loads. The effective inductance at the peak current is required to be at least 80% of the inductance value

In addition, it is required that the peak current is smaller than the OCP trigger threshold. Same PVCC and switching frequency, larger inductance means smaller idle current for lower power dissipation. The inductor's saturation current Isat > the amplifier's operating peak current is necessary. To operating safe considering, the inductor’s saturation current >1.35 times of the peak current of maximum output power is suggested.

$$Inductor\_Ipeak\_selection \geq \sqrt{2 \times \frac{Maximum\_output\_power}{Rload}} \times 1.35$$

- Power on sequence

Hereunder is AD82111's power on sequence. Give a de-mute command via I^2C when the whole system is stable.



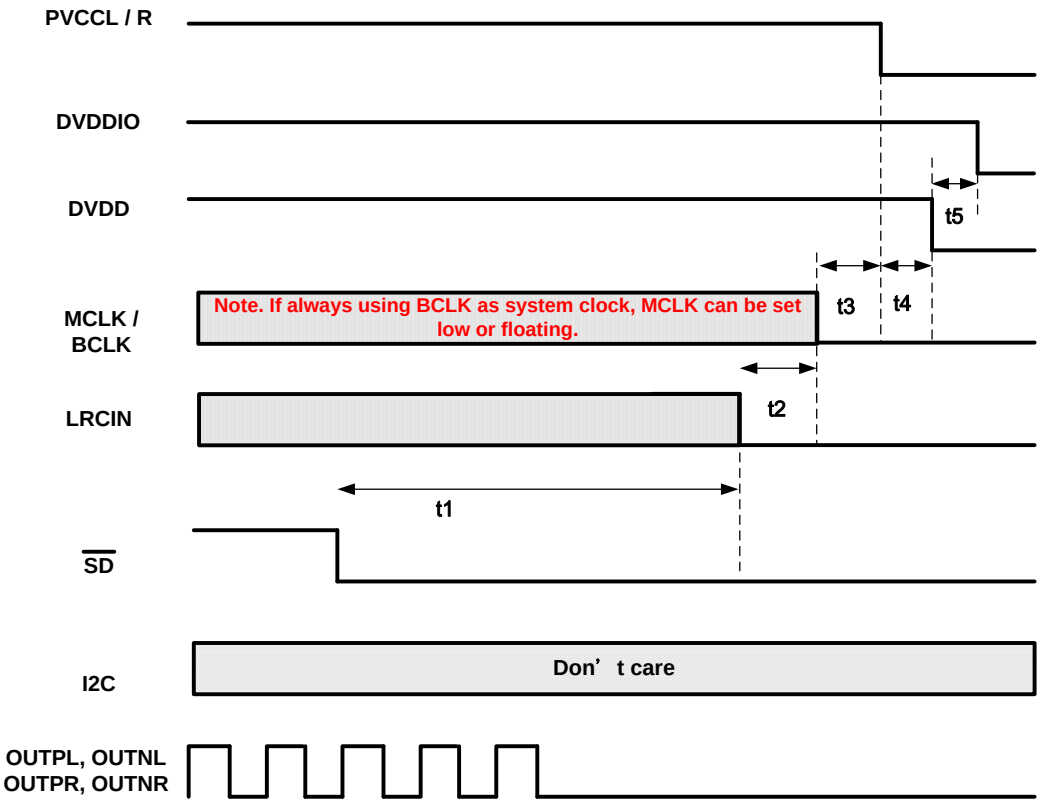
Note 7: Please be noted below sequence shall be followed up with "I2C Active" processing,
(1) Set S/W reset bit (0X02 B[4]) = 0 → (2) Delay 5ms → (3) Set S/W reset bit (0X02 B[4]) = 1 → (4) Delay 20ms → (5) Set all channels = mute (setting address 0X02 B[3] = 1) → (6) Set other registers (except setting address 0X02 B[4:3]) → (7) Set all channels = de-mute (setting address 0X02 B[3] = 0)

Symbol	Condition	Min	Max	Units
t1		0	-	msec
t2		0	-	msec
t3		10	-	msec
t4		0	-	msec
t5		10	-	msec
t6		0	-	msec
t7		10	-	msec
t8		-	22	msec
t9		-	150	msec
t10		10	-	msec
t11		150	-	msec

t12		-	0.1	msec
t13		25	-	msec
t14		25	-	msec
t15		20	-	msec

- Power off sequence

Hereunder is AD82111's power off sequence.



Symbol	Condition	Min	Max	Units
t1		35(Note 8)	-	msec
t2		0	-	msec
t3		1(Note 9)	-	msec
t4		1(Note 9)	-	msec
t5		0(Note 9)	-	msec

Note 8: t1 min 35ms refer to FADE_SPEED register=00(address: 0X16, bit3~2). If the FADE_SPEED=11, t1 should change to 280ms.

Note 9: Don't care it if the PVCC, DVDDIO, or DVDD power supports continuously during the system off.

I²C-Bus Transfer Protocol

- Introduction

  AD82111 employs I²C-bus transfer protocol. Two wires, serial data and serial clock carry information between the devices connected to the bus. Each device is recognized by a unique 7-bit address and can operate as either a transmitter or a receiver. The master device initiates a data transfer and provides the serial clock on the bus. AD82111 is always an I²C slave device.

- Protocol

  - START and STOP condition

    START is identified by a high to low transition of the SDA signal. A START condition must precede any command for data transfer. A STOP is identified by a low to high transition of the SDA signal. A STOP condition terminates communication between AD82111 and the master device on the bus. In both START and STOP, the SCL is stable in the high state.

  - Data validity

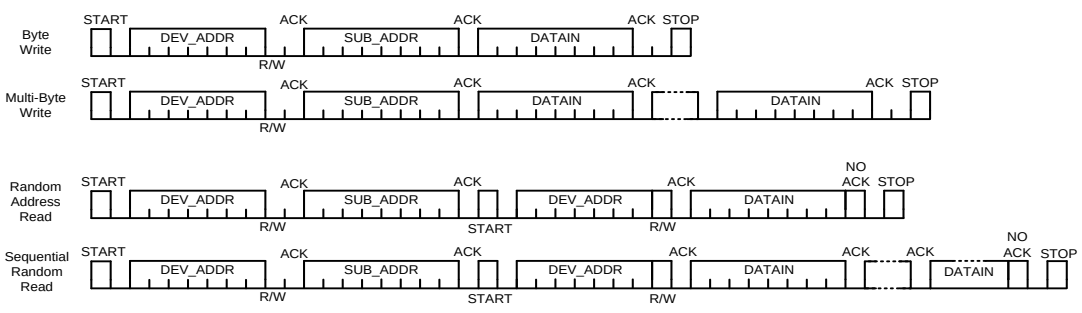
    The SDA signal must be stable during the high period of the clock. The high or low change of SDA only occurs when SCL signal is low. AD82111 samples the SDA signal at the rising edge of SCL signal.

  - Device addressing

    The master generates 7-bit address to recognize slave devices. When AD82111 receives 7-bit address matched with 0110000 (0x30) or 0110100 (0x34) depend on $\overline{\text{FAULT}}$ pin state during power up, AD82111 will acknowledge at the 9th bit (the 8th bit is for R/W bit). The bytes following the device identification address are for AD82111 internal sub-addresses.

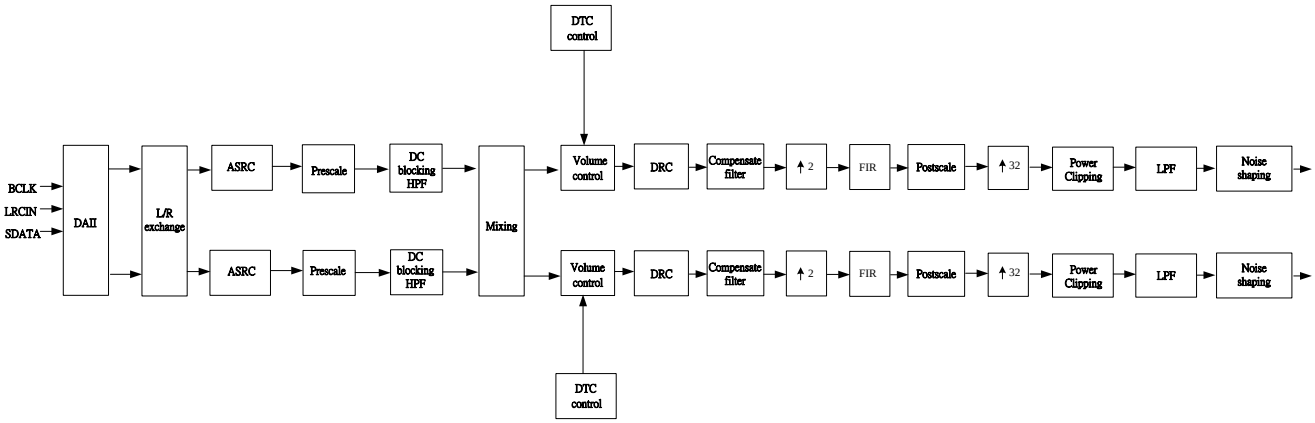
  - Data transferring

    Each byte of SDA signaling must consist of 8 consecutive bits, and the byte is followed by an acknowledge bit. Data is transferred with MSB first, as shown in the figure below. In both write and read operations, AD82111 supports both single-byte and multi-byte transfers. Refer to the figure below for detailed data-transferring protocol.



Register Table

The audio signal processing data flow is shown as the following figure. Users can control these function by programming appropriate setting to register table. In this section, the register table is summarized first. The definition of each register follows in the next section.



Address	Register	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	Default
0X00	SCTL1	IF[2]	IF[1]	IF[0]	LREXC	Reserved			NGE	0X01
0X01	SCTL 2	BCLK_SEL	Reserved		FS[0]	PMF[3]	PMF[2]	PMF[1]	PMF[0]	0x91
0X02	SCTL 3	A_SEL_FAULT	HPB	LV_UVSEL	SW_RSTB	MUTE	CM1	CM2	COMP_EN	0X10
0X03	MVOL	MV[7]	MV[6]	MV[5]	MV[4]	MV[3]	MV[2]	MV[1]	MV[0]	0XFF
0X04	C1VOL	C1V[7]	C1V[6]	C1V[5]	C1V[4]	C1V[3]	C1V[2]	C1V[1]	C1V[0]	0X18
0X05	C2VOL	C2V[7]	C2V[6]	C2V[5]	C2V[4]	C2V[3]	C2V[2]	C2V[1]	C2V[0]	0X18
0X06	HVUV	DIS_HVUV	DIS_LVUV_FADE	DIS_OV_FADE	DIS_OV	Reserved	HVUVSEL[2]	HVUVSEL[1]	HVUVSEL[0]	0XA2
0X07	SCTL 4	C1MX_EN	C2MX_EN	PC1_EN	PL1_EN	MONO_EN	PC2_EN	PL2_EN	Reserved	0X36
0X08	LAR	LA[3]	LA[2]	LA[1]	LA[0]	LR[3]	LR[2]	LR[1]	LR[0]	0X6A
0X09	Reserved	Reserved								0X00
0X0A	Reserved	Reserved								0X00
0X0B	Reserved	Reserved								0X00
0X0C	ERDLY	Prohibited								0X30
0X0D	PROT	Prohibited								0X00
0X0E	TM_CTRL	Prohibited								0X00
0X0F	PWM_CTRL	Prohibited								0X00
0X10	ATT	ATT[7]	ATT[6]	ATT[6]	ATT[4]	ATT[3]	ATT[2]	ATT[1]	ATT[0]	0X20
0X11	ATM	ATM[7]	ATM[6]	ATM[5]	ATM[4]	ATM[3]	ATM[2]	ATM[1]	ATM[0]	0X00
0X12	ATB	ATB[7]	ATB[6]	ATB[5]	ATB[4]	ATB[3]	ATB[2]	ATB[1]	ATB[0]	0X00
0X13	PCT	PCT[7]	PCT[6]	PCT[5]	PCT[4]	PCT[3]	PCT[2]	PCT[1]	PCT[0]	0x7F
0X14	PCM	PCM[7]	PCM[6]	PCM[5]	PCM[4]	PCM[3]	PCM[2]	PCM[1]	PCM[0]	0XFF

0X15	PCB	PCB[7]	PCB[6]	PCB[5]	PCB [4]	PCB [3]	PCB [2]	PCB [1]	PCB [0]	0XFF
0X16	SCTL5	NG_CNT_SEL[1]	NG_CNT_SEL[0]	Reserved	DIS_ZD_FADE	FADE_SPEED[1]	FADE_SPEED[0]	NG_GAIN[1]	NG_GAIN[0]	0X00
0X17	VFT	MV_FT[1]	MV_FT[0]	C1V_FT[1]	C1V_FT[0]	C2V_FT[1]	C2V_FT[0]	Reserved		0X00
0X18	DTC	DTC_EN	DTC_TH[1]	DTC_TH[0]	DTC_RATE[1]	DTC_RATE[0]	Reserved			0X40
0X19	Reserved	Reserved								0X00
0X1A	NGAL1	NGAL1[7]	NGAL1[6]	NGAL1[5]	NGAL1[4]	NGAL1[3]	NGAL1[2]	NGAL1[1]	NGAL1[0]	0X00
0X1B	NGAL2	NGAL2[7]	NGAL2[6]	NGAL2[5]	NGAL2[4]	NGAL2[3]	NGAL2[2]	NGAL2[1]	NGAL2[0]	0X00
0X1C	NGAL3	NGAL3[7]	NGAL3 [6]	NGAL3 [5]	NGAL3 [4]	NGAL3 [3]	NGAL3 [2]	NGAL3 [1]	NGAL3 [0]	0X1A
0X1D	NGAL4	NGAL4[7]	NGAL4 [6]	NGAL4 [5]	NGAL4 [4]	NGAL4 [3]	NGAL4 [2]	NGAL4 [1]	NGAL4 [0]	0X00
0X1E	NGRL1	NGRL1[7]	NGRL1[6]	NGRL1[5]	NGRL1[4]	NGRL1[3]	NGRL1[2]	NGRL1[1]	NGRL1[0]	0X00
0X1F	NGRL2	NGRL2[7]	NGRL2[6]	NGRL2[5]	NGRL2[4]	NGRL2[3]	NGRL2[2]	NGRL2[1]	NGRL2[0]	0X00
0X20	NGRL3	NGRL3[7]	NGRL3 [6]	NGRL3[5]	NGRL3[4]	NGRL3 [3]	NGRL3 [2]	NGRL3 [1]	NGRL3 [0]	0X53
0X21	NGRL4	NGRL4[7]	NGRL4[6]	NGRL4[5]	NGRL4[4]	NGRL4[3]	NGRL4[2]	NGRL4[1]	NGRL4[0]	0X00
0X22	RTT	RTT[7]	RTT[6]	RTT[5]	RTT[4]	RTT[3]	RTT[2]	RTT[1]	RTT[0]	0X08
0X23	RTM	RTM[7]	RTM[6]	RTM[5]	RTM[4]	RTM[3]	RTM[2]	RTM[1]	RTM[0]	0X00
0X24	RTB	RTB[7]	RTB[6]	RTB[5]	RTB[4]	RTB[3]	RT [2]	RTB[1]	RTB [0]	0X00
0X25	DEVICE ID	Device code				Version code				0X12
0X26	DRC_ECT	DRC_ECT[7]	DRC_ECT[6]	DRC_ECT[5]	DRC_ECT[4]	DRC_ECT[3]	DRC_ECT[2]	DRC_ECT[1]	DRC_ECT[0]	0X00
0X27	DRC_ECB	DRC_ECB[7]	DRC_ECB[6]	DRC_ECB[5]	DRC_ECB[4]	DRC_ECB[3]	DRC_ECB[2]	DRC_ECB[1]	DRC_ECB[0]	0X10
0X28	HI-RES	Reserved				FIR2_EN	ANTI_LC_EN	ANTI_ALIAS_EN	Reserved	0X0E
0X29	MK_H	MK_HBYTE[7]	MK_HBYTE[6]	MK_HBYTE[5]	MK_HBYTE[4]	MK_HBYTE[3]	MK_HBYTE[2]	MK_HBYTE[1]	MK_HBYTE[0]	0X00
0X2A	MK_L	MK_LBYTE[7]	MK_LBYTE[6]	MK_LBYTE[5]	MK_LBYTE[4]	MK_LBYTE[3]	MK_LBYTE[2]	MK_LBYTE[1]	MK_LBYTE[0]	0X00
0X2B	PRST	PRST[7]	PRST[6]	PRST[5]	PRST[4]	PRST[3]	PRST[2]	PRST[1]	PRST[0]	0X1F
0X2C	PRSM	PRSM[7]	PRSM[6]	PRSM[5]	PRSM[4]	PRSM[3]	PRSM[2]	PRSM[1]	PRSM[0]	0XA2
0X2D	PRSB	PRSB[7]	PRSB[6]	PRSB[5]	PRSB[4]	PRSB[3]	PRSB[2]	PRSB[1]	PRSB[0]	0X3A
0X2E	POST	POST[7]	POST[6]	POST[5]	POST[4]	POST[3]	POST[2]	POST[1]	POST[0]	0X20
0X2F	POSM	POSM[7]	POSM[6]	POSM[5]	POSM[4]	POSM[3]	POSM[2]	POSM[1]	POSM[0]	0X00
0x30	POSB	POSB[7]	POSB[6]	POSB[5]	POSB[4]	POSB[3]	POSB[2]	POSB[1]	POSB[0]	0X00
0x31	I2SOSEL	Reserved	Reserved	Reserved	Reserved	SDATAO_CTRL	I2S_DO_SEL[2]	I2S_DO_SEL[1]	I2S_DO_SEL[0]	0X05
0x32	I2SGT	I2SGT[7]	I2SGT[6]	I2SGT[5]	I2SGT[4]	I2SGT[3]	I2SGT[2]	I2SGT[1]	I2SGT[0]	0X80
0x33	I2SGM	I2SGM[7]	I2SGM[6]	I2SGM[5]	I2SGM[4]	I2SGM[3]	I2SGM[2]	I2SGM[1]	I2SGM[0]	0X00
0x34	I2SGB	I2SGB[7]	I2SGB[6]	I2SGB[5]	I2SGB[4]	I2SGB[3]	I2SGB[2]	I2SGB[1]	I2SGB[0]	0X00
0x35 ~0x39	Reserved	Reserved								0X00
0X3A	ANAG	Prohibited								0X00
0x3B	ERR_REG	A_OCP_N	A_OTP_N	A_UV_N	A_DCD_N	A_CKERR	A_OVP	Reserved		read only

0x3C	ERR_RECORD	A_OCP_N_LATCH	A_OTP_N_LATCH	A_UV_N_LATCH	A_DCD_N_LATCH	A_CKERR_LATCH	A_OVP_LATCH	Reserved	read only
0x3D	ERR_CLEAR	A_OCP_N_CLEAR	A_OTP_N_CLEAR	A_UV_N_CLEAR	A_DCD_N_CLEAR	A_CKERR_CLEAR	A_OVP_CLEAR	Reserved	0x00
0x3E	RAM1_ CFADDR	Prohibited							0x00
0x3F	RAM1_ A1CF1	Prohibited							0x00
0x40	RAM1_ A1CF2	Prohibited							0x00
0x41	RAM1_ A1CF3	Prohibited							0x00
0x42	RAM1_ A1CF4	Prohibited							0x00
0x43	RAM1_ A1CF5	Prohibited							0x00
0x44	RAM1_ CFRW	Prohibited							0x00
0x45	MBIST	Prohibited							0X00
0x46	Reserved	Reserved							0X00
0x47	MBIST_UP1_E	Prohibited							0X01
0x48	MBIST_UP2_E	Prohibited							0X55
0x49	MBIST_UP3_E	Prohibited							0X55
0x4A	MBIST_UP4_E	Prohibited							0X55
0x4B	MBIST_UP5_E	Prohibited							0X55
0x4C	MBIST_UP1_O	Prohibited							0X01
0x4D	MBIST_UP2_O	Prohibited							0X55
0x4E	MBIST_UP3_O	Prohibited							0X55
0x4F	MBIST_UP4_O	Prohibited							0X55
0x50	MBIST_UP5_O	Prohibited							0X55
0x51	TMR0	Prohibited							0X0E
0x52	DITHER	Prohibited							0X18
0x53	PMF read	Prohibited							read only
0x54 ~0x5C	Reserved	Reserved							0X00
0x5D	TDM_W	Reserved						TDM_W[1]	TDM_W[0]	0X00
0x5E	TDM_O	TDM_O[7]	TDM_O[6]	TDM_O[5]	TDM_O[4]	TDM_O[3]	TDM_O[2]	TDM_O[1]	TDM_O[0]	0X00
0x5F	ANA_GAIN	Reserved					ANA_GAIN[2]	ANA_GAIN[1]	ANA_GAIN[0]	0X00
0x60	FSW	Prohibited							FSW[0]	0X00
0x6F	TMR1	Prohibited	Filterless_SEL	Prohibited						0x71
0x70	OCPCTL	Prohibited								0x40

Detail Description for Register

In this section, please note that the highlighted columns are the default value of these tables. If no highlighted, it is because the default setting of this bit is determined by external pin.

- Address 0X00 : State control 1

  AD82111 support multiple serial data input formats including I^2S, Left-alignment and Right-alignment.

  These formats is chosen by user via bit7~bit5 of address 0.

  AD82111 can change L channel and R channel output via bit4

  AD82111 support noise gate function via bit0.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:5]	IF[2:0]	Input Format	000	I^2S 16-32 bits
			001	Left-alignment 16-32 bits
			010	Right-alignment 16 bits
			011	Right-alignment 18 bits
			100	Right-alignment 20 bits
			101	Right-alignment 24 bits
			110	Right-alignment 32 bits
			111	TDM
B[4]	LREXC	Left/Right (L/R) Channel Exchanged	0	No exchanged
			1	L/R exchanged
B[3:1]	X	Reserved		
B[0]	NGEN	Noise Gate Enable	0	Disable
			1	Enable

- Address 0X01 : State control 2

AD82111 has built-in PLL, and multiple MCLK/FS or BCLK/FS ratio is supported. If BCLK_SEL is high, the ratio is changed to BCLK/FS ratios. On the contrary, the ratio is changed to MCLK/FS ratios. Detail setting is shown as the above table..

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	BCLK_SEL	BCLK System enable	0	Disable
			1	Enable
B[6:5]	X	Reserved		
B[4]	FS	Sampling Frequency	0	32/44.1/48kHz
			1	64/88.2/96kHz

Multiple MCLK/FS in MCLK system or BCLK/FS in BCLK system ratio setting table

BIT	NAME	DESCRIPTION	VALUE	B[4]=0	B[4]=1
B[3:0]	PMF[3:0]	MCLK/FS or BCLK/FS setup when PLL is not bypassed	0000	1024x	512x
			0001	Reset Default (64x)	Reset Default (64x)
			0010	128x	128x
			0011	192x	192x
			0100	256x	256x
			0101	384x	384x
			0110	512x	512x
			0111	576x	Reserved
			1000	768x	
			1001	1024x	

- Address 0X02 : State control 3

The $\overline{\text{FAULT}}$ of AD82111 is a dual function pin. It is treated as an I^2C device address selection input when bit 7 is set as low. It will become as a FAULT output pin when bit 7 is set as high. To prevent the DC current from damaging the speaker, a high pass filter (3dB frequency=1Hz) is built into the AD82111. It can be enabled or disabled by bit 6 of address 0X02.

To prevent the input signal source with DC value which may damage the speaker, a high pass filter (3dB frequency=1Hz) is built in the AD82111. It can be disabled by bit 6 of address 0X02.

AD82111 has a mute function which includes master mute and individual channel mute modes. When the master mute mode is enabled, both left and right processing channels are muted. On the other hand, either channel can be muted by using the channel mute mode. When the mute function is enabled or disabled, the fade-out or fade-in process will be initiated.

AD82111 frequency response will become higher at high frequency area with PVCC lower 12V.Turning on the compensate filter will can adjust the frequency response more flat at high frequency area while PVCC lower 12V.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	A_SEL_FAULT	I^2C address selection or FAULT output	0	I^2C device address selection
			1	ERROR output
B[6]	HPB	DC Blocking HPF Bypass	0	Enable
			1	Disabled
B[5]	LV_UVSEL	LV Under Voltage Selection	0	2.6V
			1	2.2V
B[4]	SW_RSTB	Software reset	0	Reset
			1	Normal operating
B[3]	MUTE	Master Mute	0	Un-Mute
			1	Mute
B[2]	CM1	Channel 1 Mute	0	Un-Mute
			1	Mute
B[1]	CM2	Channel 2 Mute	0	Un-Mute
			1	Mute
B[0]	COMP_EN	Frequency Compensate filter	0	Disable
			1	Enable

- Address 0X03 : Master volume

AD82111 supports both master-volume and channel-volume control for the stereo processing channels. Both master volume control (Address 0X03) and channel volume (Address 0X04 and 0X05) settings range from +12dB ~ -102dB. Given master volume level, say, Level A (in dB unit) and channel volume level, say Level B (in dB unit), the total volume equals to Level A plus with Level B and its range is from +24dB ~ -102dB, i.e., -103dB ≦ Total Volume (Level A + Level B) ≦ +24dB.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	MV[7:0]	Master Volume	00000000	+12dB
			00000001	+11.5dB
			00000010	+11dB
			:	:
			00010111	0.5dB
			00011000	0dB
			00011001	-0.5dB
			:	:
			11100110	-103dB
			11100101	-∞dB
			:	:
			11111111	-∞dB

- Address 0X04 : Channel1 volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C1V[7:0]	Channel 1 Volume	00000000	+12dB
			00000001	+11.5dB
			:	:
			00010100	2dB
			:	:
			00011000	0dB
			00011001	-0.5dB
			:	:
			11100110	-103dB
			11100101	-∞dB
			:	:
			1111111	-∞dB

- Address 0X05 : Channel2 volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C2V[7:0]	Channel 2 Volume	00000000	+12dB
			00000001	+11.5dB
			:	:
			00010100	2dB
			:	:
			00011000	0dB
			00011001	-0.5dB
			:	:
			11100110	-103dB
			11100101	-∞dB
			:	:
			1111111	-∞dB

- Address 0X06 : Under voltage selection for high voltage supply

AD82111 provides HV under voltage detection which can be enable or disable via bit 7. The under-voltage detection level is programmable via bit2~ bit0. Once the output stage voltage drops below the default value (see table), AD82111 will fade out audio signals to turn off the speaker.

If user want to have an application with PVCC is lower than 10V, user can set HV under voltage disable or set lower under voltage level. AD82111 also provides OV fade function and user can select fade or not fade for OV via bit5.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	Dis_HVUV	Disable HV Under Voltage Circuit	0	Enable
			1	Disable
B[6]	DIS_LVUV_FADE	Disable LV under voltage fade	0	Fade
			1	No fade
B[5]	DIS_OV_FADE	Disable over voltage fade	0	Fade
			1	No fade
B[4]	DIS_OV	Disable HV over voltage circuit	0	Enable
			1	Disable
B[3]	X	Reserved		
B[2:0]	HVUVSEL[2:0]	HV Under Voltage Selection (Active)	000	4V
			001	8.2V
			010	9.7V
			011	13.2V
			100	15.5V
			101	19.5V
			Others	4V

- Address 0X07 : State control 4

AD82111 provides channel mix, power clipping, and dynamic range control (DRC) function. These functions can be enable or not as the following table.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	C1MX_EN	Channel1 Mixing Enable	0	Disable
			1	Enable
B[6]	C2MX_EN	Channel2 Mixing Enable	0	Disable
			1	Enable
B[5]	PC1_EN	CH1 Power Clipping enable	0	Disable
			1	Enable
B[4]	PL1_EN	CH1 DRC enable	0	Disable
			1	Enable
B[3]	MONO_EN	MONO or Stereo configure	0	Stereo
			1	MONO
B[2]	PC2_EN	CH2 Power Clipping enable	0	Disable
			1	Enable
B[1]	PL2_EN	CH2 DRC enable	0	Disable
			1	Enable
B[0]	X	Reserved		

AD82111 also provides MONO register via bit 3 of address 0X07. Besides this MONO register, address 0X29 and 0X2A should be setting to enter MONO configuration. The output configuration shall be right connected before Mono configuration enable. That's possible to damage chips due to channel shoot-through if the wrong output configuration is connected.

- Address 0X08 : Attack rate and Release rate for Dynamic Range Control (DRC)

The attack/release rates of AD82111 are defined as following table,

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:5]	LA[3:0]	DRC Attack Rate	0000	3 dB/ms
			0001	2.667 dB/ms
			0010	2.182 dB/ms
			0011	1.846 dB/ms
			0100	1.333 dB/ms
			0101	0.889 dB/ms
			0110	0.4528 dB/ms
			0111	0.2264 dB/ms
			1000	0.15 dB/ms
			1001	0.1121 dB/ms
			1010	0.0902 dB/ms
			1011	0.0752 dB/ms
			1100	0.0645 dB/ms
			1101	0.0563 dB/ms
			1110	0.0501 dB/ms
			1111	0.0451 dB/ms
B[3:0]	LR[3:0]	DRC Release Rate	0000	0.5106 dB/ms
			0001	0.1371 dB/ms
			0010	0.0743 dB/ms
			0011	0.0499 dB/ms
			0100	0.0360 dB/ms
			0101	0.0299 dB/ms
			0110	0.0264 dB/ms
			0111	0.0208 dB/ms
			1000	0.0198 dB/ms
			1001	0.0172 dB/ms
			1010	0.0147 dB/ms
			1011	0.0137 dB/ms
			1100	0.0134 dB/ms
			1101	0.0117 dB/ms
			1110	0.0112 dB/ms
			1111	0.0104 dB/ms

- Address 0X10 : Top 5 bits of attack threshold for Dynamic Range Control (DRC)

The AD82111 provides dynamic range control function. When the input RMS exceeds the programmable attack threshold value, the output power will be limited by this threshold power level via gradual gain reduction. Attack threshold is defined by 24-bit representation composed of registers controlled by I^2C. The device addresses of DRC attack threshold are 0X10, 0X11, and 0X12.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	ATT[7:0]	Top 8 Bits of Attack Threshold	X	User programmed
			00100000	0dB

- Address 0X11 : Middle 8 bits of attack threshold

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	ATM[7:0]	Middle 8 Bits of Attack Threshold	X	User programmed
			00000000	0dB

- Address 0X12 : Bottom 8 bits of attack threshold

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	ATB[7:0]	Bottom 8 bits of attack threshold	X	User programmed
			00000000	0dB

- Address 0X13 : Top 8 bits of power clipping

The AD82111 provides power clipping function to avoid excessive signal that may destroy loud speaker. The power clipping level is defined by 24-bit representation composed of registers controlled by I^2C. The device addresses of power clipping threshold are 0X13, 0X14, and 0X15.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	PCT[7:0]	Top 8 Bits of Power Clipping Level	X	User programmed
			01111111	0dB

- Address 0X14 : Middle 8 bits of power clipping

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	PCM[7:0]	Middle 8 Bits of Power Clipping Level	X	User programmed
			11111111	0dB

- Address 0X15 : Bottom 8 bits of power clipping level

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	PCB[7:0]	Bottom 8 Bits of Power Clipping Level	X	User programmed
			11111111	0dB

The following table shows the power clipping level's numerical representation.

Sample calculation for power clipping

Max amplitude	dB	Linear	Decimal	Hex (1.23 format)
Gain	0	1	8388608	800000
Gain*0.707	-3	0.707	5930720	5A7EE0
Gain*0.5	-6	0.5	4194304	400000
Gain*L	x	$L=10^{(x/20)}$	D=8388608xL	H=dec2hex(D)

Note: Gain is the closed loop gain of AD82111, and the value is 30(±5%) with 8ohm load. If the max amplitude is larger than PVCC, max amplitude changes to PVCC.

- Address 0X16 : State control 5

When receiving signal sample points less than noise gate attack level for the time more than noise gate count time, noise gate function will active. The noise gate count time can be programmed via bit [7:6].User can change noise gate gain via bit1~ bit0. When noise gate function occurs, input signal will multiply noise gate gain (x1/8, x1/4 x1/2, x0). User can select fade out or not via bit 4.

AD82111 provide 4 kinds of fade speed (1.25ms, 2.5ms, 5ms, 10ms), user can select most suitable fade speed for their system.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]	NG_CNT_SEL	Noise gate count time selection	00	43ms @fs:48K
			01	86ms @fs:48K
			10	172ms @fs:48K
			11	344ms @fs:48K
B[4]	DIS_NG_FADE	Disable Noise Gate Fade	0	Fade
			1	No fade
B[3:2]	FADE_SPEED	Fade in/out speed selection	00	1.25ms
			01	2.5ms
			10	5ms
			11	10ms
B[1:0]	NG_GAIN	Noise Gate Detection Gain	00	x1/8
			01	x1/4
			10	x1/2
			11	Mute

- Address 0X17 : Volume fine tune

AD82111 supports both master-volume fine tune and channel-volume control fine tune modes. Both volume control settings range from 0dB ~ -0.375dB and 0.125dB per step. Note that the master volume fine tune is added to the individual channel volume fine tune as the total volume fine tune.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]	MV_FT	Master Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[5:4]	C1V_FT	Channel 1 Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[3:2]	C2V_FT	Channel 2 Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[1:0]	X	Reserved		

- Address 0X18 : Dynamic Temperature Control (DTC)

AD82111 supports dynamic temperature control. The table describes the setting of DTC.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	DTC_EN	DTC Enable	0	Disable
			1	Enable
B[6:5]	DTC_TH	DTC Attack Threshold	00	110 °C
			01	120 °C
			10	130 °C
			11	140 °C
B[4:3]	DTC_RATE	DTC Attack and Release Rate	00	1dB/sec
			01	0.5dB/sec
			10	0.33dB/sec
			11	0.25dB/sec
B[2:0]	X	Reserved		

DTC release threshold is designed 10 °C lower than attack threshold.

For example:

DTC attack threshold =130 °C, the release threshold is 120 °C.

DTC attack threshold =120 °C, the release threshold is 110 °C.

If junction temperature (Tj) exceeds 130 °C, amplifier gain will be lowered to timing of 1dB/sec. If amplifier gain falls and junction temperature (Tj) turns into less than 130 °C and larger than 120 °C, the gain will not increase or decrease. If amplifier gain falls and junction temperature (Tj) turns into less than 120 °C, amplifier gain will be raised to timing of 1dB/sec.

- Address 0X1A : The first byte of noise gate attack level

When both left and right signals have 2048 consecutive sample points less than the programmable noise gate attack level, the audio signal will multiply noise gate gain, which can be set at x1/8, x1/4, x1/2, or zero if the noise gate function is enabled. Noise gate attack level is defined by 32-bit representation composed of registers controlled by I^2C. The addresses of noise gate attack level are 0X1A, 0X1B, 0X1C and 0X1D.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	NGAL1[7:0]	The first 8 Bits of Noise Gate Attack Level	X	User programmed
			00000000	-110dB

- Address 0X1B : The second byte of noise gate attack level

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	NGAL2[7:0]	The second 8 Bits of Noise Gate Attack Level	X	User programmed
			00000000	-110dB

- Address 0X1C : The third byte of noise gate attack level

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	NGAL3[7:0]	Bottom 8 Bits of Noise Gate Attack Level	X	User programmed
			00011010	-110dB

- Address 0X1D : The fourth byte of noise gate attack level

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	NGAL4[7:0]	Bottom 8 Bits of Noise Gate Attack Level	X	User programmed
			00000000	-110dB

- Address 0X1E : The first byte of noise gate release level

  After entering the noise gating status, the noise gain will be removed whenever AD82111 receives any input signal that is more than the noise gate release level. Noise gate release level is defined by 32-bit representation composed of registers controlled by I^2C. The device addresses of noise gate release level are 0X1E, 0X1F, 0X20 and 0X21.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	NGRL1[7:0]	The first 8 Bits of Noise Gate Release Level	X	User programmed
			00000000	-100dB

- Address 0X1F : The second byte of noise gate release level

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	NGRL2[7:0]	The second 8 Bits of Noise Gate Release Level	X	User programmed
			00000000	-100dB

- Address 0X20 : The third byte of noise gate release level

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	NGRL3[7:0]	The third 8 Bits of Noise Gate Release Level	X	User programmed
			01010011	-100dB

- Address 0X21 : The fourth byte of noise gate release level

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	NGRL4[7:0]	The fourth 8 Bits of Noise Gate Release Level	X	User programmed
			00000000	-100dB

The following table shows the noise gate attack and release threshold level's numerical representation.

Sample calculation for noise gate attack and release level

Input amplitude (dB)	Linear	Decimal	Hex (1.31 format)
0	1	2147483647	7FFFFFFF
-100	10^{-5}	21475	5300
-110	$10^{-5.5}$	6791	1A00
X	$L=10^{(x/20)}$	D=2147483647xL	H=dec2hex(D)

- Address 0X22 : Top 8 bits of release threshold for Dynamic Range Control (DRC)

  After AD82111 has reached the attack threshold, its output power will be limited to that level. The output power level will be gradually adjusted to the programmable release threshold level. Release threshold is defined by 21-bit representation composed of registers controlled by I^2C. The device addresses of release threshold are 0X22, 0X23, and 0X24.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	RTT[7:0]	Top 8 Bits of Release Threshold	X	User programmed
			00001000	-6dB

- Address 0X23 : Middle 8 bits of release threshold

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	RTM[7:0]	Middle 8 Bits of Release Threshold	X	User programmed
			00000000	-6dB

- Address 0X24 : Bottom 8 bits of release threshold

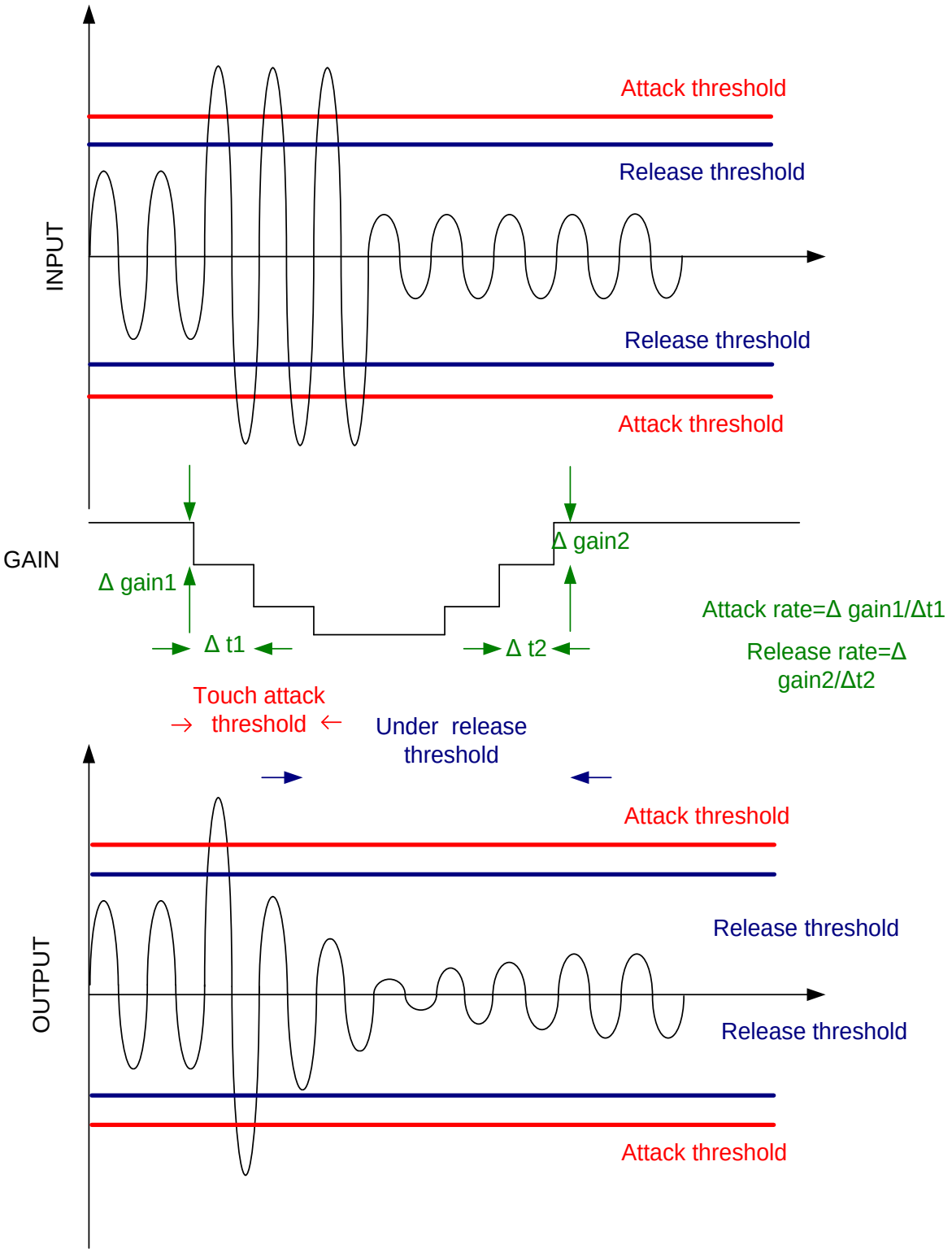
BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	RTB[7:0]	Bottom 8 Bits of Release Threshold	X	User programmed
			00000000	-6dB

The following table shows the attack and release threshold's numerical representation.

Sample calculation for attack and release threshold

Power	dB	Linear	Decimal	Hex (3.21 format)
(Gain^2)/R	0	1	2097152	200000
(Gain^2)/2R	-3	0.5	1048576	100000
(Gain^2)/4R	-6	0.25	524288	80000
((Gain^2)/R)*L	x	$L=10^{(x/10)}$	D=2097152xL	H=dec2hex(D)

To best illustrate the dynamic range control function, please refer to the following figure.

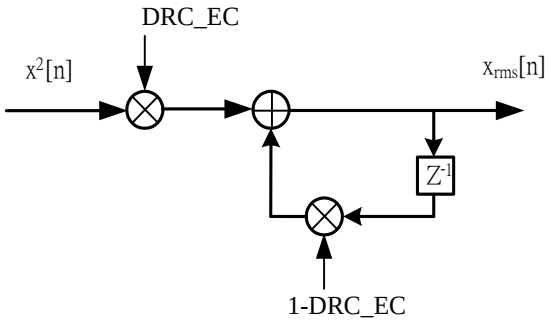


- Address 0X26 : Top 8 bits of DRC energy coefficient

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	DRC_ECT [7:0]	Top 8 Bits of DRC Energy Coefficient	X	User programmed
			00000000	1/2048

- Address 0X27 : Bottom 8 bits of DRC energy coefficient

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	DRC_ECB [7:0]	Bottom 8 Bits of DRC Energy Coefficient	X	User programmed
			00010000	1/2048



The above figure illustrates the digital processing of calculating RMS signal power. In this processing, a DRC energy coefficient is required, which can be programmed for different frequency range. Energy coefficient is defined by 16-bit representation composed of registers controlled by I^2C. The device addresses of DRC energy coefficient are 0X26, and 0X27. The following table shows the DRC energy coefficient numerical representation.

Sample calculation for DRC energy coefficient

DRC energy coefficient	dB	Linear	Decimal	Hex {1,b0, DRC_ECT[6:0], DRC_ECB,8'b0} (1.23 format)
1	0	1	8388352	7FFF00
1/256	-48.2	1/256	32768	8000
1/2048	-66.2	1/2048	4096	1000
L	x	$L=10^{(x/20)}$	D=8388352xL	H=dec2hex(D)

- Address 0X28 : Wide Band Setting Register

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]	X	Reversed		
B[3]	FIR2_EN	FIR2 filter	0	Disabled
			1	Enable
B[2]	ANTI_LC_EN	ANTI LC filter	0	Disabled
			1	Enable
B[1]	ANTI_ALIAS_EN	ANTI ALAIAS filter	0	Disabled
			1	Enable
B[0]	X	Reversed		

Fs=96KHz input, please set address 0X28=”0X0A” to extend frequency response from 20kHz to 40KHz if Wide Band Setting spec. is request. We called this “Wide Band Setting enable”.

- Address 0X29 : Mono Key High Byte

AD82111 provide a protection method to enter mono mode. Besides setting MONO_EN register high, it needs to set the value of address 0X29 to 0X30 and the value of address 0X2A to 0X06 for mono application. Otherwise, AD82111 will be stereo mode.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	MK_HBYTE[7:0]	Mono key high byte	0000_0000	Stereo
			Others	Stereo
			0011_0000	MONO

- Address 0X2A : Mono Key Low Byte

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	MK_LBYTE[7:0]	Mono key high byte	0000_0000	Stereo
			Others	Stereo
			0000_0110	MONO

- Address 0X2B: Top 8 bits of pre-scale coefficient

  For both audio channels, AD82111 can scale input signal level prior to DC blocking processing which is realized by a 24-bit signed fractional multiplier. The range of pre-scale factor is from -4 (0x800000) to 3.9999995(0x7FFFFF). The device addresses of pre-scale are 0X2B, 0X2C, and 0X2D.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	PRST[7:0]	Top 8 Bits of Pre-scale Coefficient	X	User programmed
			00011111	-0.1dB

- Address 0X2C : Middle 8 bits of pre-scale coefficient

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	PRSM[7:0]	Middle 8 Bits of Pre-scale Coefficient	X	User programmed
			10100010	-0.1dB

- Address 0X2D : Bottom 8 bits of pre-scale coefficient

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	PRSB[7:0]	Bottom 8 Bits of Pre-scale Coefficient	X	User programmed
			00111010	-0.1dB

- Address 0X2E: Top 8 bits of post-scale coefficient

For both audio channels, AD82111 provides an additional multiplication after compensate filter, which is realized by a 24-bit signed fractional multiplier. The range of post-scale factor is from -4 (0x800000) to 3.9999995(0x7FFFFF). The device addresses of pre-scale are 0X2E, 0X2F, and 0X30.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	POST[7:0]	Top 8 Bits of Post-scale Coefficient	X	User programmed
			00100000	0dB

- Address 0X2F : Middle 8 bits of post-scale coefficient

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	POSM[7:0]	Middle 8 Bits of Post-scale Coefficient	X	User programmed
			00000000	0dB

- Address 0X30 : Bottom 8 bits of post-scale coefficient

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	POSB[7:0]	Bottom 8 Bits of Post-scale Coefficient	X	User programmed
			00000000	0dB

The following table shows the pre/post scale's numerical representation.

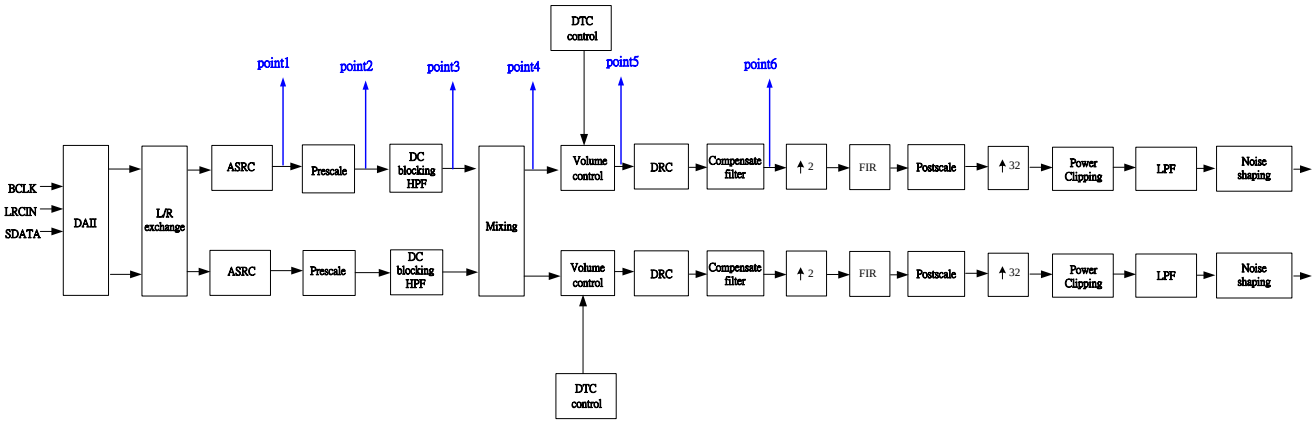
Sample calculation for pre-scale and post-scale

Pre/post scale	dB	Linear	Decimal	Hex (3.21 format)
1	0	1	2097152	200000
0.5	-6	0.5	1048576	100000
0.25	-12	0.25	524288	80000
$L=10^{(x/20)}$	x	$L=10^{(x/20)}$	D=2097152xL	H=dec2hex(D)

- Address 0X31 : I^2S output selection

AD82111 provides I^2S output function and the output point can be selected via bit 2~bit 0.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]		Reserved		
B[3]	SDATAO_CTRL	SDATAO pin control	0	GND
			1	SDATAO
B[2:0]	I2S_DO_SEL	I^2S DATA OUTPUT selection	000	DSP input (Point1)
			001	Pre-scale output (Point2)
			010	DC blocking (Point3)
			011	Mixer output (Point4)
			100	Volume output (Point5)
			101	Compensate output (Point6)
			110	Reserved
			111	



- Address 0X32: Top 8 bits of I^2S out gain coefficient

AD82111 can scale signal level before transmit the I^2S output. The range of I^2S out gain factor is from -16 (0x800000) to 15.999998(0x7FFFFF). The device addresses of I^2S out gain are 0X32, 0X33, and 0X34.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	I2SGT[7:0]	Top 8 Bits of I^2S Out Gain Coefficient	X	User programmed
			00001000	0dB

- Address 0X33 : Middle 8 bits of I^2S out gain coefficient

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	I2SGM[7:0]	Middle 8 Bits of I^2S Out Gain Coefficient	X	User programmed
			00000000	0dB

- Address 0X34 : Bottom 8 bits of I^2S out gain coefficient

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	I2SGB[7:0]	Bottom 8 Bits of I^2S Out Gain Coefficient	X	User programmed
			00000000	0dB

The following table shows the I^2S out gain numerical representation.

Sample calculation for I^2S out gain

Pre/post scale	dB	Linear	Decimal	Hex (5.19 format)
1	0	1	524288	80000
0.5	-6	0.5	262144	40000
0.25	-12	0.25	131072	20000
$L=10^{(x/20)}$	x	$L=10^{(x/20)}$	D=2097152xL	H=dec2hex(D)

- Address 0X3B, Protection Status Register

The protection registers will show what kind of protection occurs.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	A_OCP_N	Over current occur	1	Normal
			0	Occurred
B[6]	A_OTP_N	Over temperature occur	1	Normal
			0	Occurred
B[5]	A_UV_N	Under voltage occur	1	Normal
			0	Occurred
B[4]	A_DCD_N	DC detection error	1	Normal
			0	Occurred
B[3]	A_CKERR	Clock detection error	1	Normal
			0	Occurred
B[2]	A_OVP	Over voltage occur	1	Normal
			0	Occurred
B[1:0]	X	Reversed		

- Address 0X3C : Protection latch register

The protection registers will show what kind of protection ever occurred.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	A_OCP_N_LATCH	OCP latch register	0	OC ever occur
			1	Normal
B[6]	A_OTP_N_LATCH	OTP latch register	0	OT ever occur
			1	Normal
B[5]	A_UV_N_LATCH	UV latch register	0	UV ever occur
			1	Normal
B[4]	A_DCD_LATCH	DCD latch register	0	DCD ever occur
			1	Normal
B[3]	A_CKERR_LATCH	CKERR latch register	0	CKERR ever occur
			1	Normal
B[2]	A_OVP_LATCH	OVP latch register	0	OV ever occur
			1	Normal
B[1:0]	X	Reversed		

- Address 0X3D : Protection latch clear register

The protection latch registers will show what kind of protection ever occurred.

Using the protection clear registers can clear the corresponding protection latch registers.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	A_OCP_N_CLEAR	OCP latch clear register	0	No clear
			1	Clear
B[6]	A_OTP_N_CLEAR	OTP latch clear register	0	No clear
			1	Clear
B[5]	A_UV_N_CLEAR	UV latch clear register	0	No clear
			1	Clear
B[4]	A_DCD_CLEAR	DCD latch clear register	0	No clear
			1	Clear
B[3]	A_CKERR_CLEAR	CKERR latch clear register	0	No clear
			1	Clear
B[2]	A_OVP_CLEAR	OVP latch clear register	0	No clear
			1	Clear
B[1:0]	X	Reversed		

- Address 0X5D : TDM word length selection

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:2]		Reserved		
B[1:0]	WORD_WIDTH_SEL	TDM word length selection	00	32 bits
			01	24 bits
			10	20 bits
			11	16 bits

- Address 0X5E : TDM offset

These bits control the offset of audio data in the audio frame for both input and output. The offset is defined as the number of BCLK from the starting (MSB) of audio frame to the starting of the desired audio sample

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	TDM_OFFSET	TDM offset bits	00000000	Offset is 0 BCLK
			00000001	Offset is 1 BCLK
			00000010	Offset is 2 BCLK
			…	
			11111101	Offset is 253 BCLK
			11111110	Offset is 254 BCLK
			11111111	Offset is 255 BCLK

- Address 0X5F : Analog gain

AD82111 provide several analog gains for different voltage application.

For 24V application, setting +15.5dB is suggested.

For 20V application, setting +14.5dB is suggested.

For 18V application, setting +13dB is suggested.

For 15V application, setting +11.5dB is suggested.

For 12V application, setting +9.5dB is suggested.

For 10V application, setting +8dB is suggested.

For 8V application, setting +6dB is suggested.

For 7V application, setting +5.1dB is suggested.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:3]		Reserved		
B[2:0]	ANA_GAIN	Analog gain control	000	X6(+15.5dB)
			001	X5(+14dB)
			010	X4.5(+13dB)
			011	X3.75(+11.5dB)
			100	X3(+9.5dB)
			101	X2.5(+8dB)
			110	X2(+6dB)
			111	X1.8(5.1dB)

- Address 0X60 : Output switching frequency selection

AD82111 provides output switching frequency selection which can be selected via bit 0.

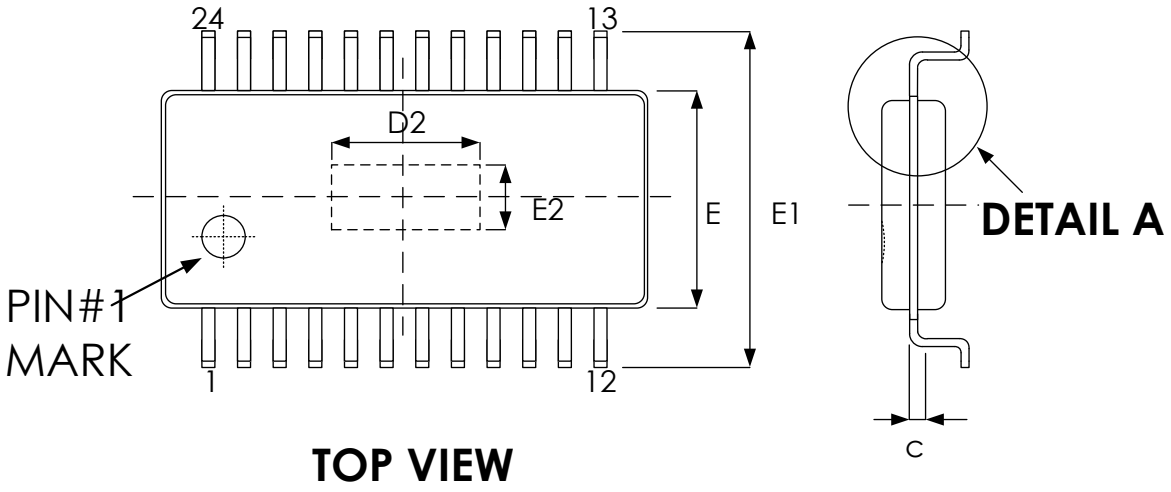
BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:1]		Prohibited		
B[0]	FSW	PWM frequency selection	0	300KHz
			1	600KHz

- Address 0X6F : Filter-less selection

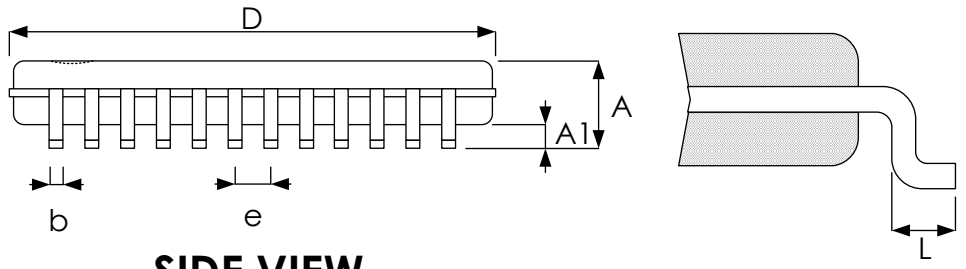
BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]		Prohibited		
B[6:5]	Filterless_SEL	EMI enhancement	00	Disabled
			01	Prohibited
			10	Prohibited
			11	Enable
B[4:0]		Prohibited		

Package Dimensions

E-TSSOP-24L (173 mil)



TOP VIEW



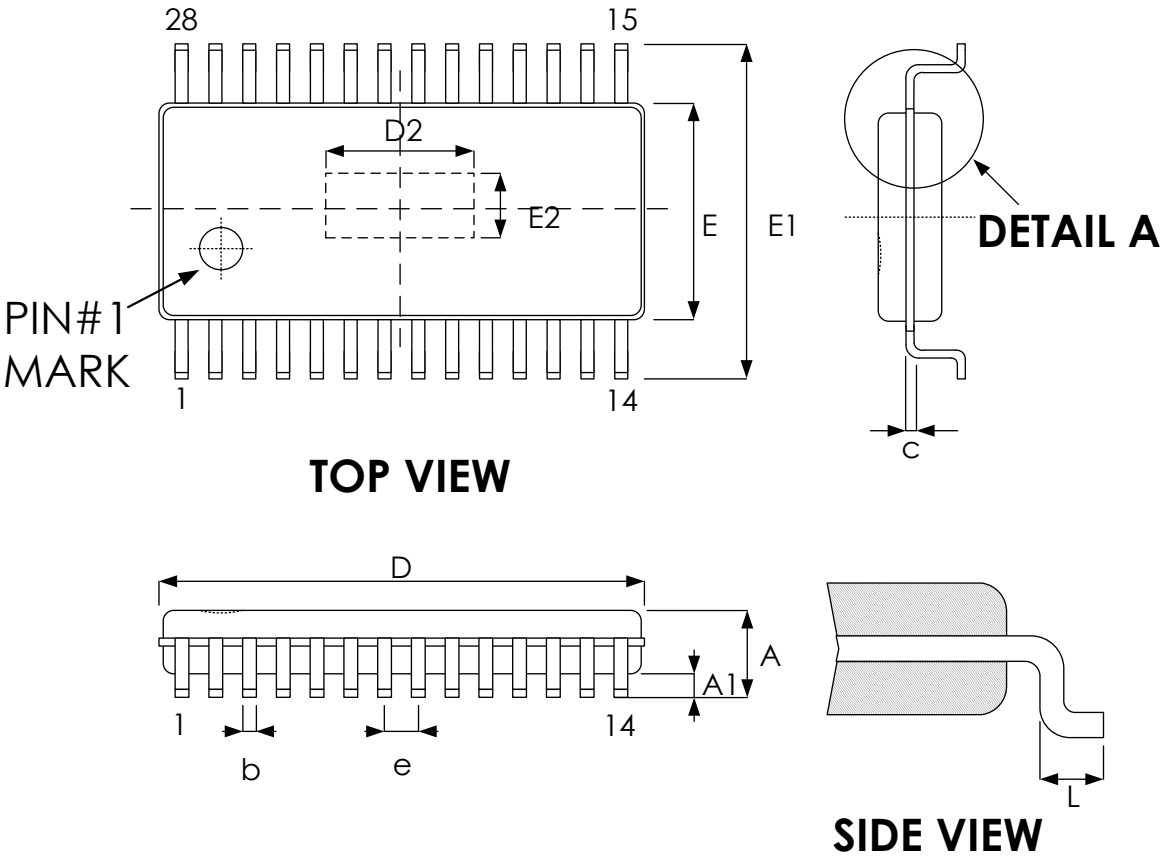
SIDE VIEW

Symbol	Dimension in mm	
	Min	Max
A	1.00	1.20
A1	0.00	0.15
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	4.30	4.50
E1	6.30	6.50
e	0.65 BSC	
L	0.45	0.75

Exposed pad

	Dimension in mm	
	Min	Max
D2	3.95	4.75
E2	2.70	3.10

E-TSSOP-28L (173 mil)



Symbol	Dimension in mm	
	Min	Max
A	--	1.20
A1	0.05	0.15
b	0.19	0.30
c	0.09	0.20
D	9.60	9.80
E	4.30	4.50
E1	6.30	6.50
e	0.65 BSC	
L	0.45	0.75

Exposed pad

	Dimension in mm	
	Min	Max
D2	5.00	6.40
E2	2.50	2.90

Revision History

Revision	Date	Description
0.1	2020.04.24	Original.
0.2	2020.07.14	1. Add 32 bits input signal format 2. Add PVCC condition for filter-less solution. 3. Modify the pin description 4. Modify the General Electrical Characteristics. 5. Modify the Electrical Characteristics and Specifications for Loudspeaker (Stereo) and (Mono). 6. Modify the description of internal PLL. 7. Add the description of dynamic temperature control and clock detection. 8. Add the application information about: power supply decoupling capacitor (Cs), boot-strap capacitor, ferrite bead selection, output LC filter and inductor selection. 9. Modify the description of Device addressing in I2C-Bus Transfer Protocol. 10. Modify the Register Table. 11. Modify the detail description for register for 0x00, 0x01, 0x02, 0x06, 0x13, 0x14, 0x15, 0x18, 0x29, 0x2B, 0x2E, 0x2D, 0x31, 0x32 and 0x60.
0.3	2020.09.21	Modify the description of Address 0X28.
0.4	2021.05.24	1. Modify power on sequence. 2. Modify the description of address 0X2A.
0.5	2021.06.21	1. Add E-TSSOP-28L package type 2. Modify the description of E-TSSOP-28L in Feature, Ordering Information, Pin Assignment, Functional Block Diagram, Available Package, Absolute Maximum Ratings, Recommended Operating Conditions, Marking Information, General Electrical Characteristics, Application Circuit Example, Data Format, Operation Description, Address 0X01, and Package Dimensions.
0.6	2021.07.02	Modify power on / off sequence.
0.7	2021.07.29	Modify Name and Description of Pin 15, 18, 20, and 21 in E-TSSOP 28L.

1.0	2021.08.24	Remove “Preliminary” and revise to 1.0 Ver. ,& Modify E-TSSOP 24L (173mil) package Dimensions D2 min value
1.1	2021.09.14	1. Modify pin name and description of Pin 13, 15, 17 and 18 for E-TSSOP 24L. 2. Modify pin name and description of Pin 15, 18, 20 and 21 for E-TSSOP 28L. 3. Modify Functional Block Diagram. 4. Modify Application Circuit Example for Stereo and Mono. 5. Modify power on / off sequence. 6. Modify Register Table for address 0X00 and description of address 0X00.
1.2	2022.05.03	Add the maximum and minimum value of $I_{SD(DVDD+DVDDIO)}$ and $I_{Q(DVDD+DVDDIO)}$.

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