2x15W Stereo / 1x19W Mono Class-D Audio Amplifier With Built-in Step-up Converter

Features

- Input voltage 2.9V~12V
- Adjustable boost converter output up to 14V
- Loudspeaker power @12V boost from 8.4V
  Stereo: 13W/CH into 4Ω @THD+N=1%
  Stereo: 15W/CH into 4Ω @ <10% THD+N
  Mono (PBTL):19W/CH into 4Ω @THD+N=10%
- Loudspeaker power @8V boost from 4.2V
  Stereo: 6W/CH into 4Ω @THD+N=1%
  Stereo: 7.5W/CH into 4Ω @ <10% THD+N
  Mono (PBTL): 8.7W/CH into 4Ω @THD+N=10%
- Differential inputs signal
- Fixed gain setting
- Internal oscillator
- Short-Circuit protection with auto recovery option
- Under-Voltage detection
- Over-Voltage protection
- Pop noise and click noise reduction
- Output DC detection for speaker protection
- Filter-Free operation
- Over temperature protection with auto recovery
- Superior EMC performance

Applications

- Blue-tooth Box
- Portable Media
- Audio Docking System
- Tablet Personal PC
- Consumer Audio Equipment

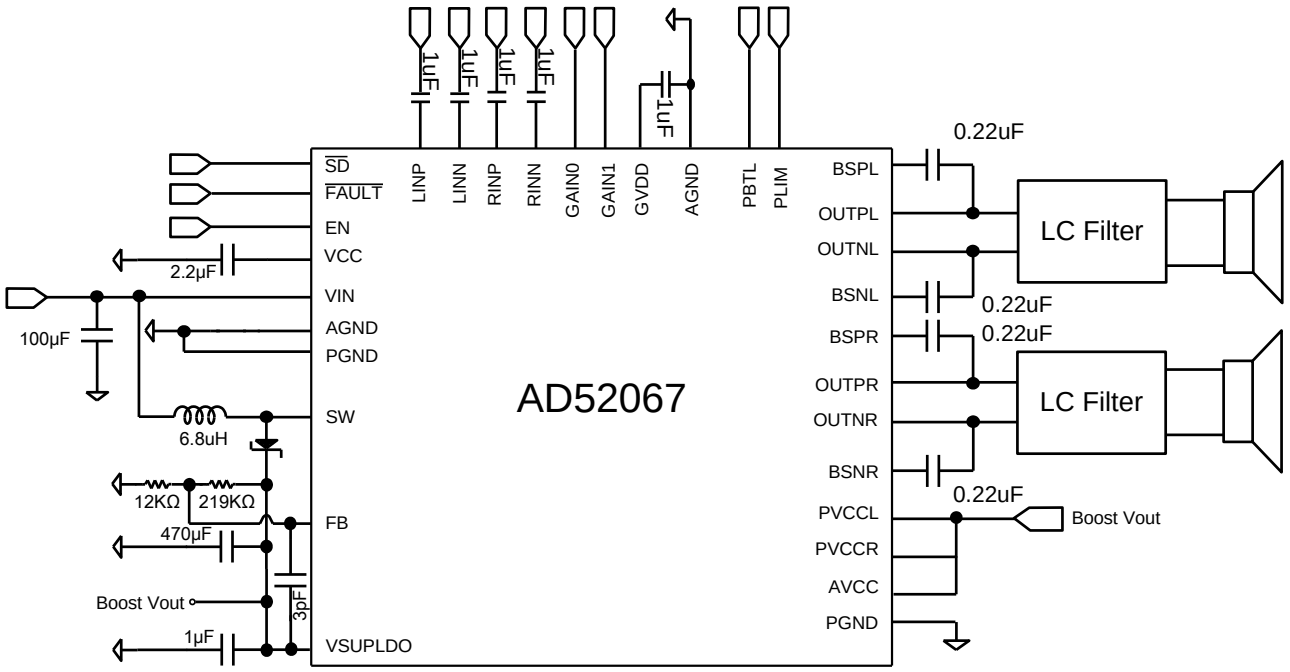
Description

The AD52067 is a high efficiency stereo class-D audio amplifier with built-in boost DC-DC converter. The loudspeaker driver can deliver stereo 15W/CH output power into 4Ω loudspeaker under 10% THD+N at two-cell Li-ion battery (8.4V).

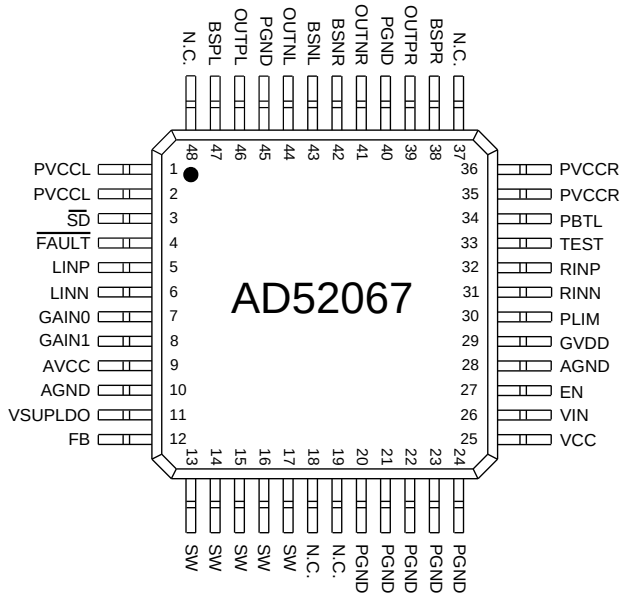
AD52067 provides parallel BTL (Mono) application also, and it can deliver 19W into 4Ω loudspeaker at 8.4V supply voltage.

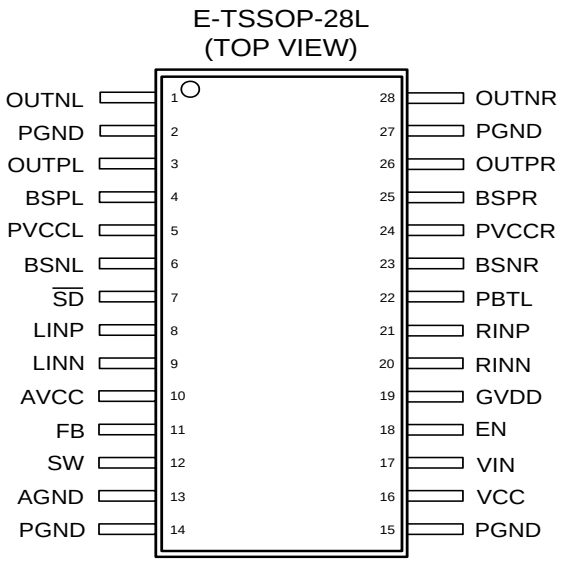
Output DC detection prevents speaker damage from long-time current stress. AD52067 provides superior EMC performance for filter-free application. The output short circuit and over temperature protection include auto-recovery feature.

Simplified Application Circuit



Pin Assignments





Pin Description

NAME	E-LQFP-48L	E-TSSOP-28L	TYP	DESCRIPTION
PVCCL	1	5	P	High-voltage power supply for left-channel. Right channel and left channel power supply inputs are connect internal.
PVCCL	2	5	P	High-voltage power supply for left-channel. Right channel and left channel power supply inputs are connect internal.
$\overline{SD}$	3	7	I	Shutdown signal for IC (low = disabled, high = operational). Voltage compliance to AVCC.
$\overline{FAULT}$	4	N/A	O	Open drain output used to display short circuit or dc detect fault. Voltage compliant to AVCC. Short circuit faults can be set to auto-recovery by connecting FAULTB pin to $\overline{SD}$ pin. Otherwise, both short circuit faults and dc detect faults must be reset by cycling AVCC.
LINP	5	8	I	Positive audio input for left channel.
LINN	6	9	I	Negative audio input for left channel.
GAIN0	7	N/A	I	Gain select least significant bit. Voltage compliance to AVCC.
GAIN1	8	N/A	I	Gain select least significant bit. Voltage compliance to AVCC.
AVCC	9	10	P	Analog supply.
AGND	10	13	P	Boost ground pin
VSUPLDO	11	N/A	P	Boost converter output for internal regulator.
FB	12	11	I	Receives the feedback voltage from an external resistive divider across the output.
SW	13,14,15,16,17	12	O	Must be connected an Inductor from VCC pin to SW pin for boost and rectifying switches.
N.C.	18,19	N/A		Not connected.

PGND	20,21,22,23,24	2,14,15,16,27	P	Power Switch Ground Pin.
VCC	25	16	P	A ceramic capacitor of more than 2.2uF requirement between this pin and GND.
VIN	26	17	P	Must be closely decoupled to GND pin with 470uF*1or greater ceramic capacitor.
EN	27	18	I	Boost enable pin (high=Enable; low=Disable).
AGND	28	N/A	P	Analog signal ground. Connect to the thermal pad.
GVDD	29	19	P	5V regulated output, also used as supply for PLIMIT function.
PLIM	30	N/A	O	Power limit level adjustment. Connect a resistor divider from GVDD to GND to set power limit. Give V(PLIMIT) <2.4V to set power limit level. Connect to GVDD (>2.4V) or GND to disable power limit function.
RINN	31	20	I	Negative audio input for right channel. Biased at 2.5V.
RINP	32	21	I	Positive audio input for right channel. Biased at 2.5V.
TEST	33	N/A	I	Test mode pin.
PBTL	34	22	I	Parallel BTL mode switch, high for parallel BTL output. Voltage compliance to AVCC.
PVCCR	35	24	P	High-voltage power supply for right-channel. Right channel and left channel power supply inputs are connect internal.
PVCCR	36	24	P	High-voltage power supply for right-channel. Right channel and left channel power supply inputs are connect internal.
N.C.	37	N/A		Not connected.
BSPR	38	25	I	Bootstrap I/O for right channel, positive high side FET.
OUTPR	39	26	O	Class-D H-bridge positive output for right channel.
PGND	40	27	P	Power ground for the H-bridges.
OUTNR	41	28	O	Class-D H-bridge negative output for right channel.
BSNR	42	23	I	Bootstrap I/O for right channel, negative high side FET.
BSNL	43	6	I	Bootstrap I/O for left channel, negative high side FET.
OUTNL	44	1	O	Class-D H-bridge negative output for left channel.
PGND	45	15		Power ground for the H-bridges.
OUTPL	46	3	P	Class-D H-bridge positive output for left channel.
BSPL	47	4		Bootstrap I/O for left channel, positive high side FET.
N.C.	48	N/A	O	Not connected.
Thermal Pad			P	Must be soldered to PCB's ground plane.

Note:

P: Power or ground pins; I: Input pins; O: Output pins; I/O: The bidirectional pins

Ordering Information

Product ID	Gain	Package	Packing / MPQ	Comments
AD52067-26QG28NRT	+26dB	E-TSSOP 28L	50Units / Tube 100 Tubes / Small Box	Green
AD52067-26QG28NRR	+26dB	E-TSSOP 28L	2500 Units / Reel 2500 Units / Small Box	Green
AD52067-00LG48NRY (By Request)	Adjustable	E-LQFP 48L (7mmX7mm)	250 Units / Tray 2.5K Units / Box (10 Tray)	Green
AD52067-00LG48NRR (By Request)	Adjustable	E-LQFP 48L (7mmX7mm)	2K Units / Reel 1 Reel / Box	Green

Available Package

Package Type	Device No.	θ_{ja}(℃/W)	θ_{jt} (℃/W)	Ψ_{jt} (℃/W)	Exposed Thermal Pad
E-LQFP-48L (7mmX7mm)	AD52067	22.9	34.9	1.64	Yes (Note1)
E-TSSOP 28L		28	27.1	1.33	Yes (Note 1)

Note 1.1: The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is suggested.

Note 1.2: θ_{JA} is measured on a room temperature (T_A=25℃), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The measurement is tested using the JEDEC51-5 thermal measurement standard.

Note 1.3: $\theta_{JC\ (top)}$ represents the heat resistance for the heat flow between the chip and the package's top surface. (The junction-to-top thermal resistance is obtained by simulating a cold plate test on the top of the package).

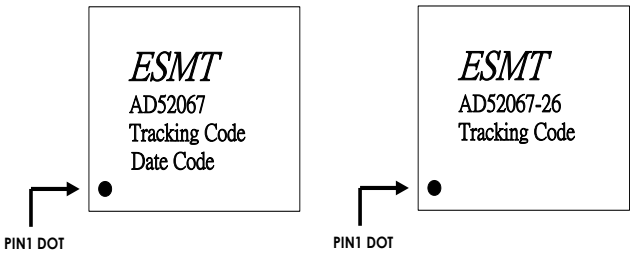
Note 1.4: $\Psi_{JC(bottom)}$ represents the heat resistance for the heat flow between the chip and the exposed pad center. (The junction-to-top characterization parameter is extracted from the simulation data to obtainθ_{ja}).

Marking Information

AD52067

- Marking Information

Line 1：LOGO
Line 2：Product No
Line 3：Tracking Code
Line 4：Date Code



E-LQFP 48L E-TSSOP 28L

Absolute Maximum Ratings

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
VIN	Supply voltage	VIN	-0.3	16	V
$V_{I(Boost)}$	Interface pin voltage for boost	EN, FB, VCC	-0.3	6	V
	Boost switch pin	LX	-0.3	16	V
PVCC	Class-D supply voltage	PVCCL, PVCCR, AVCC	-0.3	16	V
$V_{I(Class-D)}$	Interface pin voltage	$\overline{SD}$, PBTL,	-0.3	16	V
T_J	Operating junction temperature range		-40	150	°C
T_{stg}	Storage temperature range		-65	150	°C
R_L	Minimum Load Resistance	BTL, PBTL	3.2		Ω

Recommended Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
VIN	Supply voltage	VIN	2.9	12	V
PVCC	Class-D supply voltage	PVCCL, PVCCR, AVCC	5	14	V
V_{IH}	High-level input voltage	$\overline{SD}$, PBTL	2		V
		EN	1.2		
V_{IL}	Low-level input voltage	$\overline{SD}$, PBTL, EN		0.4	V
T_A	Operating free-air		-40	85	°C

Boost General Electrical Characteristics

- T_A=25°C (unless otherwise noted)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN_UVLO}	VIN UVLO Threshold	V_{IN} rising		2.6		V
	VIN UVLO Threshold	V_{IN} falling		2.4		V
F_{OSC}	Operation Frequency	V_{FB}=0.5V		500		kH_Z
T_{DUTY}	Maximum Duty Cycle			90		%
V_{REF}	Reference Voltage			0.6		V
I_{LIM}	Current Limit	V_{IN}=6V, V_{EN}=1.2V		6.5		A
	EN Pull down resistor			800		kΩ

Audio General Electrical Characteristics

- PVCC=8V, R_L=4Ω, T_A=25°C (unless otherwise noted)

SYMBOL	PARAMETER	CONDITION		MIN	TYP	MAX	UNIT
$R_{DS(on)}$	Drain-source on-state resistance-High side NMOS	PVCC=8V, Id=250mA, T_J=25 °C			220		mΩ
	Drain-source on-state resistance-Low side NMOS				220		mΩ
$\|V_{OS}\|$	Class-D output offset voltage (measured differential)	PVCC=8V V_I=0V, Gain=36dB			1.5	15	mV
t_{ON}	Turn-on time	SD=2V			90		ms
t_{OFF}	Turn-off time	SD=0.8V			2		μs
GVDD	Regulator output	I_{GVDD}=0.1mA		4.75	5	5.25	V
fosc	Oscillator frequency			250	310	370	kHz
G	Gain	GAIN1 =0.8V	GAIN0=0.8V	19	20	21	dB
			GAIN0=2V	25	26	27	
		GAIN1 =2V	GAIN0=0.8V	31	32	33	
			GAIN0=2V	35	36	37	
		For product ID of AD52067-26QG28NRT only (E-TSSOP-28L)		25	26	27	

Electrical Characteristics and Specifications of Loudspeaker Driver

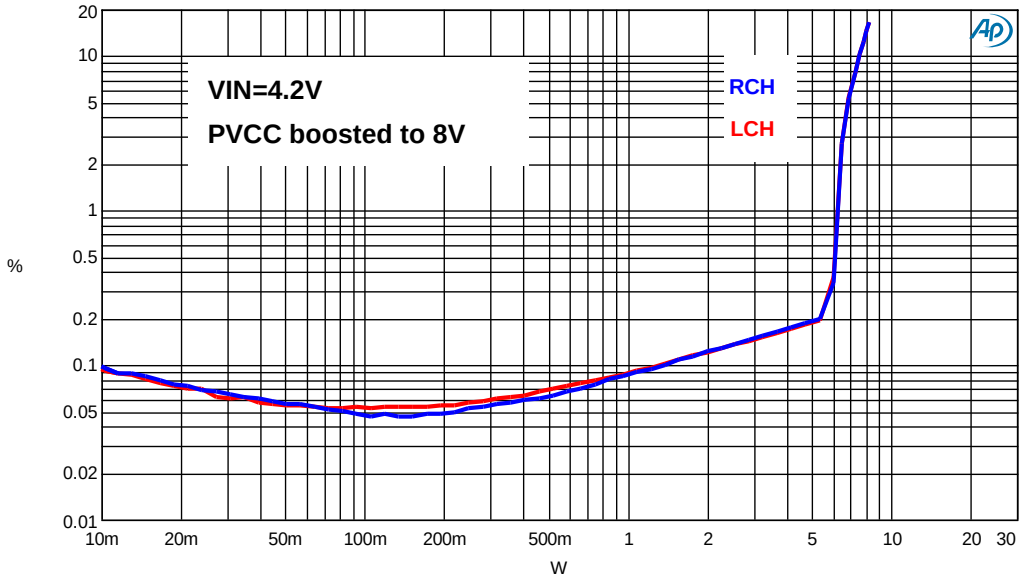
● Stereo Output (BTL Output)

Condition: VIN=4.2V, PVCC boosted to 8V, R_L=4Ω+33uH, Common mode filter=15uH+2.2uF, T_A=25°C (unless otherwise noted)

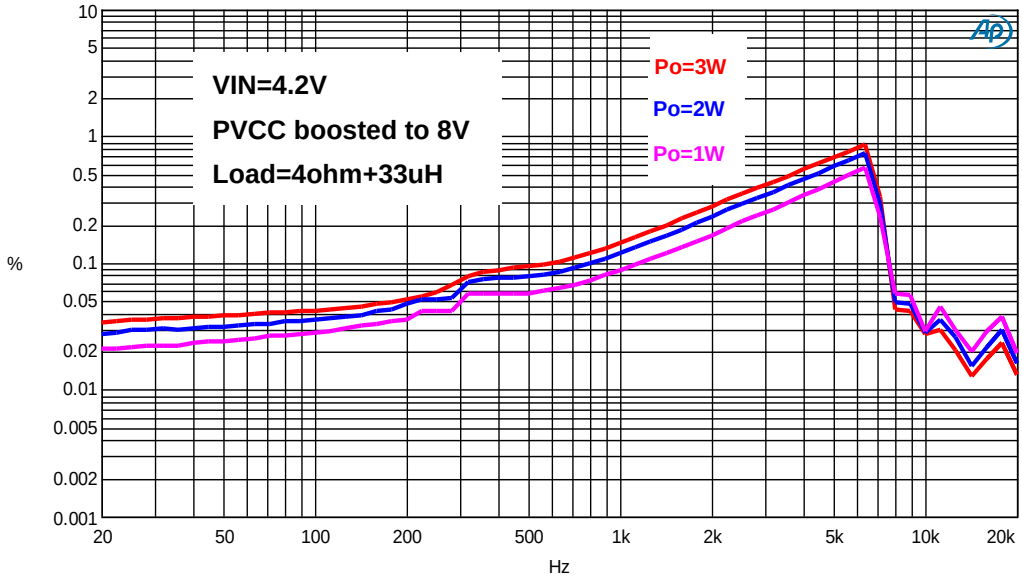
SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Po	Output power	THD+N=1%, f=1kHz, PVCC=8V		6		W
		THD+N=10%, f=1kHz, PVCC=8V		7.5		
THD+N	Total harmonic distortion plus noise	PVCC=8V, f=1kHz, P_O=2W		0.13		%
		PVCC=8V, f=1kHz, P_O=5W		0.2		
SNR	Signal to noise ratio	Maximum output at THD+N<1%, f=1kHz, Gain=20dB, a-weighted		91		dB
V_n	Output integrated noise	F=20Hz ~ 20kHz, Gain=26dB, a-weighted filter,		125		μV
K_{SVR}	Power Supply Rejection Ratio	V_{ripple}=200mVpp at 1kHz, Gain=26dB, inputs ac-grounded		-70		dB
Crosstalk	Crosstalk	F=1kHz, V_O=1Vrms, Gain=26dB		-90		dB
I_Q	Quiescent Current	VIN=4.2V, PVCC=8V		30		mA
I_{SD}	Shutdown Current	VIN=4.2V, PVCC=8V		45		uA

Note: Po measurement is probed at the terminal on the EVB.

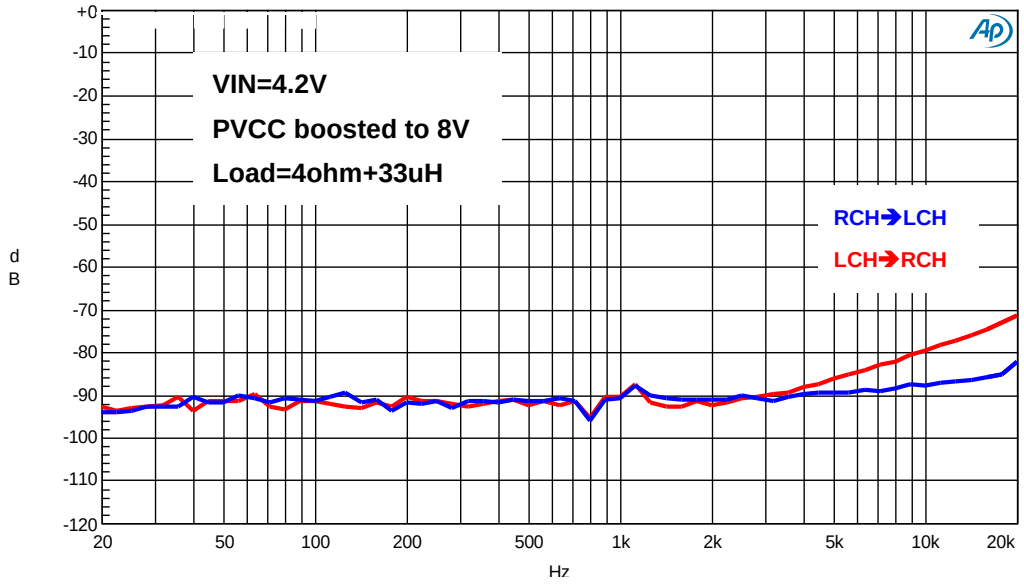
THD + N (%) vs. Output power (8ohm+66uH load)



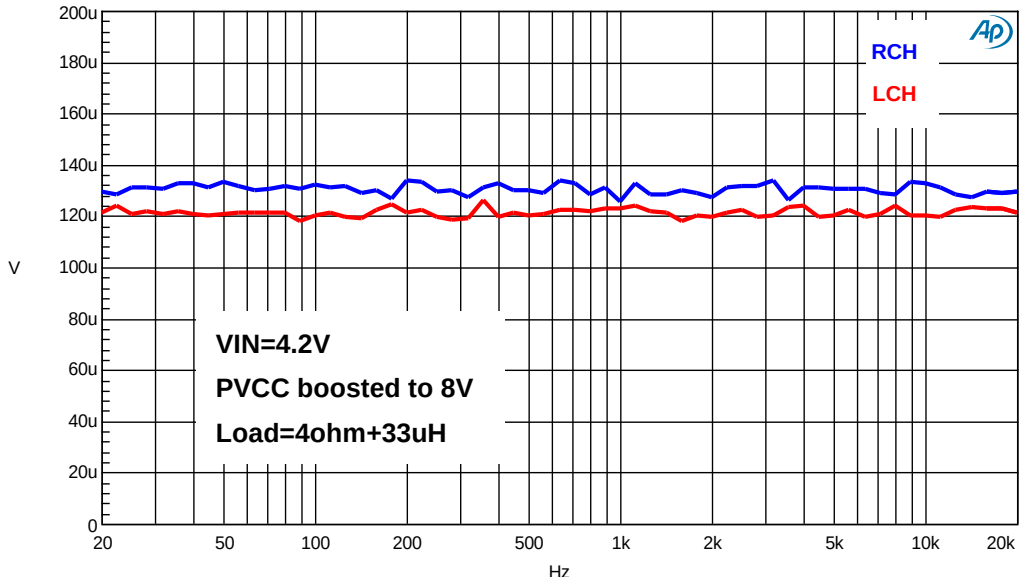
THD + N (%) vs. Frequency



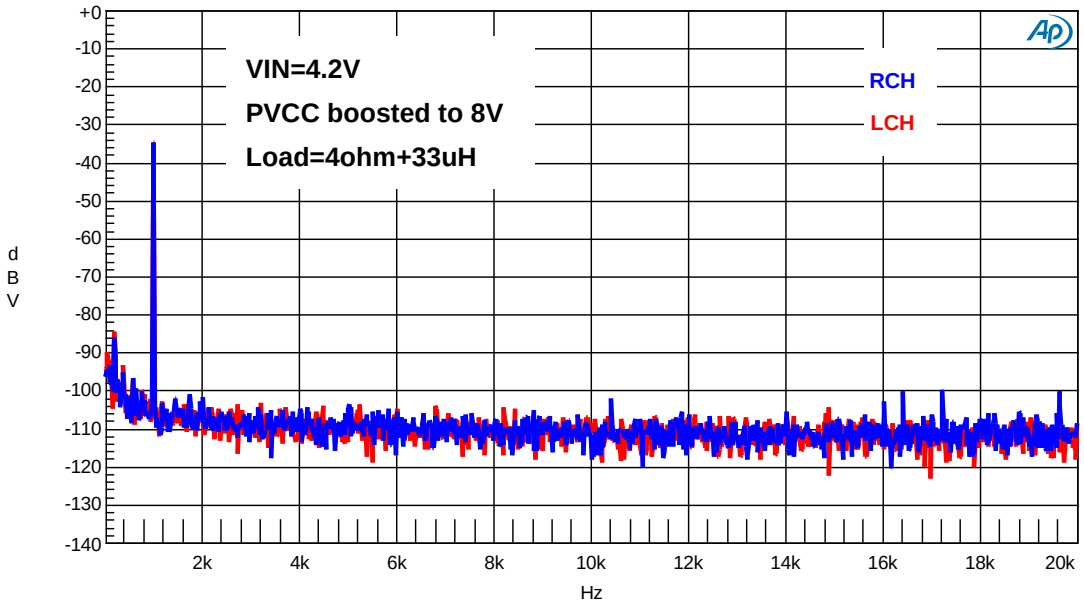
Crosstalk



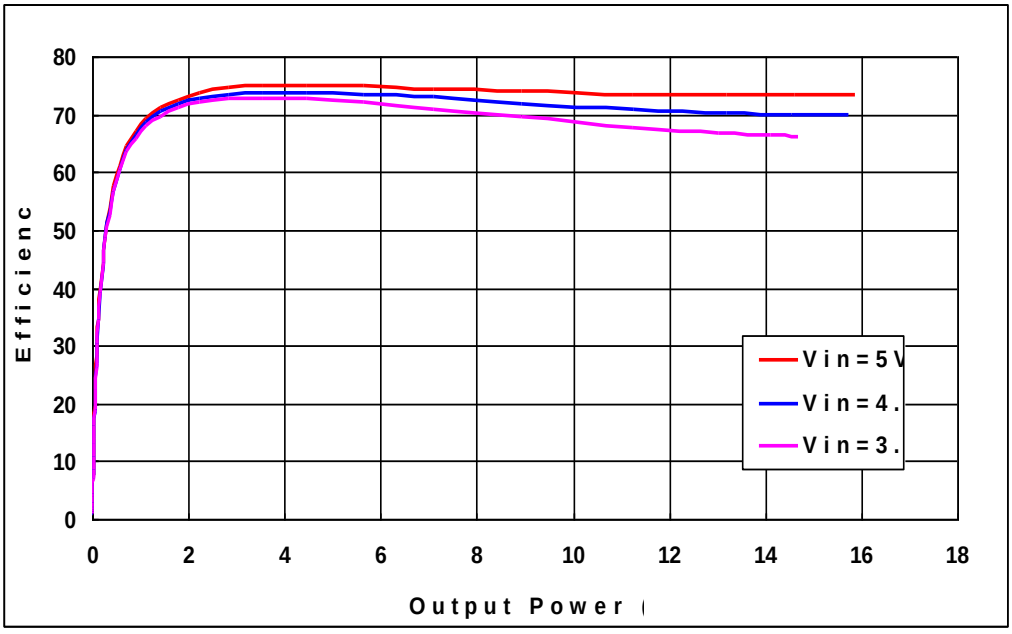
Noise



DR



Efficiency (4ohm+33uH load) / 2ch, PVCC boosted to 8V



Electrical Characteristics and Specifications of Loudspeaker Driver

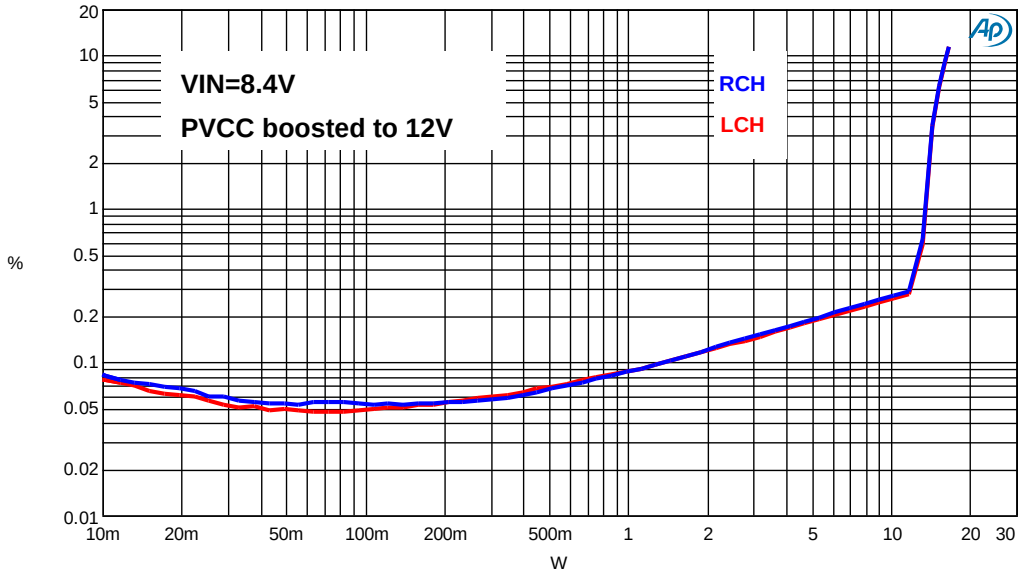
● Stereo Output (BTL Output)

Condition: VIN=8.4V, PVCC boosted to 12V, R_L=4Ω+33uH, Common mode filter=15uH+2.2uF,T_A=25°C (unless otherwise noted)

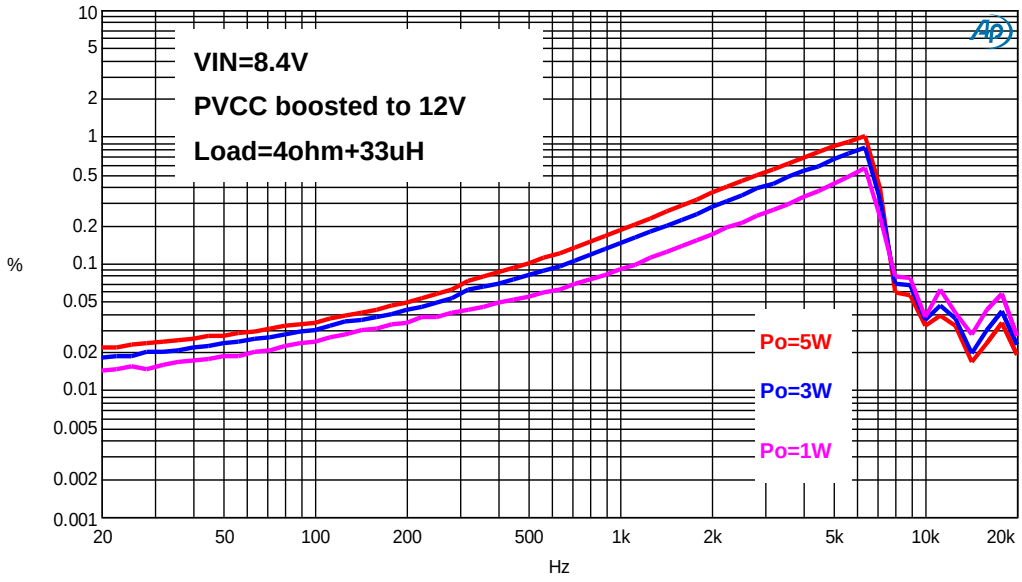
SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Po	Output power	THD+N=1%, f=1kHz, PVCC=12V		13		W
		THD+N<10%, f=1kHz, PVCC=12V		15		
THD+N	Total harmonic distortion plus noise	PVCC=12V, f=1kHz, P_O=5W		0.2		%
		PVCC=12V, f=1kHz, P_O=10W		0.28		
SNR	Signal to noise ratio	Maximum output at THD+N<1%, f=1kHz, Gain=26dB, a-weighted		96		dB
V_n	Output integrated noise	F=20Hz ~ 20kHz, Gain=26dB, a-weighted filter,		113		μV
K_{SVR}	Power Supply Rejection Ratio	V_{ripple}=200mVpp at 1kHz, Gain=20dB, inputs ac-grounded		-70		dB
Crosstalk	Crosstalk	F=1kHz, V_O=1Vrms, Gain=20dB		-98		dB
I_Q	Quiescent Current	VIN=8.4V, PVCC=12V		26		mA
I_{SD}	Shutdown Current	VIN=8.4V, PVCC=12V		90		uA

Note: Po measurement is probed at the terminal on the EVB.

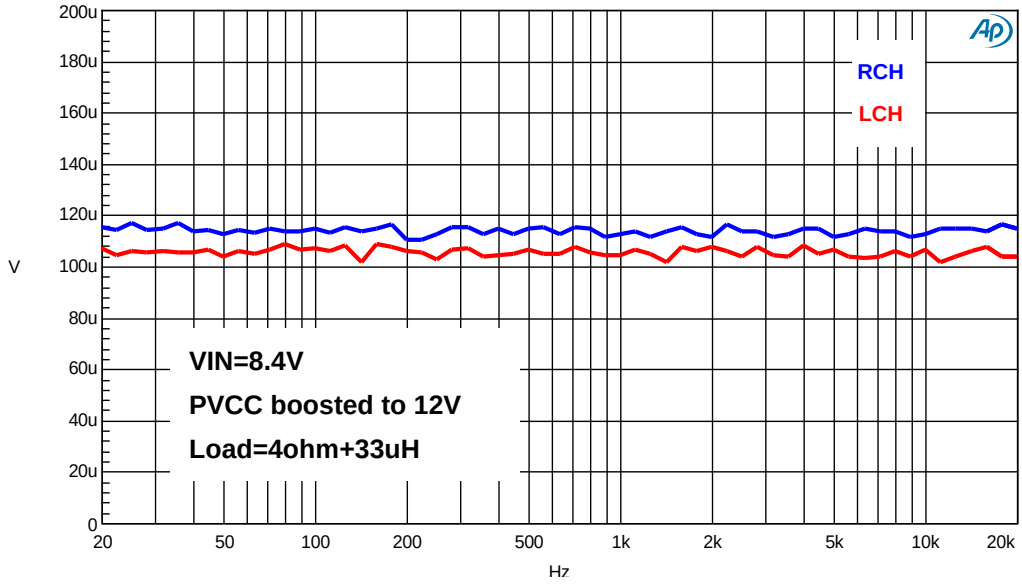
THD + N (%) vs. Output power (4ohm+33uH load)



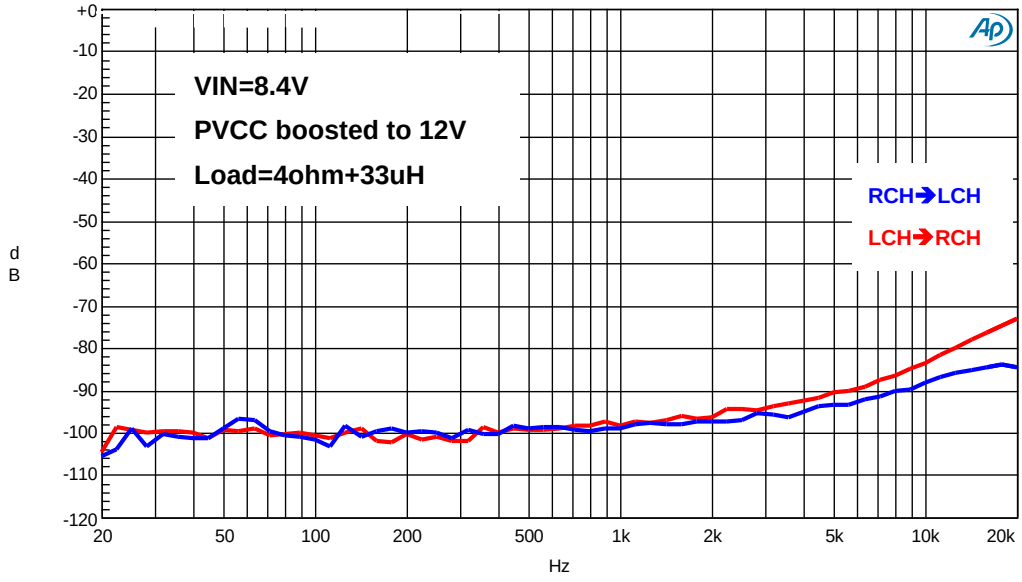
THD + N (%) vs. Frequency



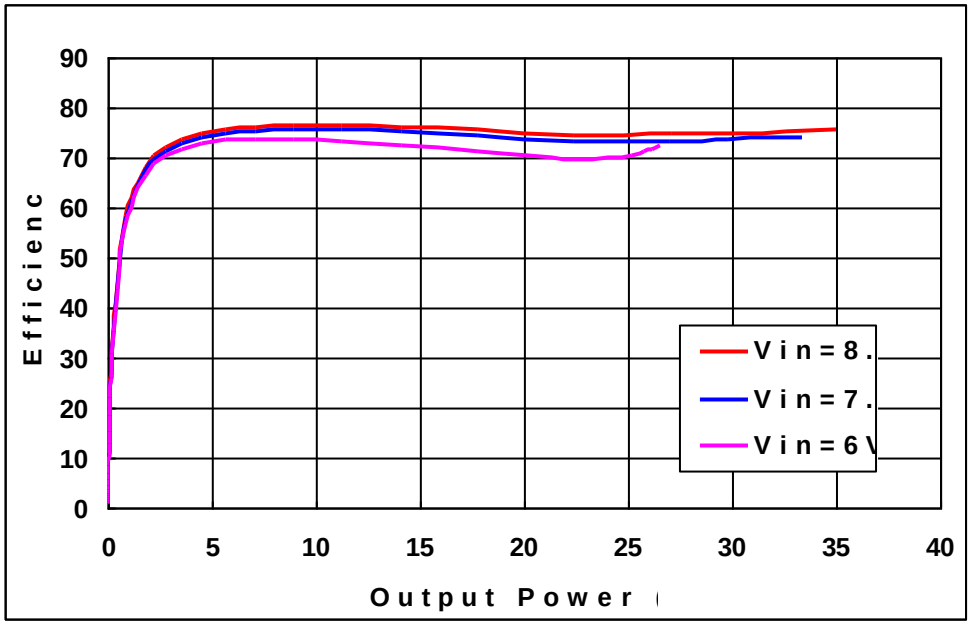
Noise



Crosstalk



Efficiency (4ohm+33uH load) / 2ch, PVCC boosted to 12V



Electrical Characteristics and Specifications of Loudspeaker Driver

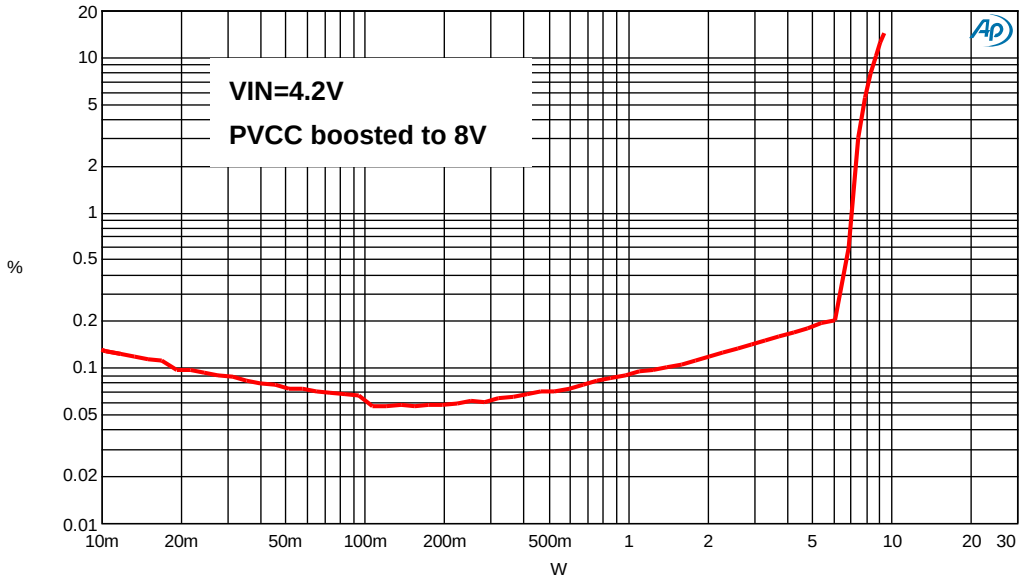
● Mono Output (PBTL Output)

Condition: VIN=4.2V, PVCC boosted to 8V, R_L=4Ω+33uH, Common mode filter=15uH+2.2uF, T_A=25°C (unless otherwise noted)

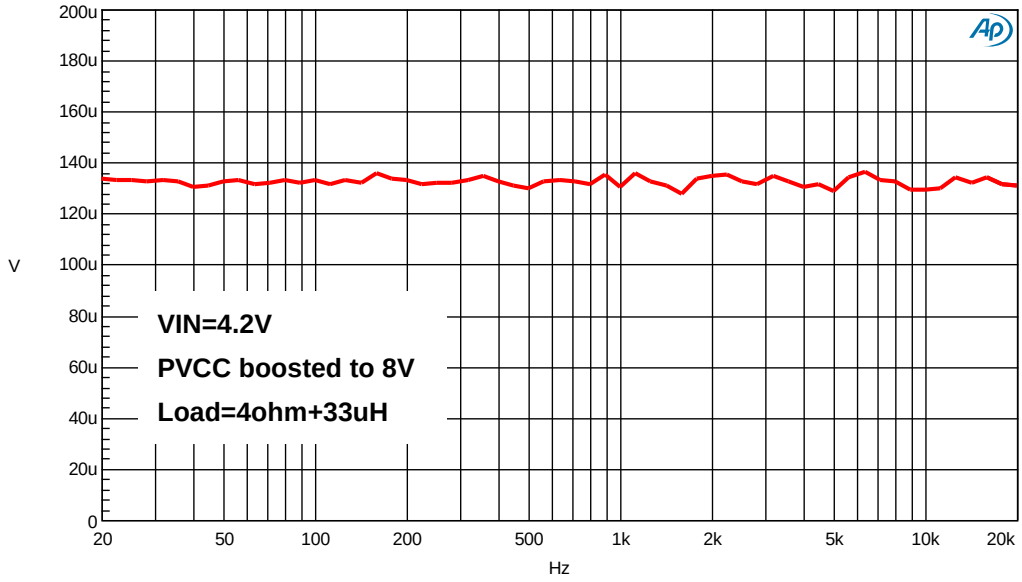
SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
P_O	Output power	THD+N=1%, f=1kHz, PVCC=8V		7		W
		THD+N=10%, f=1kHz, PVCC=8V		8.7		
THD+N	Total harmonic distortion plus noise	PVCC=8V,f=1kHz, P_O=6W		0.2		%
		PVCC=8V,f=1kHz, P_O=3W		0.15		
SNR	Signal to noise ratio	Maximum output at THD+N<1%, f=1kHz, Gain=20dB, a-weighted		91		dB
V_n	Output integrated noise	F=20Hz ~ 20kHz, Gain=20dB, a-weighted filter, R_L=8Ω		131		μV
K_{SVR}	Power Supply Rejection Ratio	V_{ripple}=200mVpp at 1kHz, Gain=20dB, inputs ac-grounded		-70		dB
I_Q	Quiescent Current	VIN=4.2V, PVCC=8V		30		mA
I_{SD}	Shutdown Current	VIN=4.2V, PVCC=8V		45		uA

Note: Po measurement is probed at the terminal on the EVB.

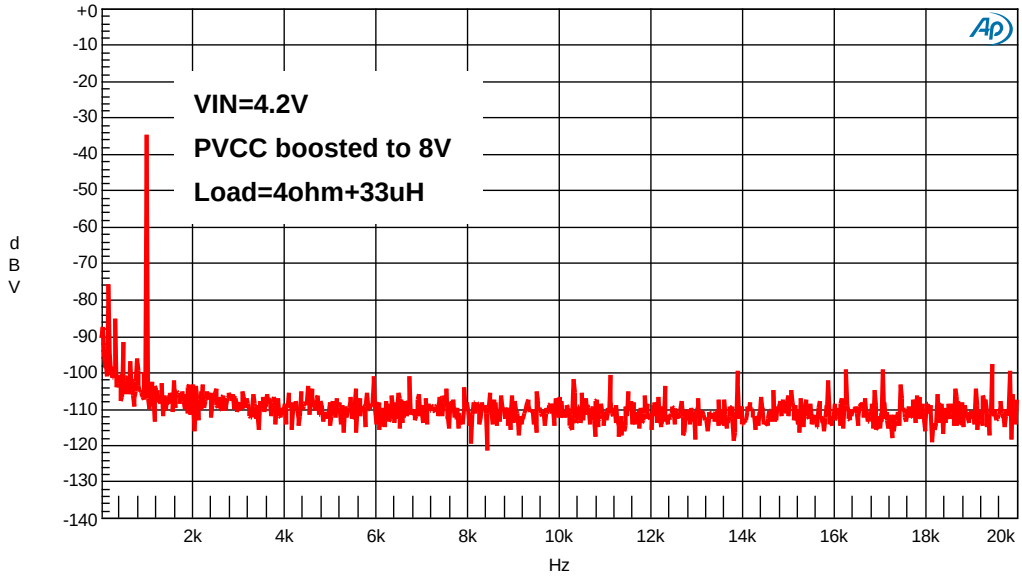
THD + N (%) vs. Output power (4ohm+33uH load)



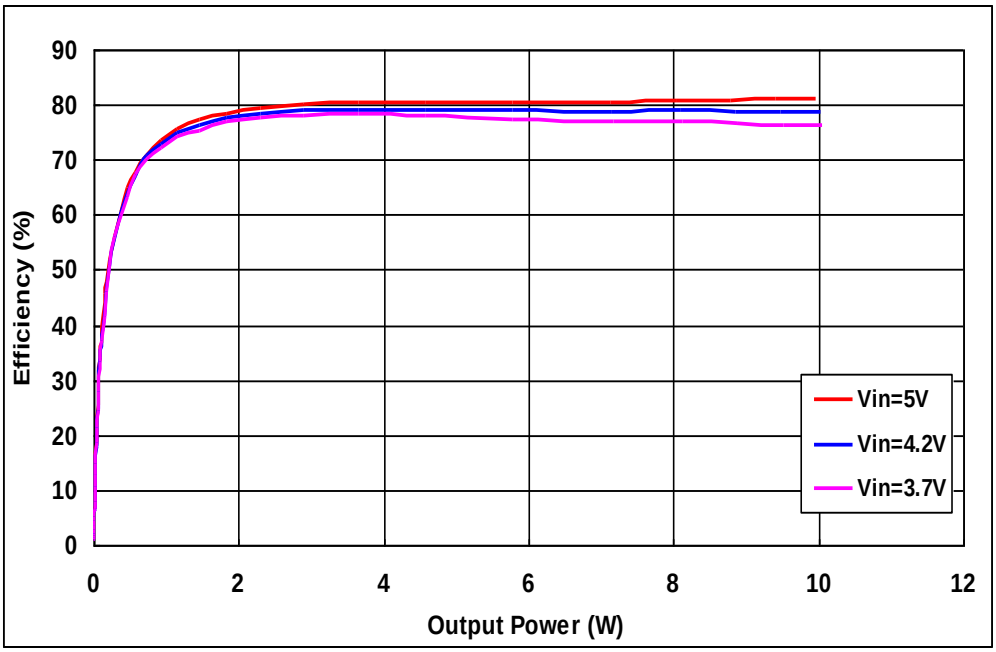
Noise


200u
180u
160u
140u
120u
100u
80u
60u
40u
20u
0
V
VIN=4.2V
PVCC boosted to 8V
Load=4ohm+33uH
20
50
100
200
500
1k
2k
5k
10k
20k
Hz

DR


+0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
-110
-120
-130
-140
dBV
VIN=4.2V
PVCC boosted to 8V
Load=4ohm+33uH
2k
4k
6k
8k
10k
12k
14k
16k
18k
20k
Hz

Efficiency (4ohm+33uH load) , PVCC boosted to 8V



Electrical Characteristics and Specifications of Loudspeaker Driver

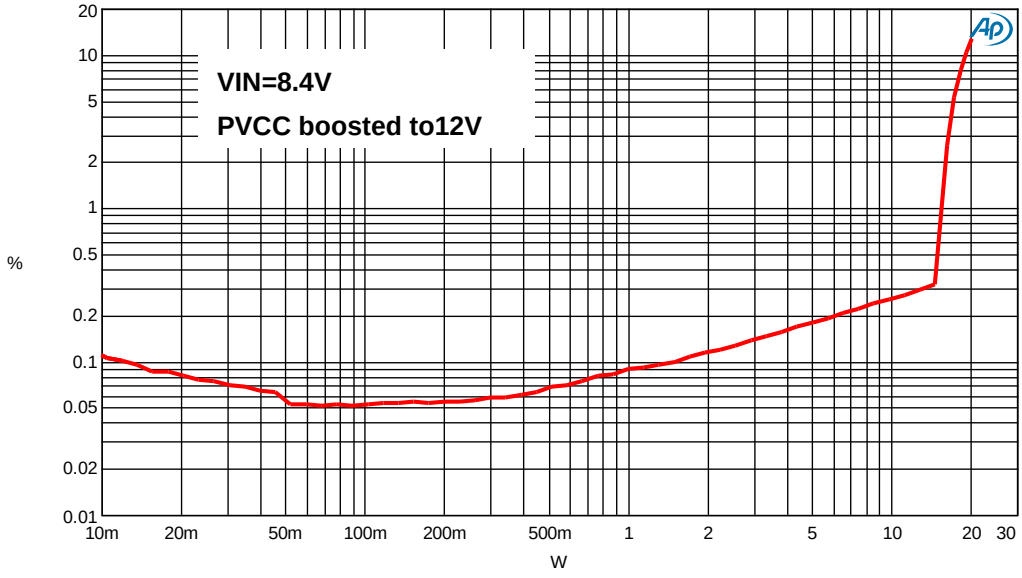
● Mono Output (PBTL Output)

Condition: VIN=8.4V, PVCC boosted to 12V, R_L=4Ω+33uH, Common mode filter=15uH+2.2uF, T_A=25°C (unless otherwise noted)

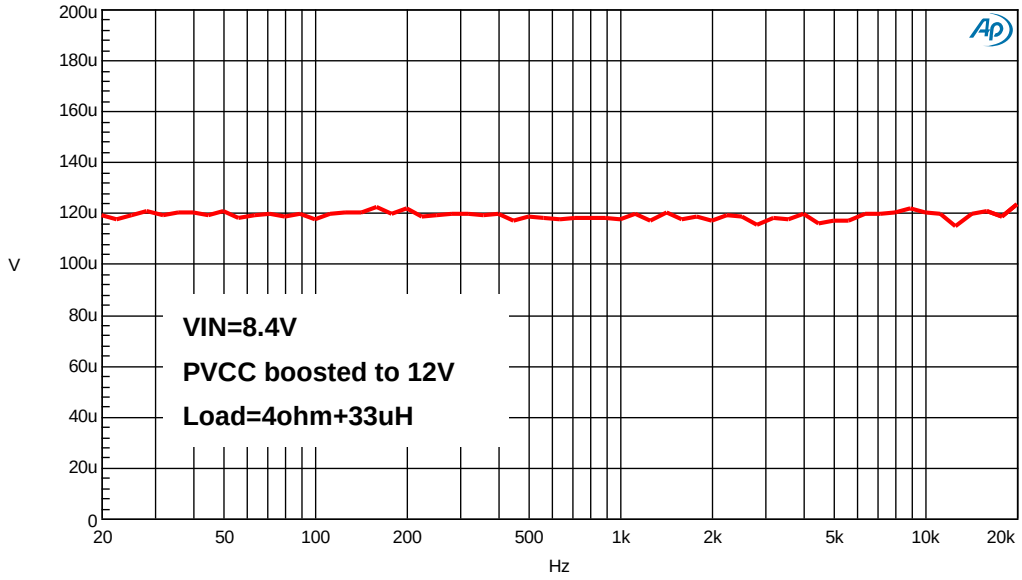
SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
P_O	Output power	THD+N=1%, f=1kHz, PVCC=12V		16		W
		THD+N=10%, f=1kHz, PVCC=12V		19		
THD+N	Total harmonic distortion plus noise	PVCC=12V, f=1kHz, P_O=5W		0.18		%
		PVCC=12V, f=1kHz, P_O=10W		0.26		
SNR	Signal to noise ratio	Maximum output at THD+N<1%, f=1kHz, Gain=20dB, a-weighted		97		dB
V_n	Output integrated noise	F=20Hz ~ 20kHz, Gain=20dB, a-weighted filter, R_L=8Ω		120		μV
K_{SVR}	Power Supply Rejection Ratio	V_{ripple}=200mVpp at 1kHz, Gain=20dB, inputs ac-grounded		-70		dB
I_Q	Quiescent Current	VIN=8.4V, PVCC=12V		26		mA
I_{SD}	Shutdown Current	VIN=8.4V, PVCC=12V		90		uA

Note: Po measurement is probed at the terminal on the EVB.

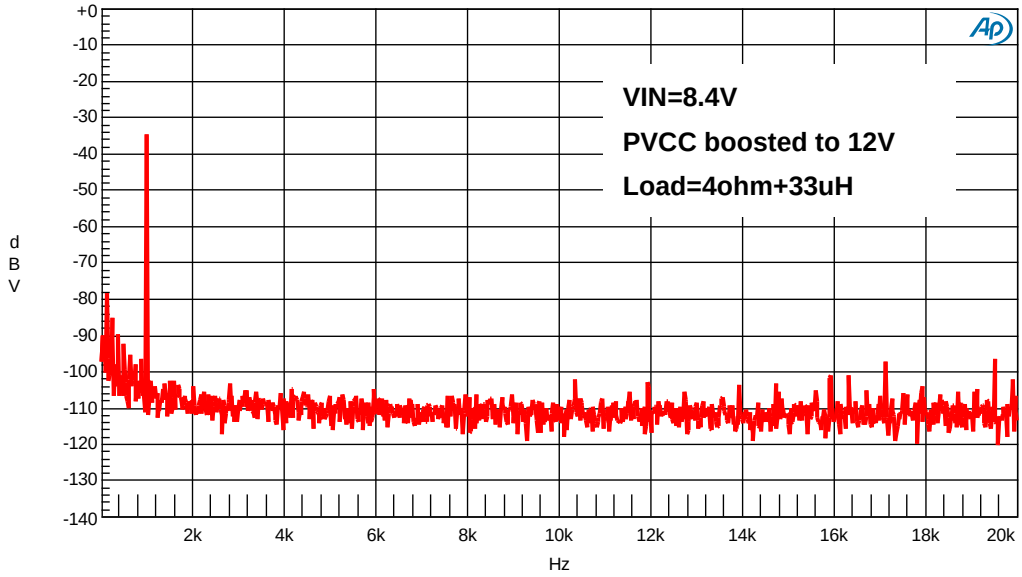
THD + N (%) vs. Output power (4ohm+33uH load)



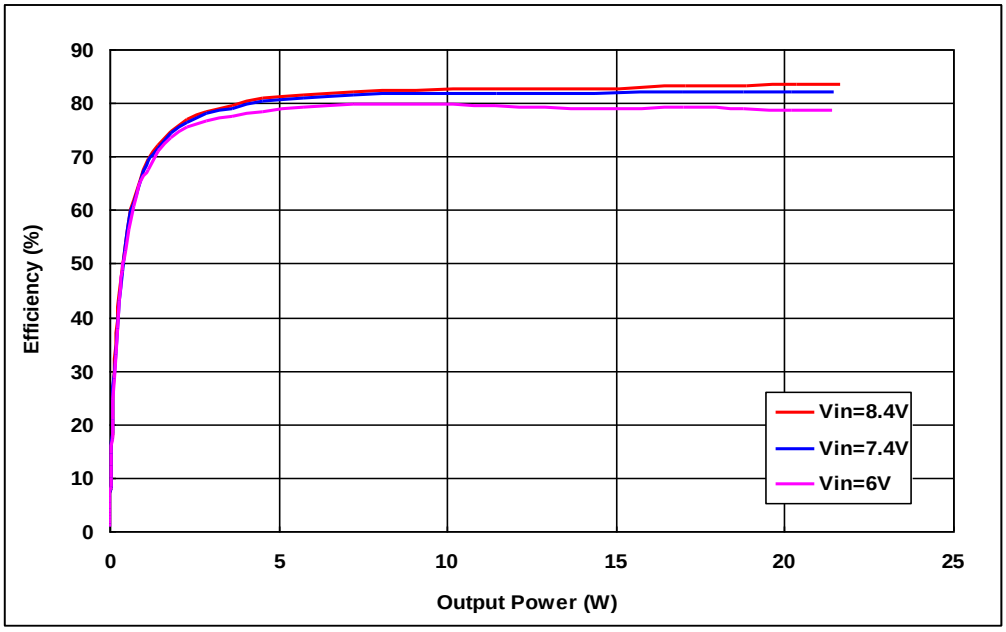
Noise


200u
180u
160u
140u
120u
100u
80u
60u
40u
20u
0
V
VIN=8.4V
PVCC boosted to 12V
Load=4ohm+33uH
20
50
100
200
500
1k
2k
5k
10k
20k
Hz

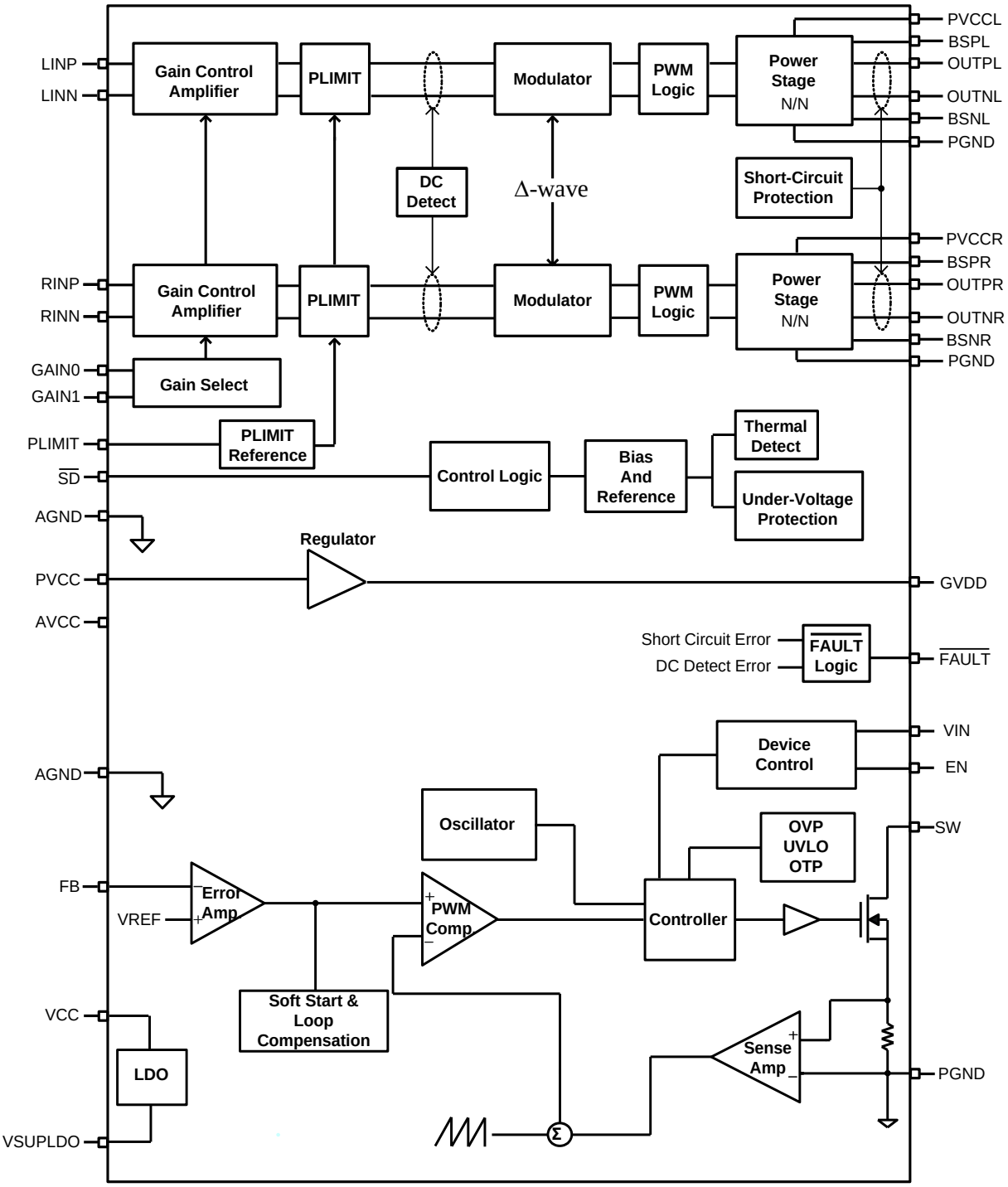
DR


+0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
-110
-120
-130
-140
dBV
VIN=8.4V
PVCC boosted to 12V
Load=4ohm+33uH
2k
4k
6k
8k
10k
12k
14k
16k
18k
20k
Hz

Efficiency (4ohm+33uH load) , PVCC boosted to 12V



Functional Block Diagram



Boost Converter Operation Description

- **Detailed Description**

  The AD52067 with a current mode boost converter. The constant switching frequency is 500kHz and operates with pulse width modulation (PWM). The control loop architecture is peak current mode control; therefore slope compensation circuit is added to the current signal to allow stable operation for duty cycles larger than 50%.

- **Soft Start**

  Soft start circuitry is integrated into AD52067 to avoid inrush current during power on. After the IC is enabled, the output of error amplifier is clamped by the internal soft-start function, which causes PWM pulse width increasing slowly and thus reducing input surge current.

- **Over Temperature Protection**

  AD52067 will turn off the power MOSFET automatically when the internal junction temperature is over 160°C. The power MOSFET wake up when the junction temperature drops 30°C under the OTP threshold temperature.

- **Over Voltage Protection**

  The AD52067 has output over-voltage protections. The thresholds output OVP circuit minimum 118% x VOUT, respectively. Once the output voltage is higher than the threshold, the NMOS driver is turned off. When the output voltage drops lower than the threshold, the NMOS will be turned on again.

- **Over Current Protection**

  The AD52067 cycle-by-cycle limits the peak inductor current to protect NMOS driver. The NMOS driver will turn off when switching current reaches OCP level.

Audio Operation Description

- **Gain settings**

  The gain of the AD52067 is set by two input pins, GAIN0 and GAIN1. By varying input resistance in AD52067, the various volume gains are achieved. The respective volume gain and input resistance are listed in Table 1. However, there is 20% variation in input resistance from production variation.

Table 1. Volume gain and input impedance

GAIN1	GAIN0	Volume Gain (dB)	Input Resistance, R_{in} (kΩ)
0	0	20	60
0	1	26	30
1	0	32	15
1	1	36	9

- **Shutdown ($\overline{SD}$) control**

  Pulling $\overline{SD}$ pin low will let AD52067 operate in low-current state for power conservation. The AD52067 outputs will enter mute once $\overline{SD}$ pin is pulled low, and regulator will also disable to save power. If let $\overline{SD}$ pin floating, the chip will enter shutdown mode because of the internal pull low resistor. For the best power-off performance, place the chip in the shutdown mode in advance of removing the power supply.

- **DC detection**

  AD52067 has dc detection circuit to protect the speakers from DC current which might be occurred as input capacitor defect or inputs short on printed circuit board. The detection circuit detects first volume amplifier stage output, when both differential outputs' voltage become higher than a determined voltage or lower than a determined voltage for more than 420ms, the dc detect error will occur and report to $\overline{FAULT}$ pin. At the same time, loudspeaker drivers of right/left channel will disable and enter Hi-Z. This fault can not be cleared by cycling $\overline{SD}$, it is necessary to cycle the PVCC supply.

  The minimum differential input voltages required to trigger the DC detect function are shown in table2. The input voltage must keep above the voltage listed in the table for more than 420msec to trigger the DC detect fault. The equivalent class-D output duty of the DC detect threshold is listed in table3.

Table 2. DC Detect Threshold

AV (dB)	Vin (mV, differential)
20	250
26	125
32	63
36	35

Table 3. Output DC Detect Duty (for Either Channel)

PVCC (V)	Output Duty Exceeds
8	20.8%
12	20.8%

- **Thermal protection**

  If the internal junction temperature is higher than 150^{o}C, the outputs of loudspeaker drivers will be disabled and at low state. The temperature for AD52067 returning to normal operation is about 125^{o}C. The variation of protected temperature is about 10%.

- **Short-circuit protection**

  To protect loudspeaker drivers from over-current damage, AD52067 has built-in short-circuit protection circuit. When the wires connected to loudspeakers are shorted to each other or shorted to PGND or to PVCC, overload detectors may activate. Once one of right and left channel overload detectors are active, the amplifier outputs will enter a Hi-Z state and the protection latch is engaged. The short protection fault is reported on $\overline{\text{FAULT}}$ pin as a low state. The latch can be cleared by reset $\overline{\text{SD}}$ or power supply cycling.

  The short circuit protection latch can have auto-recovery function by connect the $\overline{\text{FAULT}}$ pin directly to $\overline{\text{SD}}$ pin. The latch state will be released after 420msec, and the short protection latch will re-cycle if output overload is detected again.

- **Under-voltage detection**

  When the PVCC voltage is lower than 4V, loudspeaker drivers of right/left channel will be disabled and kept at low state. Otherwise, AD52067 return to normal operation.

- **Power limit function**
  - The voltage at PLIMIT pin can used to limit the power of first gain control amplifier output. Add a resistor divider from GVDD to ground to set the voltage V_{PLIMIT} at the PLIMIT pin. The voltage V_{PLIMIT} sets a limit on the output peak-to-peak voltage. PLIMIT is adjustable from 1.33V~2.5V.

For normal BTL operation (Stereo) and PBTL (Mono) operation:

$$Po@1\% = \frac{\left[\frac{2.5V - P_{LIMIT}}{2.1V + 0.81 \times P_{LIMIT}} \times 2 \times PVDD \times (1.23 - 0.0076 \times PVDD)\right]^2}{2 \times R_L}$$

$$Po@10\% = (Po@1\%) \times (1.2 + 0.02 \times PVDD)$$

Connect PLIMIT pin to ground or GVDD to disable power limit function. The output variation during power limit feature enable may have +-20% variation due to process window.

- **PBTL (Mono) function**

AD52067 provides the application of parallel BTL operation with two outputs of each channel connected directly. If the PBTL pin is tied high, the positive and negative outputs of left and right channel are synchronized and in phase. Apply the input signal to the RIGHT channel input in PBTL mode and let the LEFT channel input grounded, and place the speaker between the LEFT and RIGHT outputs. The output swing is doubled of that in normal mode. See the application circuit example for PBTL (Mono) mode operation. For normal BTL (Stereo) operation, connect the PBTL pin to ground.

Boost Converter Application information

- **Inductor Selection**

  Inductance value is decided based on different condition. 3.3uH to 6.8µH inductor value is recommended for general application circuit. There are three important inductor specifications, DC resistance, saturation current and core loss. Low DC resistance has better power efficiency.

- **Capacitor Selection**

  The output capacitor is required to maintain the DC voltage. Low ESR capacitors are preferred to reduce the output voltage ripple. Ceramic capacitor of X5R and X7R are recommended, which have low equivalent series resistance (ESR) and wider operation temperature range.

- **Diode Selection**

  Schottky diodes with fast recovery times and low forward voltages are recommended. Ensure the diode average and peak current rating exceed the average output current and peak inductor current. In addition, the diode's reverse breakdown voltage must exceed the output voltage.

- **Output Voltage Setting**

  The output voltage of AD52067 can be adjusted by a resistive divider according to the following formula:

$$V_{OUT} = V_{REF} * \left(1 + \frac{R_1}{R_2}\right) = 0.6 * \left(1 + \frac{R_1}{R_2}\right)$$

  The resistive divider senses the fraction of the output voltage as shown in Figure.1 Using large feedback resistor can increase efficiency, but too large value affects the device's output accuracy because of leakage current going into device's FB pin. The recommended value for R2 is therefore in the range of 10~20KΩ.

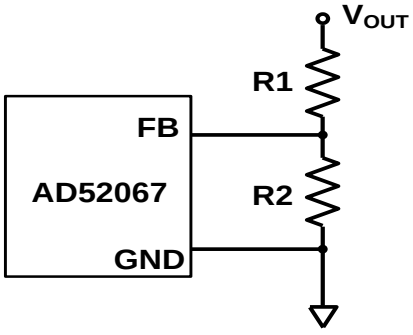


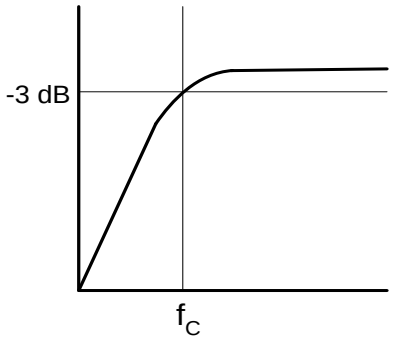
Figure.1 The resistive divider senses the fraction of the output voltage

Audio Application information

- **Input capacitors (C_{in})**

  The performance at low frequency (bass) is affected by the corner frequency (f_c) of the high-pass filter composed of input resistor (R_{in}) and input capacitor (C_{in}), determined in equation (2). Typically, a 0.1μF or 1μF ceramic capacitor is suggested for C_{in}. The resistance of input resistors is different at different gain setting. The respective gain and input resistance are listed in Table 1 (shown at GAIN SETTING). However, there is 20% variation in input resistance from production variation.

$$f_c = \frac{1}{2\pi R_{in} C_{in}} \ (\mathrm{Hz}) \quad \cdots\cdots\cdots (2)$$



- **Ferrite Bead selection**

  If the traces from the AD52067 to speaker are short, the ferrite bead filters can reduce the high frequency emissions to meet FCC requirements. A ferrite bead that has very low impedance at low frequency and high impedance at high frequency (above 1MHz) is recommended. The impedance of the ferrite bead can be used along with a small capacitor with a value around 1000pF to reduce the frequency spectrum of the signal to an acceptable level.

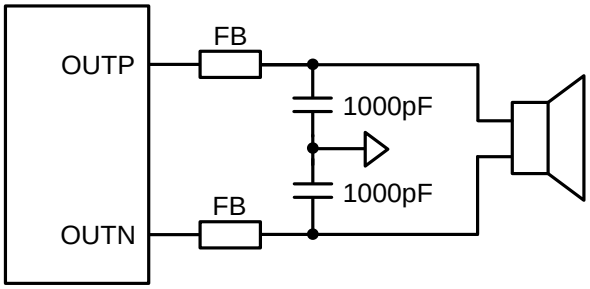


Figure 2. Typical Ferrite Bead Filter

- **Output LC Filter**

  If the traces from the AD52067 to speaker are not short, it is recommended to add the output LC filter to eliminate the high frequency emissions. Figure 3 shows the typical output filter for 8Ω speaker with a cut-off frequency of 27 kHz and Figure 4 shows the typical output filter for 4Ω speaker with a cut-off frequency of 27 kHz.

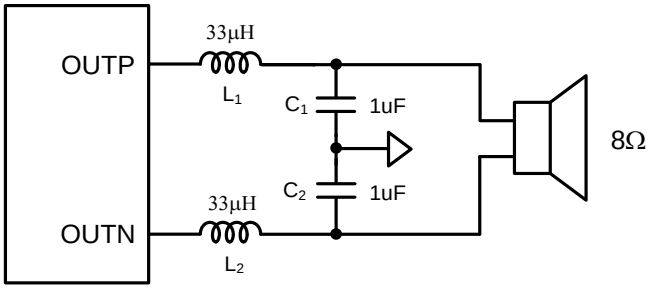


Figure 3. Typical LC Output Filter for 8Ω Speaker

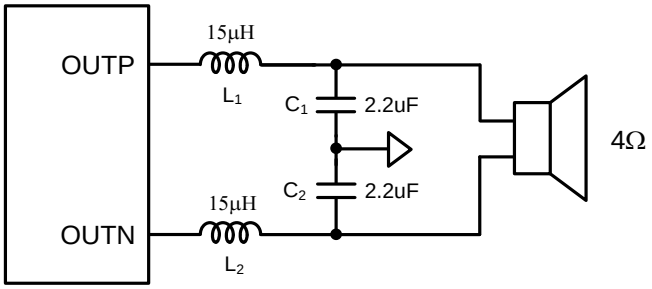


Figure 4. Typical LC Output Filter for 4Ω Speaker

- **Power supply decoupling capacitor (Cs)**

  Because of the power loss on the trace between the device and decoupling capacitor, the decoupling capacitor should be placed close to PVCC and PGND to reduce any parasitic resistor or inductor. A low ESR ceramic capacitor, typically 1000pF, is suggested for high frequency noise rejection. For mid-frequency noise filtering, place a capacitor typically 0.1μF or 1μF as close as possible to the device PVCC leads works best. For low frequency noise filtering, a 100μF or greater capacitor (tantalum or electrolytic type) is suggested.

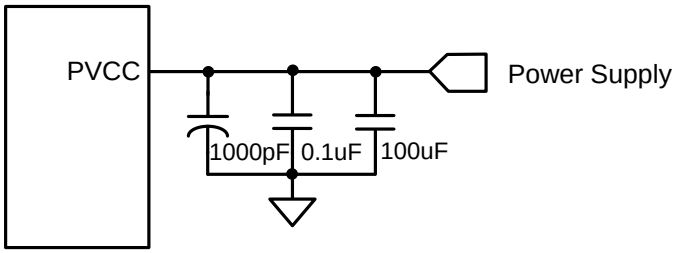
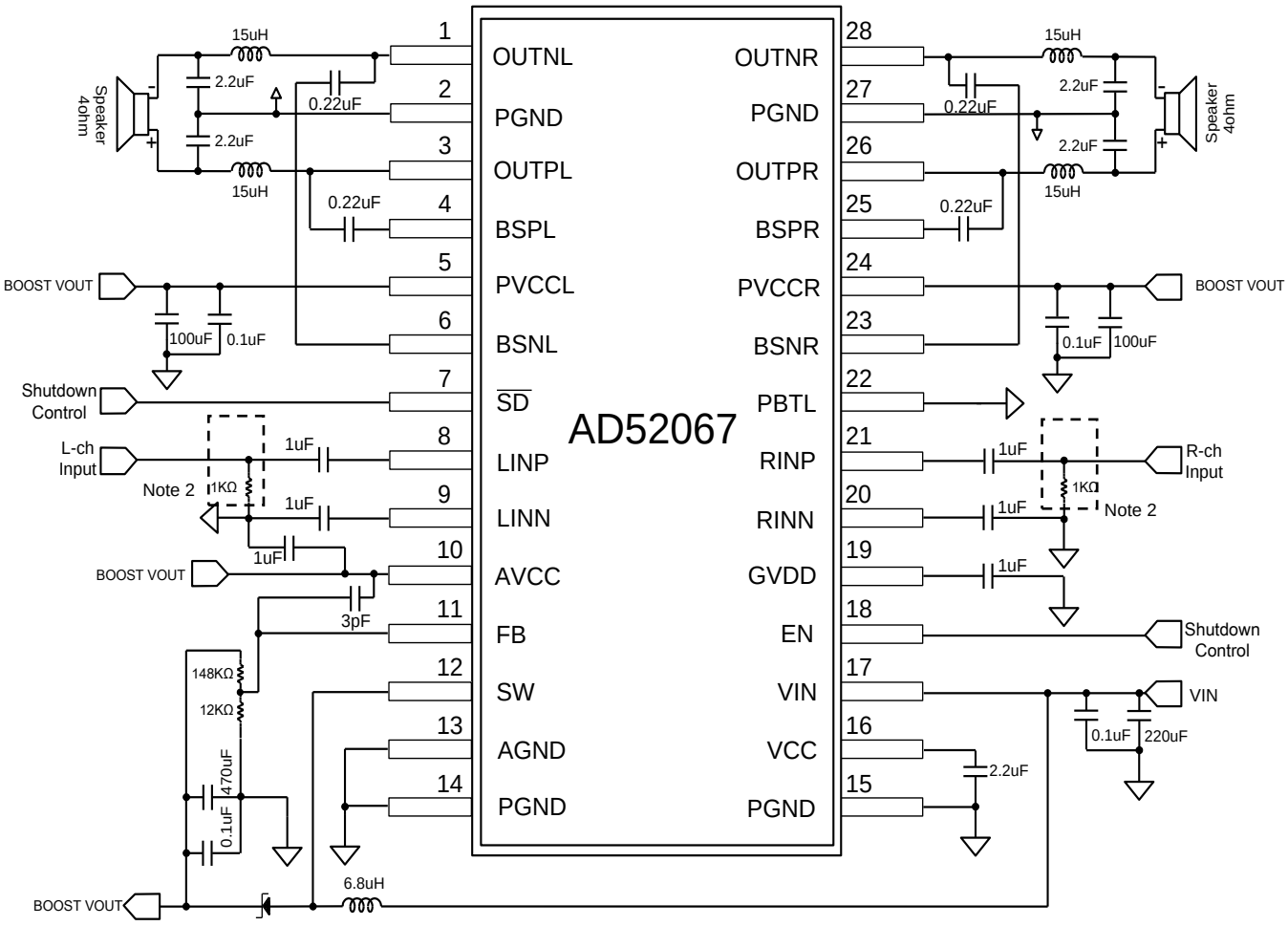


Figure 5. Recommended Power Supply Decoupling Capacitors.

Application Circuit Example

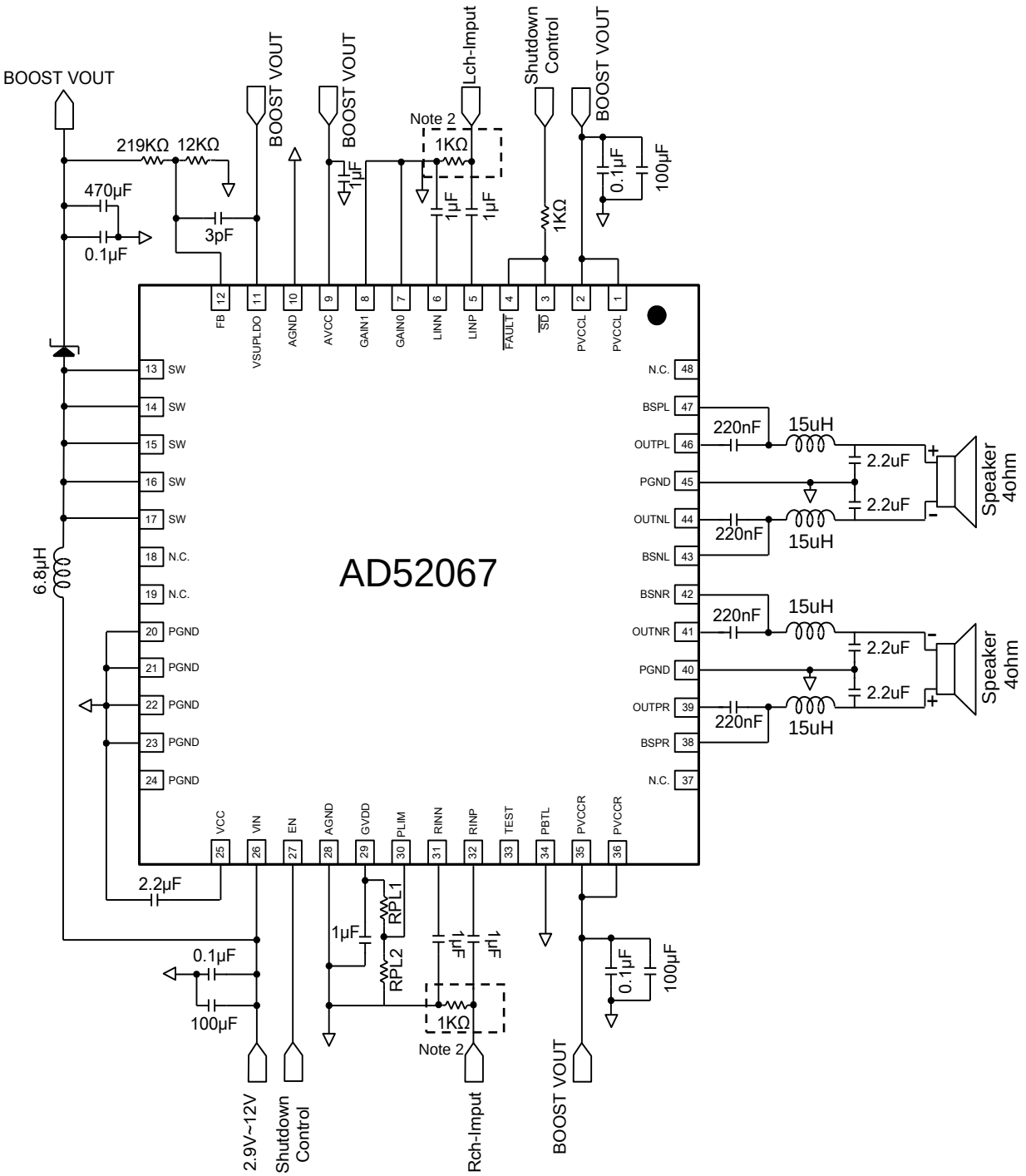
- Application circuit for Stereo (BTL) mode configuration and Single-Ended Input



Note 2: These resistances must be connected to ground, resistance=1Kohm.

Application Circuit Example

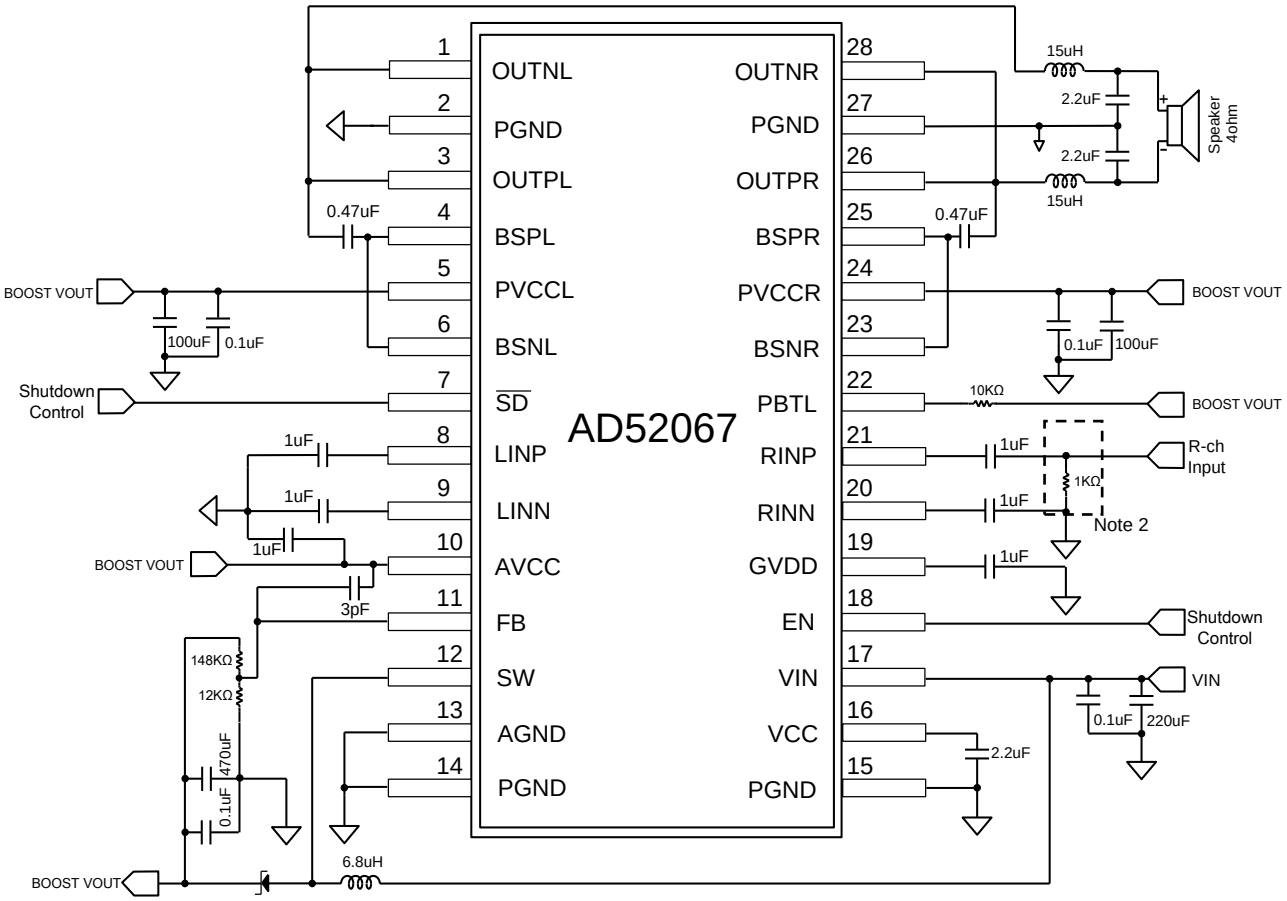
- Application circuit for Stereo (BTL) mode configuration and Single-Ended Input



Note 2: These resistances must be connected to ground, resistance=1Kohm.

Application Circuit Example

- Application circuit for Mono (parallel BTL) mode configuration and Single-Ended Input

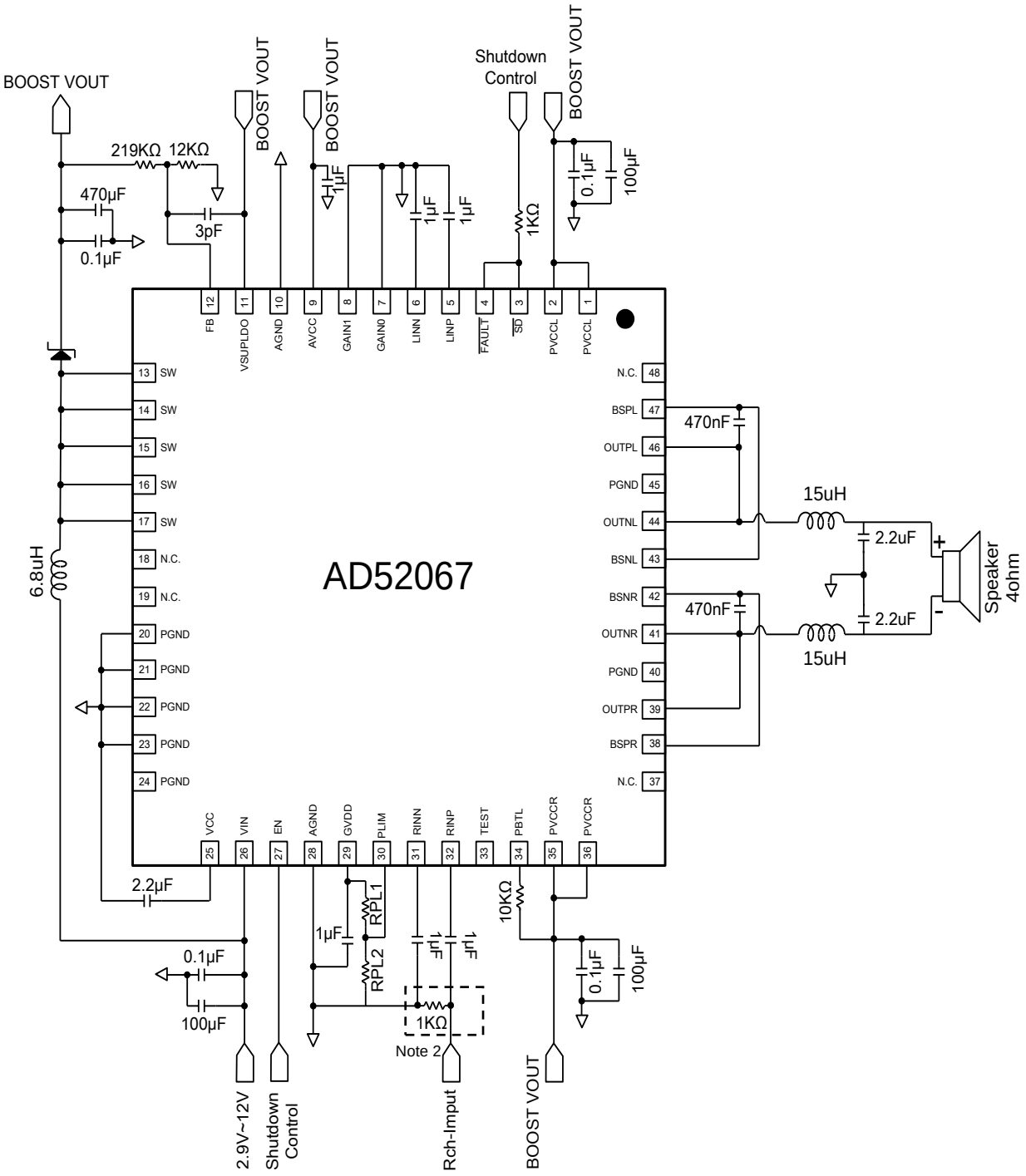


Note 2: These resistances must be connected to ground, resistance=1Kohm.

Note 3: Be noted that input should be applied on R-channel only for Mono application.

Application Circuit Example

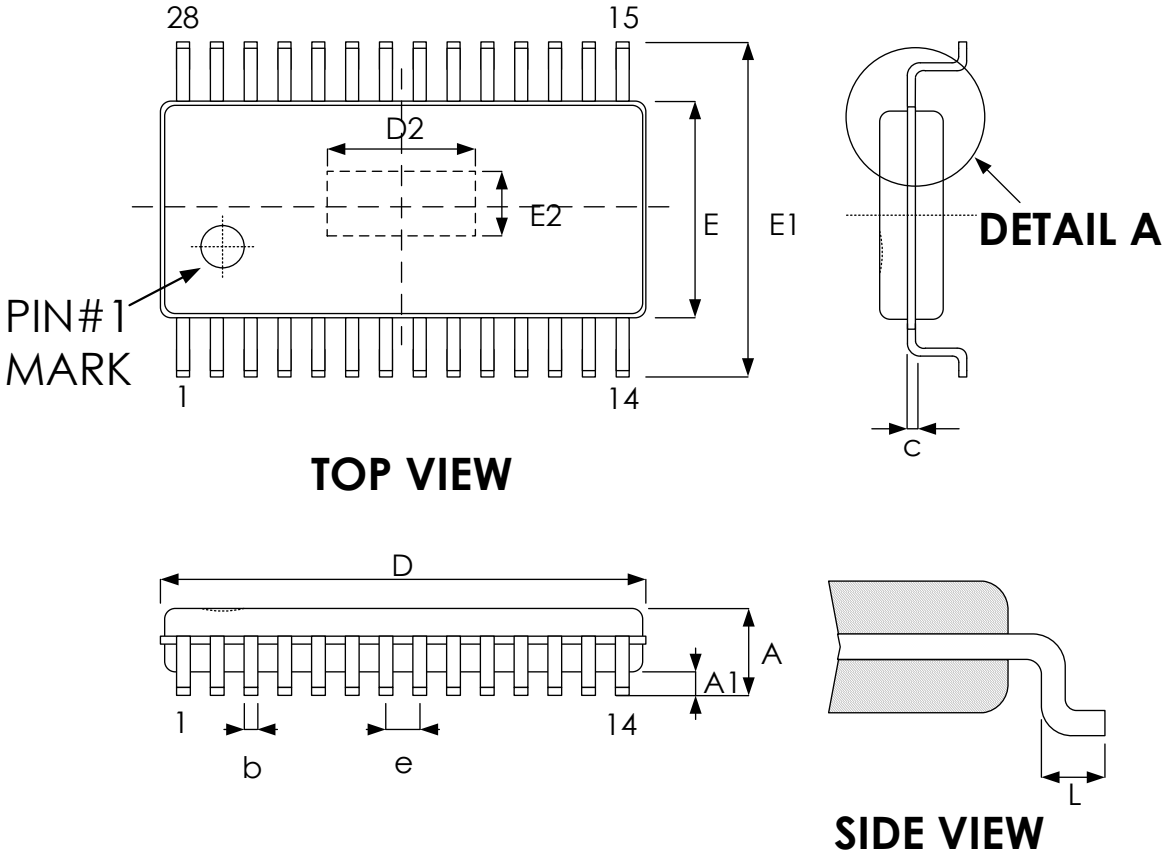
- Application circuit for Mono (parallel BTL) mode configuration and Single-Ended Input



Note 2: These resistances must be connected to ground, resistance=1Kohm.

Note 3: Be noted that input should be applied on R-channel only for Mono application.

Package Outline Drawing
TSSOP-28 (173 mil)



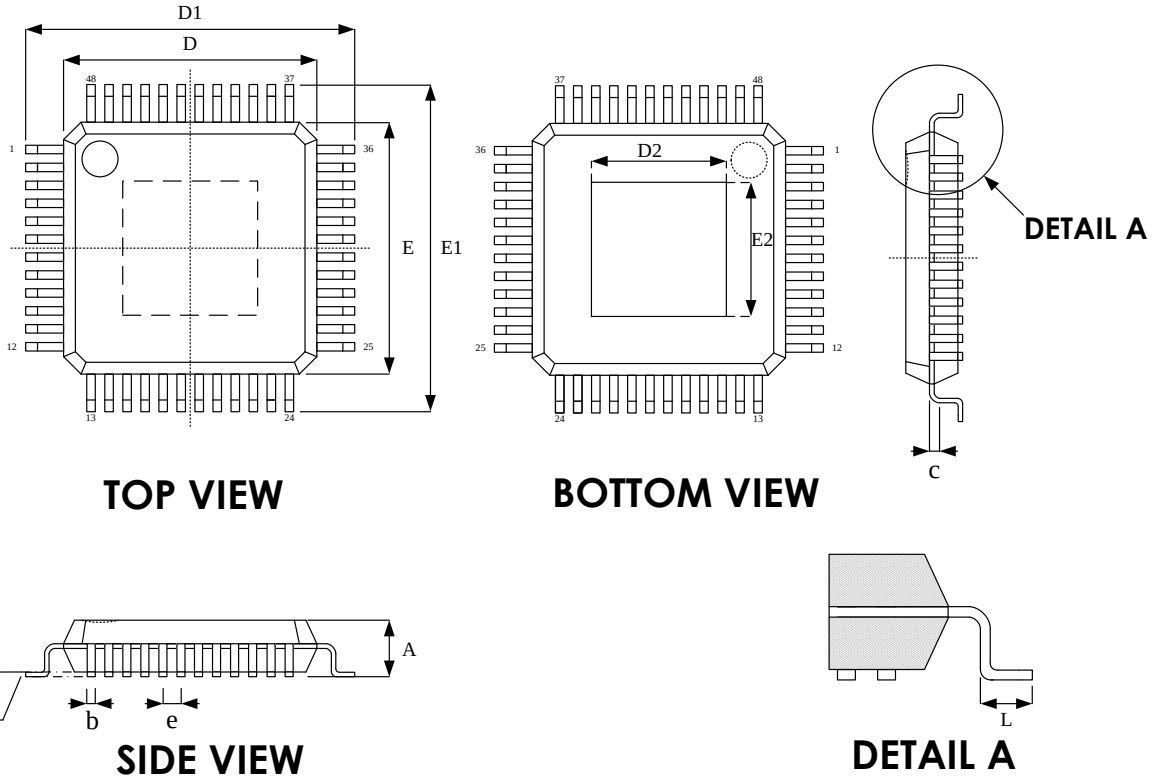
Symbol	Dimension in mm	
	Min	Max
A	--	1.20
A1	0.05	0.15
b	0.19	0.30
c	0.09	0.20
D	9.60	9.80
E	4.30	4.50
E1	6.30	6.50
e	0.65 BSC	
L	0.45	0.75

Exposed pad

	Dimension in mm	
	Min	Max
D2	5.00	6.40
E2	2.50	2.90

Package Dimensions

- **E-LQFP 48L (7x7mm)**



Symbol	Dimension in mm	
	Min	Max
A	--	1.60
A1	0.05	0.15
b	0.17	0.27
c	0.09	0.20
D	6.90	7.10
D1	8.90	9.10
E	6.90	7.10
E1	8.90	9.10
e	0.50 BSC	
L	0.45	0.75

Exposed pad

	Dimension in mm	
	Min	Max
D2	4.31	5.21
E2	4.31	5.21

Revision History

Revision	Date	Description
0.1	2016.11.14	Draft version.
0.2	2016.12.16	Modify measurement data (with LC filter performance) base on MP sample.
0.3	2017.05.11	Modify ordering Information
1.0	2017.12.12	Remove preliminary word and change version to 1.0
1.1	2018.03.29	Add Tape/Reel information
1.2	2019.02.20	Update gain spec to +/-1dB and POD
1.3	2020.11.03	Remove 32dB option and change LQFP-48 option by request

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